INTERSIL

LD110/LD111
3½-Digit A/D Converter Set
LD114 Multiple-Option Digital Processor

4

FEATURES

- Accuracy 0.05% Of Reading ±1 Count
- Two Voltage Ranges – 1.999 V and 199.9 mV
- Sampling Rates up to 12 Samples/Second
- FET Input for $Z_{in} > 1000\ M\Omega$
- Auto-Zero Minimizes Effects of Offset, Drift and Temperature
- Auto-Polarity
- Multiplexed Parallel BCD or Serial BCD Output (LD114)
- Active High or Active Low Logic Outputs (LD114)
- Overrange and Underrange Signals Available for Auto-Ranging Capability.
- ÷512 Output Available for Phase Locked Loop Clock (LD114)
- TTL Compatible Outputs

GENERAL DESCRIPTION

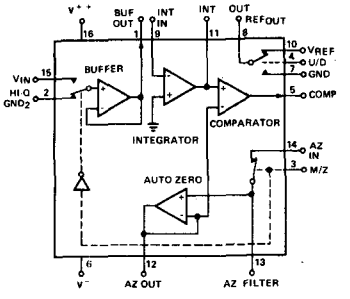
The monolithic LD111 analog processor contains a bipolar comparator, a bipolar integrating amplifier, two MOS-FET input unity gain amplifiers, several P-channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. A wide range of conversion rates (1/3 to 12 samples per second) as well as two voltage ranges can be accommodated using externally determined RC time constants. All amplifiers are internally compensated.

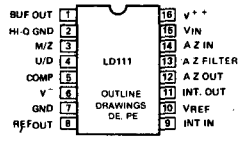
The PMOS LD110/LD114 synchronous digital processor combines the counting, storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing function of the analog processor. Seventeen static latches store the 3½ digits of BCD data as well as overrange, underrange and polarity information.

In the LD110, nine push-pull output buffers (capable of driving one standard TTL load each) provide the sign, digit strobe and multiplexed BCD data outputs, all of which are active high. The digit scan is an interlaced format of digits 1, 3, 2, and 4.

In the LD114, ten push-pull output buffers (capable of driving one standard TTL load) provide the clock frequency ÷512, sign, digit strobe and multiplexed BCD data. Four data output format options allow the user to tailor the BCD output to his circuit requirements.

LD111 ANALOG PROCESSOR

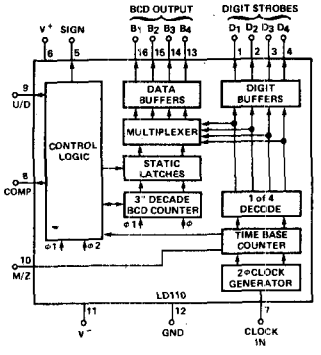


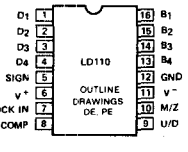


ORDER NUMBER
LD111CJ-PLASTIC
LD111CP-CERAMIC

TOP VIEW

LD110 DIGITAL PROCESSOR

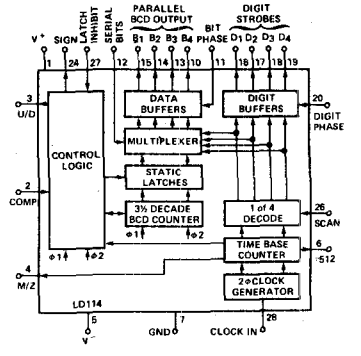


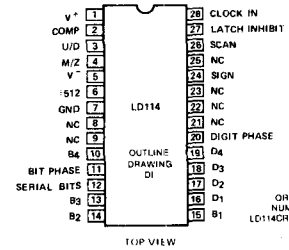


ORDER NUMBER
LD110CJ-PLASTIC
LD111CP-CERAMIC

TOP VIEW

LD114 DIGITAL PROCESSOR





ORDER NUMBER
LD114CH-CERAMIC

TOP VIEW

ABSOLUTE MAXIMUM RATINGS

V_{IN} . . . . . ±5.0V
$V^{++} - V^{-}$ (LD111) 30V
V^{+} 6V
$V^{+} - V^{-}$ (LD110/LD114) 20V
Voltage on any pin relative to V^{+} (LD114) . . 0.3V to −20V
V_{REF} . . . . . V^{++}

Operating Temperature . . . . . 0 to 70°C
Storage Temperature . . . . . −65°C to 150°C
Power Dissipation (Package, LD110/LD111)* 750mW
Power Dissipation (Package, LD114)* 1200mW

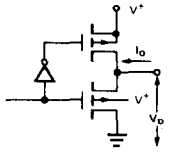
*Device mounted with all leads welded or soldered to PC Board, Derate 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS $V^{++} = 12V, V^{+} = 5V, V^{-} = 5V, V_{REF} = 8.2V, T_A = 25°C$.

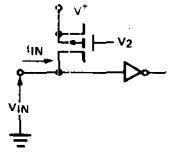
	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	Clock Frequency	f_{IN}	50% Duty Cycle		30.7		kHz
	Input Bias Current	I_{IN}	$T_A = 25°C$		4		pA
			$T_A = 70°C$		40		
	Normal Mode Rejection	NMR	$f_L = 60$ Hz		40		dB
	Clock Input Current, Low	I_{CL}	V_{CLOCK} in = 0.4 V			-500	µA
	Comparator	I_{INL}	$V_{INL} = -12$ V			-100	
	Latch Inhibit	I_{INL}	$V_{INL} = -12$ V		180	-600	
	Format Option Inputs	I_{INH}	$V_{INH} = V_{SS}$		25	400	
OUTPUT	Measure/Zero Voltage, Low	V_{OL1}	$I_{OL} = 150\ \mu A$			0.4	V
	Measure/Zero Voltage, High	V_{OH1}	$I_{OH} = -200\ \mu A$	2.4			
	Up/Down Logic Voltage, Low	V_{OL2}	$I_{OL} = 250\ \mu A$			0.4	
	Up/Down Logic Voltage, High	V_{OH2}	$I_{OH} = -200\ \mu A$	2.4			
	Digits, Bits, Sign Voltage, ÷512*	V_{OL3}	$I_{OL} = 1.6$ mA			0.4	
	Analog Comparator Voltage	V_{OH3}	$I_{OH} = -100\ \mu A$	2.4			
	Data Bit Voltage, High	V_{OH4}	$I_{OH} = -200\ \mu A$	2.4			
	Digits, Sign Voltage, ÷512*	V_{OH5}	$I_{OH} = -800\ \mu A$	2.4			
SWITCH	ON Resistance, Auto Zero Switch	$r_{DS(on)}$	$V_{AZ(in)} = -4.0$ V, $I_S = -50\ \mu A$		11	50	kΩ
	ON Resistance, Up/Down Switch	$r_{DS(on)}$	$I_S = 1$ mA		650	3000	Ω
	Up/Down Switch Temperature Coefficient	TC			0.20	0.50	%/°C
SUPPLY	Supply Current, LD111	I^{++}			2.2	3.5	mA
	Supply Current, LD111	I_A^-			-1.8	-3.0	
	Supply Current, LD110/114	I_D^-			-17	-23	
	Supply Current, LD110/114	I^{+}			17.4	24	
	Power Supply Rejection Ratio, V^{++}	$PSRR_1$		80	85		dB
	Power Supply Rejection Ratio, V^{-}	$PSRR_2$		60	65		
	Reference Current Rejection Ratio		$R_{REF} = R_2 = 100K\Omega$, $V_{IN} = 2V$	35	41		nA/LSB

*÷512 output applicable to LD114 only

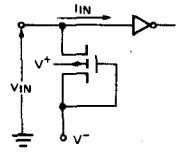
INPUT/OUTPUT SCHEMATICS



OUTPUT BUFFERS
(Digits, Bits, Sign, 512, M/Z, U/D)



COMPARATOR, CLOCK, LATCH INHIBIT INPUTS



FORMAT OPTION INPUTS
(Bit Phase, Digit Phase, Scan, Serial Bits)

DESCRIPTION OF PIN FUNCTIONS (LD110/LD114)

V^+ – Positive Supply Voltage. Recommended level is +5 volts ± 10%.

V^- – Negative Supply Voltage. Recommended level is -12 volts ±10%.

CLOCK IN – This input accepts a TTL or MOS level clock to drive the synchronous digital circuitry. Acceptable duty cycles on the external clock range from 30% high, 70% low to 70% high, 30% low for clock frequencies from 2 kHz to 75 kHz. Although any clock frequency between 2 kHz and 75 kHz may be used, clock frequencies that are integer divisions of $2048F_L$ ($F_{IN} = 2084F_L/n$, n = 2, 3, 4, 51, F_L = Line Frequency) provide measure and zero periods that are integer multiples of the line frequency period ($T_{zero} = n/F_L$, $T_{measure} = 2n/F_L$). Line frequency interference is minimized by the selection of one of these 50 frequencies.

This input has an active pull-up to V^+.

M/Z – Measure/Zero Logic Output. This 0 to 5 volt logic output successively provides Autozero and Measurement intervals of 2048 and 4096 clock periods respectively. This output is compatible with CMOS logic and directly interfaces with the LD111 analog processor.

÷512 (LD114) – This TTL compatible output (1 standard load) provides the necessary clock frequency division for a phase locked loop digital clock. The line frequency rejection will be held at the maximum level (>80 dB) when locked to the line frequency.

U/D – Up/Down Logic Output. This output has logic levels of 0 to +5 volts to provide pulse-width modulation of the reference current when used with the LD111 analog processor. This output is CMOS compatible.

COMP – Analog Comparator Input. This input has an active pull-up to V^+ for a comparator "high" state. This pin must be pulled down to V^- for a "low" comparator state.

An End-of-Conversion Signal can be decoded from the three interconnecting logic lines (M/Z, U/D, Comp) using the following CMOS logic.

$\overline{M/Z + U/D + Comp}$ = E.O.C.

SIGN – Sign of Analog Input Polarity. This TTL level output is a static signal which is either 0 or V^+ for a negative or positive input polarity respectively.

BIT PHASE (*LD114) – The bit outputs will be active high (positive) logic if this pin is left open or connected to V^-. The application of V^+ to this pin will give a complemented output (negative logic).

DIGIT PHASE (*LD114) – The Digit Strobe outputs will be of positive logic if this pin is left open or connected to V^- (an active pull-down is internally connected to V^-). Applying V^+ to this pin will complement the outputs to give negative logic. Negative logic may simplify interfacing with Common Anode LED, Gas Discharge and Liquid Crystal Displays.

B_1, B_2, B_3, B_4 – BCD Data Bit Output. B_4 represents the most significant bit and B_1 the least significant bit of the BCD output. Bit 4 of digit 4 goes high for an underrange condition (less than 100 counts). These outputs are compatible with 1 standard TTL load.

MUX Underrange = $B_4 \cdot D_4$ (5% of full scale)

D_1, D_2, D_3, D_4 – Digit Strobe Outputs. D_4 is the most significant and D_1 the least significant digit of the 3½ digit output. The digit strobes are each selected in turn when the BCD data bits for that digit appear at the bit outputs.

MUX Overrange = $\overline{D_1 + D_2 + D_3 + D_4}$ (100% of full scale, count ≥2000).

SCAN (*LD114) – Sequential/Interlace Digit Scan. The digit strobe format will be an interlaced format of digits 1, 3, 2 and 4 if this pin is left open or is connected to V^-. This format is useful for display digits packaged two to an envelope and which require an interdigit blanking period eg. (Beckman Displays). By alternating from envelope, an interdigit blanking period is effectively provided.

The application of V^+ to this pin will give a sequencial scan of digits 1, 2, 3 and 4. This format may be more useful in interfacing with data acquisition equipment.

LATCH INHIBIT (*LD114) – Connecting this pin to V_2 will prevent updating of the internal static latches, thus providing a "hold" function. Leaving this pin disconnected will allow the latches to be updated once each sampling period.

DESCRIPTION OF PIN FUNCTIONS (LD110/LD114) Cont.

SERIAL BITS (*LD114)—Parallel/Serial Bit Output Format. The BCD data bits for each digit will appear simultaneously with the digit strobe if the parallel bit option is selected.

This format is useful for driving multiplexed displays. The parallel bit format is available when this pin is left open or connected to V^-.

The application of V^+ to this pin will put all of the BCD data bits in a serial order at the bit 4 output.

Bit outputs 1, 2, and 3 contain time markers to identify the data. The most significant bit of the last digit (D_4) is identified by a marker at the bit 2 output. The least significant bit of the first Digit (D_1) is identified by a marker at bit 3. Bit 1 shows a marker for the least significant bit of each digit.

All output format options are independent of one another (i.e., the serial bit output can have either sequential or interlace scan, Positive or Negative logic).

(*For LD110, action is described for "pin left open".)

DESCRIPTION OF PIN FUNCTIONS – LD111

BUF OUT – The output of this unity gain input buffer amplifier is applied to the integrator summing node through a scaling resistor R_2. The value of this resistor is typically 10 KΩ for a 200.0 mV full-scale and 100 KΩ for a 2.000 V full-scale. The digital output is inversely proportional to the value of this resistor,

$$\text{Count} = \frac{V_{IN}}{V_{REF}} \frac{R_1}{R_2} 8192$$

HI-QUALITY GND – This pin, typically connected to a High Quality Ground point for single ended inputs **CAN BE USED AS THE INVERTING INPUT FOR DIFFERENTIAL SIGNALS.** The digital output will be $V_{IN} - V_{HI} - Q$. When using this differential mode, it is important that resistor R_3 equal Resistor R_2 for proper operation.

M/Z – Measure/Zero Logic Input. Internal level shifting drivers operate the PMOS switches in response to this digital signal.

U/D – Up/Down Logic Input. The logic signal applied to this pin operates a SPDT switch to provide Quantized pulses of charge to the integrator.

COMP – This analog comparator output is an open collector configuration which goes to V^- when "low."

V^- – Negative Supply Voltage. Recommended level is −12V ± 10%.

GND – Analog Processor Ground.

REF_{out} – This voltage output of the SPDT U/D switch, converted to a current by resistor R_1, supplies the reference current to the integrator.

INT. IN – Integrator Summing Node.

V_{REF} – A stable positive reference voltage (5 to 11 V) applied to this pin is the standard to which the input voltage V_{IN} is measured. Ratio measurements can be made by applying a variable to this input (1.0 to 11V).

INT. OUT – The output of the integrating amplifier is made available for application to the Auto-Zero amplifier by means of resistor R_4.

AZ OUT – The output of the unity gain Auto-Zero Amplifier provides a second negative reference current to the integrator through resistor R_3.

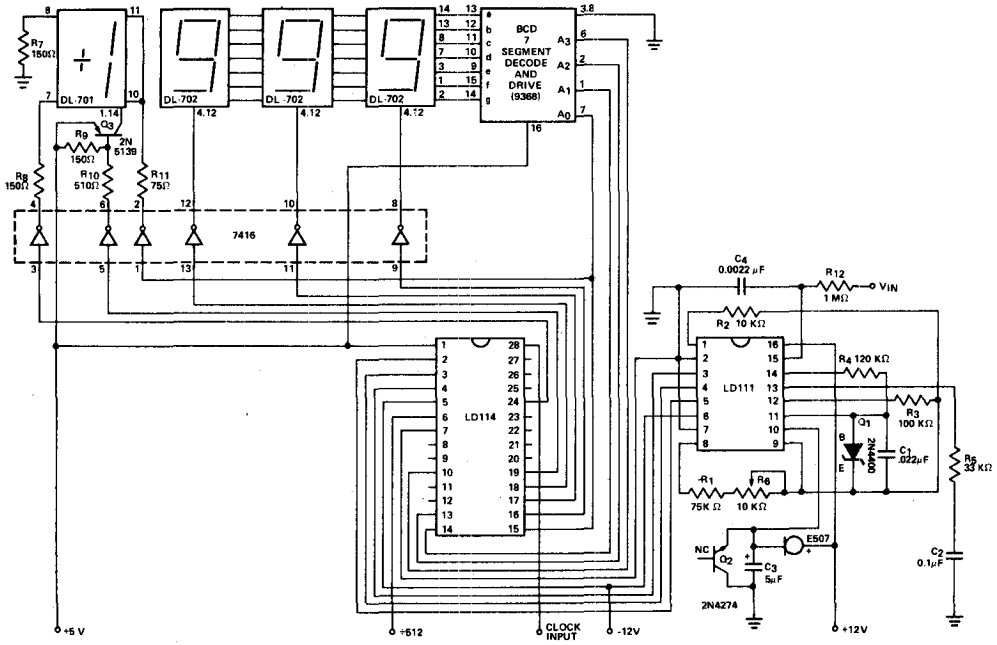
AZ FILTER – The RC filter (R_5 and C_{STRG}) connected to this pin stores. D.C. voltage components to balance amplifier offset and drift components.

AZ IN – This input is switched into the AZ filter during the Zeroing interval.

V_{IN} – Analog Voltage Input. The A/D System digitizes the voltage appearing at this input.

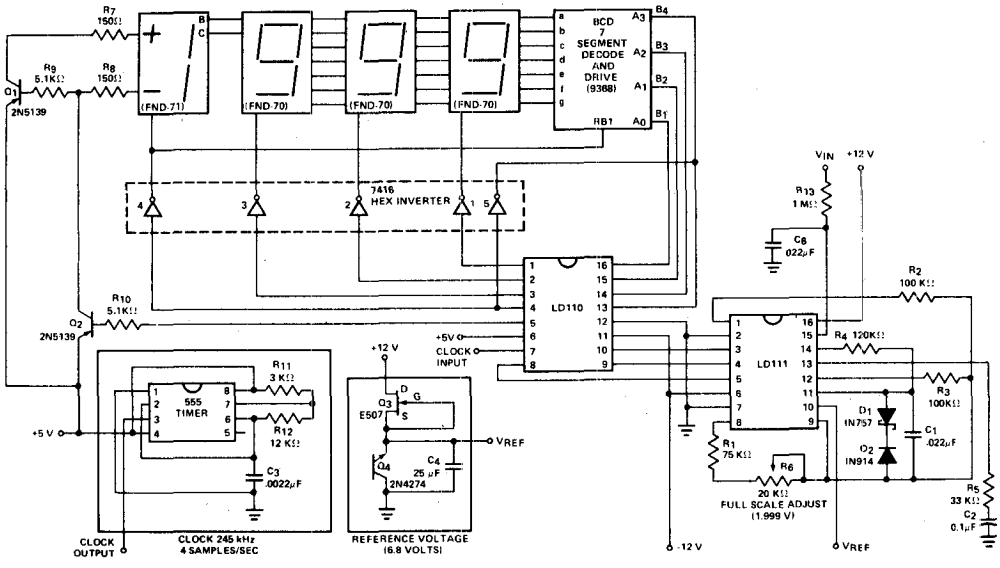
V^{++} – Positive Supply Voltage. The recommended level is +12 volts ± 10%.

APPLICATIONS LD111/LD114



3½ Digit DVM (±200.0 mV)

APPLICATIONS LD110/LD111



3½ Digit DVM (±2.000 Volts)