SPECIFICATION
FOR
APPROVAL

(●) Preliminary Specification
( ) Final Specification

Title	47.0” WUXGA TFT LCD

BUYER	General
MODEL	

SUPPLIER	LG.Display Co., Ltd.
MODEL	LD470WUJ
SUFFIX	SCE1 (RoHS Verified)

APPROVED BY	SIGNATURE / DATE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE / DATE
K. S. Nah / Chief Senior Engineer	
REVIEWED BY	
K.N. Kim / Chief Senior Engineer	
PREPARED BY	
J.H. Song / Senior Engineer	

PD Product Design Dept.
LG Display Co., Ltd

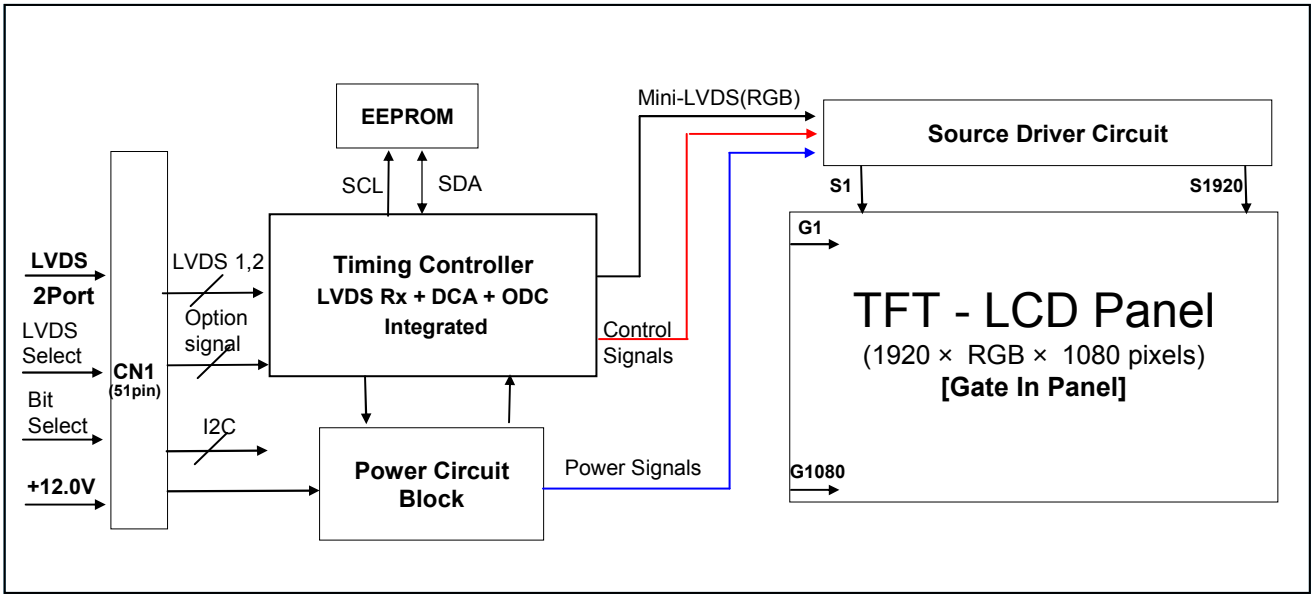
CONTENTS

RECORD OF REVISIONS

Revision No.	Revision Date	Page	Description
0.0	Jun, 19, 2012	-	Preliminary Specification(First Draft)
0.1	Jul, 20, 2012	19	Updated the Front view
0.2	Aug, 06, 2012	2	Updated the Absolute Maximum Ratings
		15	Updated the Contrast Ratio
0.3	Jul, 20, 2012	4	pdated the Surface Treatment
		19	Updated the Front view
0.4	Aug, 13, 2012	14	Updated the Optical Specification
		15, 16	Updated the Notes

1. General Description

The LD470WUJ is a Color Active Matrix Liquid Crystal Display with an integral the Source PCB and Gate implanted on Panel (GIP). The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 46.96 inch diagonally measured active display area with WUXGA resolution (1080 vertical by 1920 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 10-bit gray scale signal for each dot. Therefore, it can present a palette of more than 1.07 Billion colors.
It has been designed to apply the 10-bit 2-port LVDS interface.
It is intended to support Public Display where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	46.96 inch (1192.87mm) diagonal
Outline Dimension	1061.8(H) x 606.8 (V) x 1.75 mm(D) (Typ.)
Pixel Pitch	0.5415 mm x 0.5415 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels, RGB stripe arrangement
Color Depth	10Bit (D), 1.07 Billion colors
Transmittance (With POL)	5,5 %(Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Power Consumption	Total 6.6W (Typ.)
Weight	2.6Kg (Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment (Top)	Hard coating(3H), Anti-reflection treatment of the front polarizer (Reflectance 〈 2%)
Possible Display Type	Landscape and Portrait Enabled

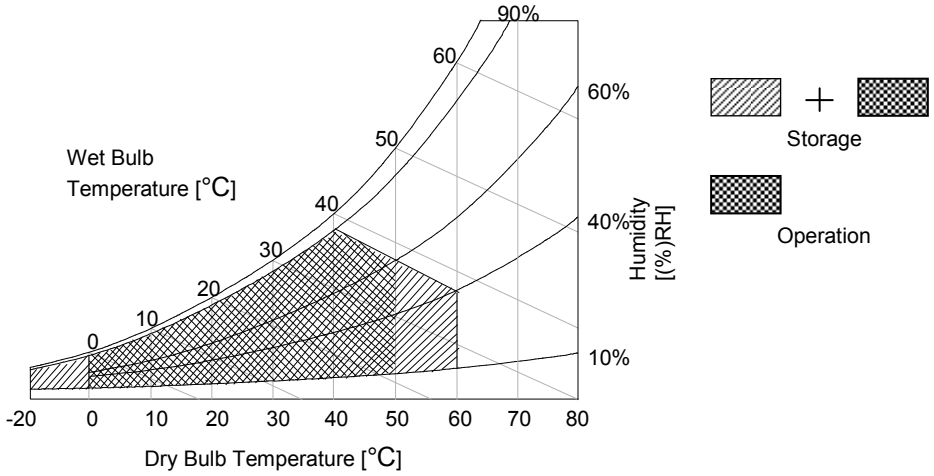
2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or permanent damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value		Unit	Remark
			Min	Max		
Power Input Voltage	LCM	V_{LCD}	-0.3	+14.0	V_{DC}	at 25 ± 2 °C
ON/OFF Control Voltage		VON/OFF	-0.3	+5. 5	V_{DC}	
Operating Temperature		T_{OP}	0	+50	°C	Note 1
Storage Temperature		T_{ST}	-20	+60	°C	
Operating Ambient Humidity		H_{OP}	10	90	%RH	
Storage Humidity		H_{ST}	10	90	%RH	

Note: 1. Ambient temperature condition (Ta = 25 ± 2 °C)
2. Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be Max 39 °C and no condensation of water.
3. Gravity mura can be guaranteed below 40℃ condition.
4. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 68 ℃ with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68 ℃. The range of operating temperature may degrade in case of improper thermal management in final product design.



3. Electrical Specifications

3-1. Electrical Characteristics

It requires one power inputs. That is employed to power for the LCD circuit.

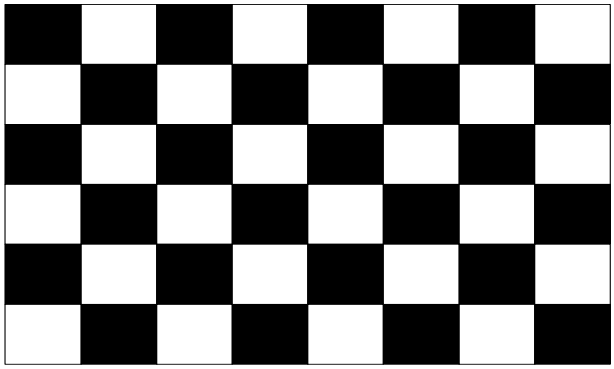
Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Circuit :						
Power Input Voltage	V_{LCD}	11.4	12.0	12.6	V_{DC}	
Power Input Current	I_{LCD}	-	550	715	mA	1
		-	810	1053	mA	2
Power Consumption	P_{LCD}	-	6.6	8.88	Watt	1
Rush current	I_{RUSH}	-	-	5.0	A	3

Note

1. The specified current and power consumption are under the V_{LCD}=12.0V, Ta=25 ± 2°C, fV=120Hz condition, and mosaic pattern(8 x 6) is displayed and fV is the frame frequency.
2. The current is specified at the maximum current pattern.
3. The duration of rush current is about 2ms and rising time of power input is 0.5ms (min.).
4. Ripple voltage level is recommended under ±5% of typical voltage

White : 1023 Gray
Black : 0 Gray



Mosaic Pattern(8 x 6)

3-2. Interface Connections

This LCD module employs a 51-pin connector, It is used for the module electronics

3-2-1. LCD Module

- LCD Connector(CN1): FI-RE51S-HF or Equivalent, Refer to below table.
- Mating Connector : FI-RE51HL

Table 3-1. MODULE CONNECTOR(CN1) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	GND	Ground	27	Bit Select	'H' or NC= 10bit(D) , 'L' = 8bit
2	NC	No Connection	28	RE0N	SECOND LVDS Receiver Signal (A-)
3	NC	No Connection	29	RE0P	SECOND LVDS Receiver Signal (A+)
4	NC	No Connection (Reserved for LGD)	30	RE1N	SECOND LVDS Receiver Signal (B-)
5	NC	No Connection (Reserved for LGD)	31	RE1P	SECOND LVDS Receiver Signal (B+)
6	NC	No Connection (Reserved for LGD)	32	RE2N	SECOND LVDS Receiver Signal (C-)
7	LVDS Select	'H' =JEIDA , 'L' or NC = VESA	33	RE2P	SECOND LVDS Receiver Signal (C+)
8	NC	No Connection	34	GND	Ground
9	NC	No Connection	35	RECLKN	SECOND LVDS Receiver Clock Signal(-)
10	NC	No Connection	36	RECLKP	SECOND LVDS Receiver Clock Signal(+)
11	GND	Ground	37	GND	Ground
12	RO0N	FIRST LVDS Receiver Signal (A-)	38	RE3N	SECOND LVDS Receiver Signal (D-)
13	RO0P	FIRST LVDS Receiver Signal (A+)	39	RE3P	SECOND LVDS Receiver Signal (D+)
14	RO1N	FIRST LVDS Receiver Signal (B-)	40	RE4N	SECOND LVDS Receiver Signal (E-)
15	RO1P	FIRST LVDS Receiver Signal (B+)	41	RE4P	SECOND LVDS Receiver Signal (E+)
16	RO2N	FIRST LVDS Receiver Signal (C-)	42	NC	No Connection
17	RO2P	FIRST LVDS Receiver Signal (C+)	43	NC	No Connection
18	GND	Ground	44	NC	No Connection
19	ROCLKN	FIRST LVDS Receiver Clock Signal(-)	45	GND	Ground
20	ROCLKP	FIRST LVDS Receiver Clock Signal(+)	46	GND	Ground
21	GND	Ground	47	AGP	'H'=AGP, 'L or NC' = NSB
22	RO3N	FIRST LVDS Receiver Signal (D-)	48	VLCD	Power Supply +12.0V
23	RO3P	FIRST LVDS Receiver Signal (D+)	49	VLCD	Power Supply +12.0V
24	RO4N	FIRST LVDS Receiver Signal (E-)	50	VLCD	Power Supply +12.0V
25	RO4P	FIRST LVDS Receiver Signal (E+)	51	VLCD	Power Supply +12.0V
26	NC	No Connection	-	-	-

Note :

1. All GND(ground) pins should be connected together to the LCD module's metal frame.
2. All V_{LCD} (power input) pins should be connected together.
3. All Input levels of LVDS signals are based on the **EIA 644** Standard.
4. Specific pins(pin No. **#2~#6**) are used for internal data process of the LCD module.
   These pins should be no connection.
5. LVDS pin (pin No. **#24,25,40,41**) are used for 10Bit(D) of the LCD module.
   If used for 8Bit(R), these pins are no connection.
6. Specific pin No. **#47** is used for "No signal detection" of system signal interface.
   It should be GND or NC for NSB(No Signal Black) during the system interface signal is not.
   If this pin is "H", LCD Module displays AGP(Auto Generation Pattern).

3-3. Signal Timing Specifications

Table 6 shows the signal timing required at the input of the LVDS transmitter. All of the interface signal timings should be satisfied with the following specification for normal operation.

Table 6-1. TIMING TABLE for NTSC (DE Only Mode)

ITEM		Symbol	Min	Typ	Max	Unit	Note
Horizontal	Display Period	t_{HV}	-	960	-	tclk	
	Blank	t_{HB}	100	140	240	tclk	
	Total	t_{HP}	1060	1100	1200	tclk	2200/2
Vertical	Display Period	t_{VV}	-	1080	-	t_{HP}	
	Blank	t_{VB}	11	45	69	t_{HP}	
	Total	t_{VP}	1091	1125	1149	t_{HP}	
Frequency	DCLK	f_{CLK}	70	74.25	77	MHz	148.5/2
	Horizontal	f_H	65	67.5	70	KHz	
	Vertical	f_V	57	60	63	Hz	

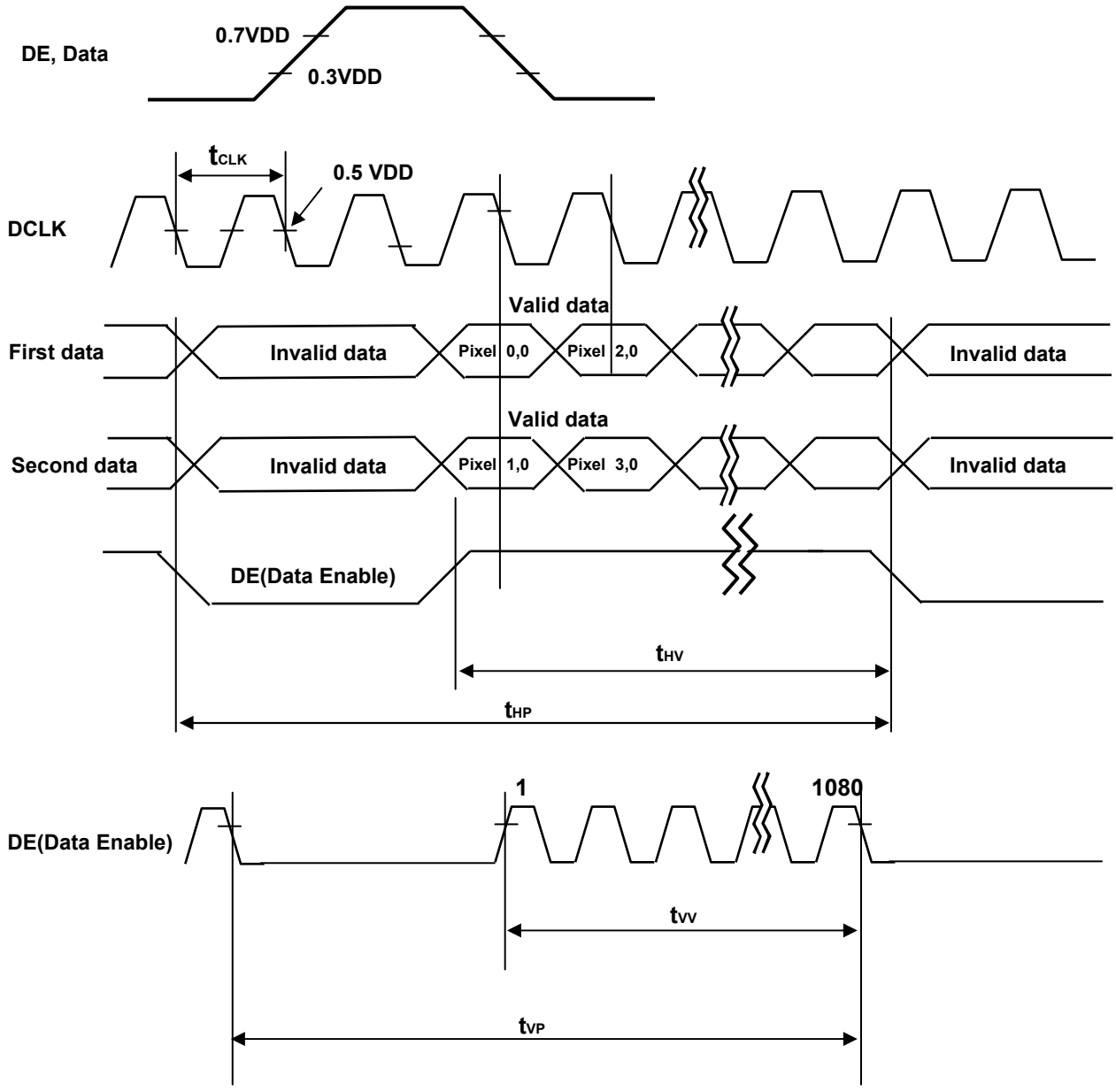
Table 6-2. TIMING TABLE for PAL (DE Only Mode)

ITEM		Symbol	Min	Typ	Max	Unit	Note
Horizontal	Display Period	t_{HV}	-	960	-	tclk	
	Blank	t_{HB}	100	140	240	tclk	
	Total	t_{HP}	1060	1100	1200	tclk	2200/2
Vertical	Display Period	t_{VV}	-	1080	-	t_{HP}	
	Blank	t_{VB}	228	270	300	t_{HP}	
	Total	t_{VP}	1308	1350	1380	t_{HP}	
Frequency	DCLK	f_{CLK}	70	74.25	77	MHz	148.5/2
	Horizontal	f_H	65	67.5	70	KHz	
	Vertical	f_V	47	50	53	Hz	

Note The Input of HSYNC & VSYNC signal does not have an effect on normal operation(DE Only Mode).
The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rate.

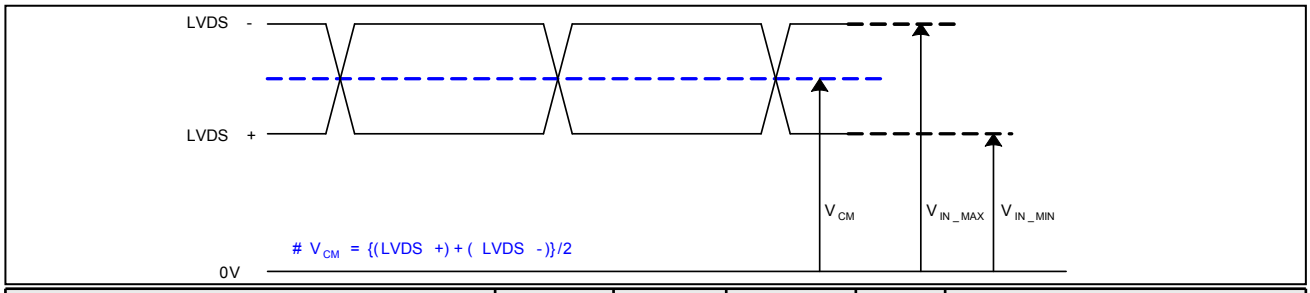
3-4. LVDS Signal Specification

3-4-1. LVDS Input Signal Timing Diagram



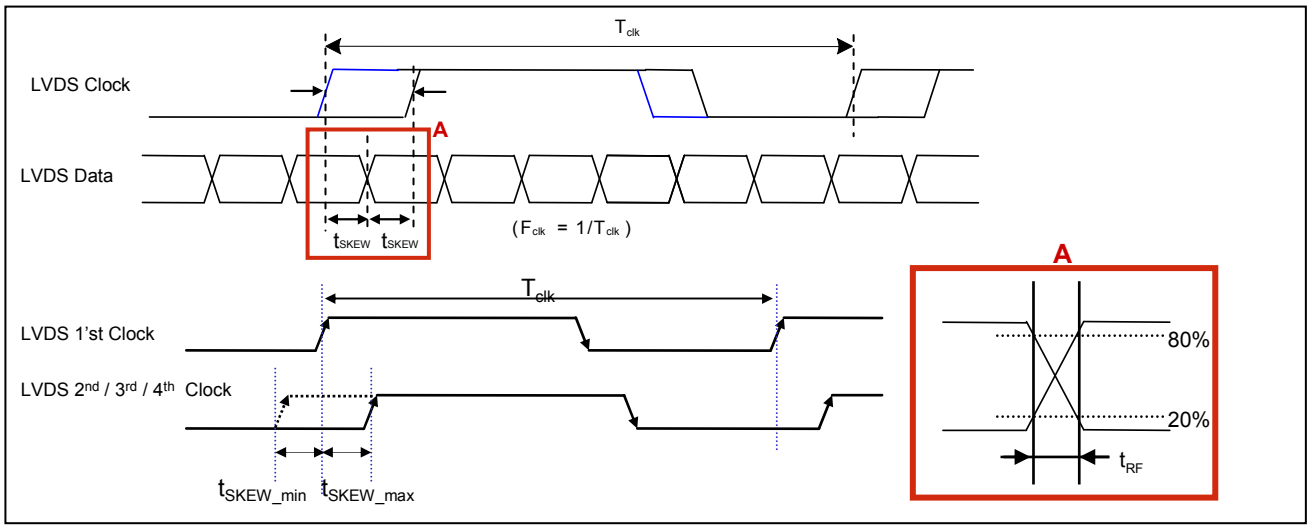
3-4-2. LVDS Input Signal Characteristics

1) DC Specification



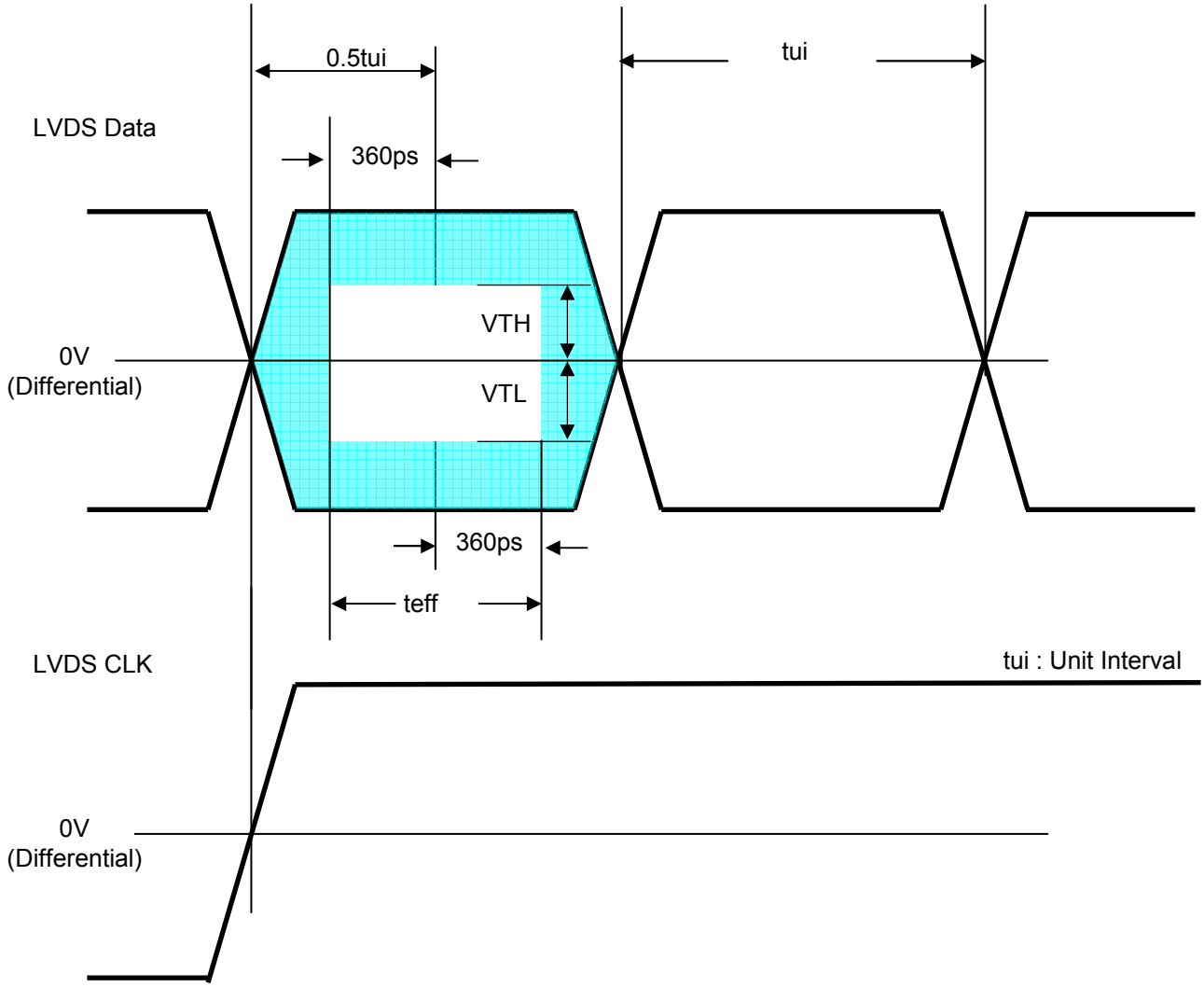
Description	Symbol	Min	Max	Unit	Note
LVDS Common mode Voltage	V_{CM}	1.0	1.5	V	-
LVDS Input Voltage Range	V_{IN}	0.7	1.8	V	-
Change in common mode Voltage	ΔVCM		250	mV	-

2) AC Specification



Description		Symbol	Min	Max	Unit	Note
LVDS Differential Voltage	High Threshold	V_{TH}	100	300	mV	3
	Low Threshold	V_{TL}	-300	-100	mV	
LVDS Clock to Data Skew Margin		t_{SKEW}		|(0.25*T_{clk})/7|	ps	-
LVDS Clock/DATA Rising/Falling time		t_{RF}	260	(0.3*T_{clk})/7	ps	2
Effective time of LVDS		t_{eff}	± 360		ps	-
LVDS Clock to Clock Skew Margin (Even to Odd)		t_{SKEW_EO}		1/7* T_{clk}	T_{clk}	-

Note 1. All Input levels of LVDS signals are based on the EIA 644 Standard.
2. If t_{RF} isn't enough, t_{eff} should be meet the range.
3. LVDS Differential Voltage is defined within t_{eff}



* This accumulated waveform is tested with differential probe

3-5. Color Data Reference

The brightness of each primary color(red,green,blue) is based on the 10-bit gray scale data input for the color. The higher binary input, the brighter the color. Table 8 provides a reference for color versus data input.

Table 8. COLOR DATA REFERENCE

Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB									LSB	MSB									LSB	MSB									LSB
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (0000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (0001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	...	...										...										...									
	RED (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN(0000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(0001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	...	...										...										...									
	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
BLUE	BLUE (0000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (0001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	...	...										...										...									
	BLUE (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	BLUE (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

3-6. Power Sequence

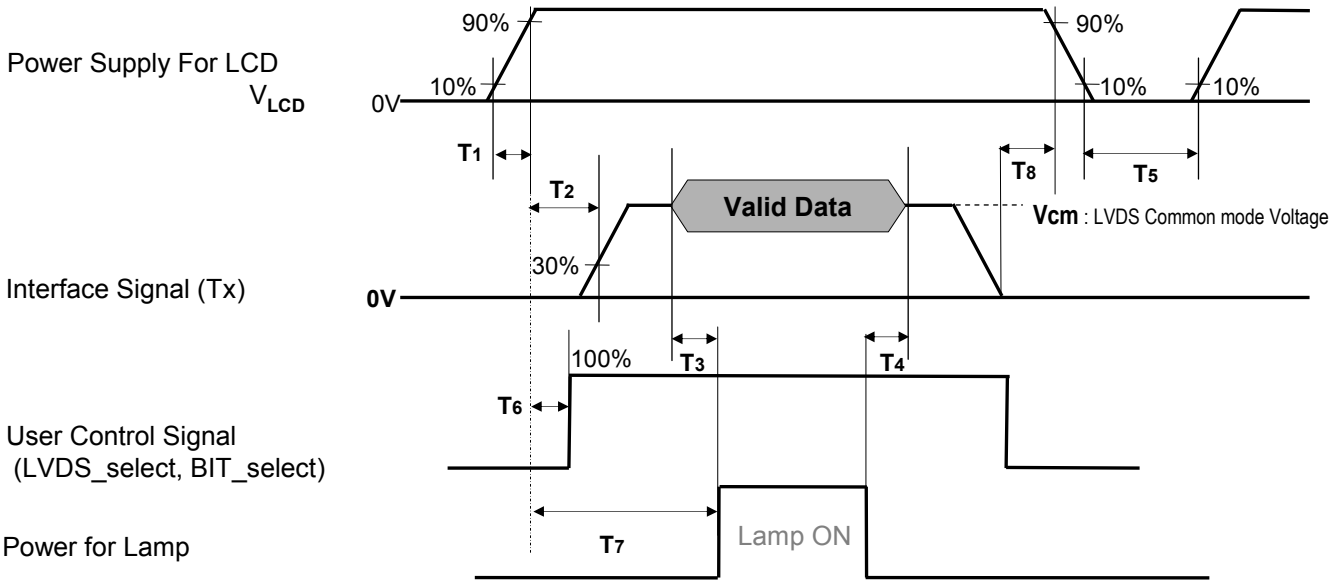


Table 8. POWER SEQUENCE

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	0.5	-	20	ms	
T2	0	-	-	ms	4
T3	200	-	-	ms	3
T4	200	-	-	ms	3
T5	1.0	-	-	s	5
T6	-	-	T2	ms	4
T7	0.5	-	-	s	
T8	100	-	-	ms	6

Note : 1. Please avoid floating state of interface signal at invalid period.
2. When the power supply for LCD (VLCD) is off, be sure to pull down the valid and invalid data to 0V.
3. The **T3** / **T4** is recommended value, the case when failed to meet a minimum specification, abnormal display would be shown. There is no reliability problem.
4. If the on time of signals(Interface signal and user control signals) precedes the on time of Power(V_{LCD}), it will be happened abnormal display. When **T6** is NC status, **T6** doesn't need to be measured.
5. **T5** should be measured after the Module has been fully discharged between power off and on period.
6. It is recommendation specification that **T8** has to be 100ms as a minimum value.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25± 2°C. The values are specified at distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °. FIG. 9 shows additional information concerning the measurement equipment and method.

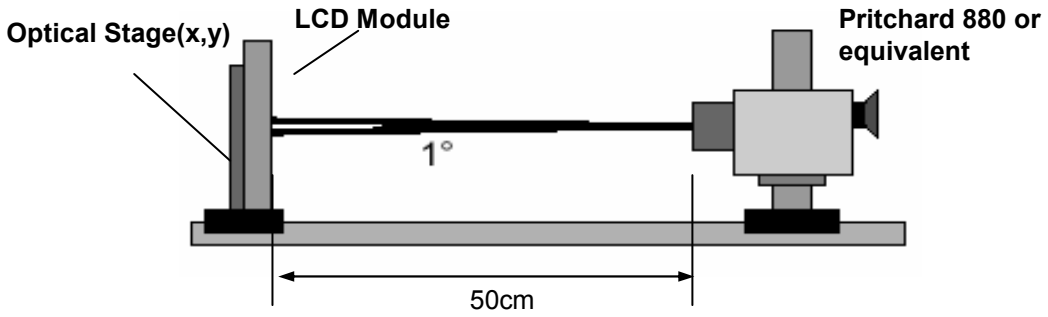


FIG. 9 Optical Characteristic Measurement Equipment and Method

Ta= 25± 2°C, V_{LCD}=12.0V, fv=60Hz, Dclk=74.25MHz VBR_A=1.65V
Back Light : Lamp (Type) 7200nit (Luminance) 0.263/0.240 (Color)

Table 6. OPTICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Contrast Ratio		CR	1000	1200	-		1
Response Time	Gray-to-Gray	G to G	-	9	15	ms	2
Transmittance			-	5.5	-	%	3
Color Coordinates [CIE1931]	RED	Rx	Typ -0.03	0.639	Typ +0.03		
		Ry		0.334			
	GREEN	Gx		0.290			
		Gy		0.606			
	BLUE	Bx		0.146			
		By		0.058			
Viewing Angle (CR>10)							
	x axis, right(ϕ=0°)	θr	89	-	-	degree	4
	x axis, left (ϕ=180°)	θl	89	-	-		
	y axis, up (ϕ=90°)	θu	89	-	-		
	y axis, down (ϕ=270°)	θd	89	-	-		
Gray Scale			-	-	-		5

Notes : 1. Contrast Ratio(CR) is defined mathematically as :

CR(Contrast Ratio) = Maximum CRn (n=1, 2, 3, 4, 5)

$$CRn = \frac{\text{Surface Luminance at position n with all white pixels}}{\text{Surface Luminance at position n with all black pixels}}$$

n = the Position number(1, 2, 3, 4, 5). For more information, see FIG 10.

※. Surface luminance is determined after the unit has been 'ON' and 1Hour after lighting the backlight in a dark environment at 25± 2°C. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see the FIG. 10.

2. Response time is the time required for the display to transit from G(N) to G(M) (Rise Time, TrR) and from G(M) to G(N) (Decay Time, TrD). For additional information see the FIG. 11. (N<M)
※ G to G Spec stands for average value of all measured points.
Photo Detector : RD-80S / Field : 2°

3. Definition of Transmittance (Measure Pattern : Full white)

$$\frac{\text{The intensity of radiation (Output)}}{\text{The intensity of radiation (Input)}} \times 100$$

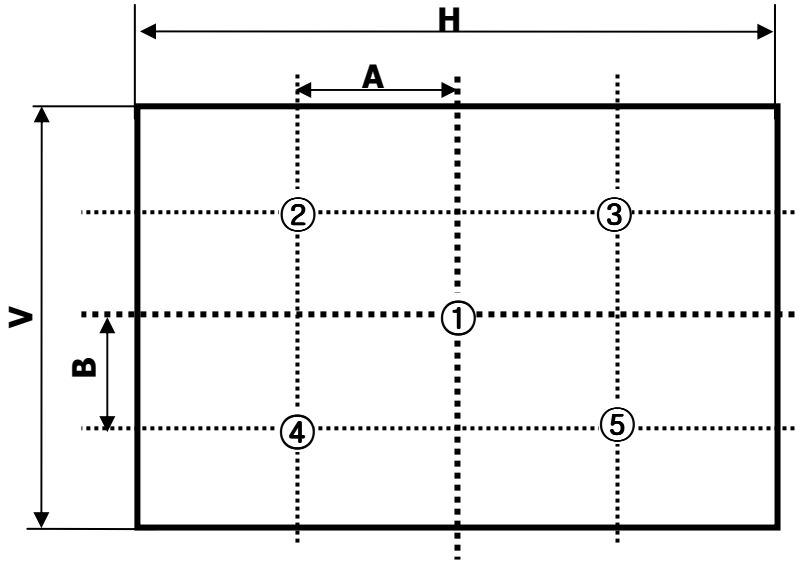
4. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 12.

5. Gray scale specification
Gamma Value is approximately 2.2. For more information, see the Table 7.

Table 7. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ.)
L0	0.07
L63	0.27
L127	1.04
L191	2.49
L255	4.68
L319	7.66
L383	11.5
L447	16.1
L511	21.6
L575	28.1
L639	35.4
L703	43.7
L767	53.0
L831	63.2
L895	74.5
L959	86.7
L1023	100

Measuring point for surface luminance & luminance variation



A : H / 4 mm
B : V / 4 mm
@ H,V : Active Area

FIG. 10 5 Points for Luminance Measure

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".

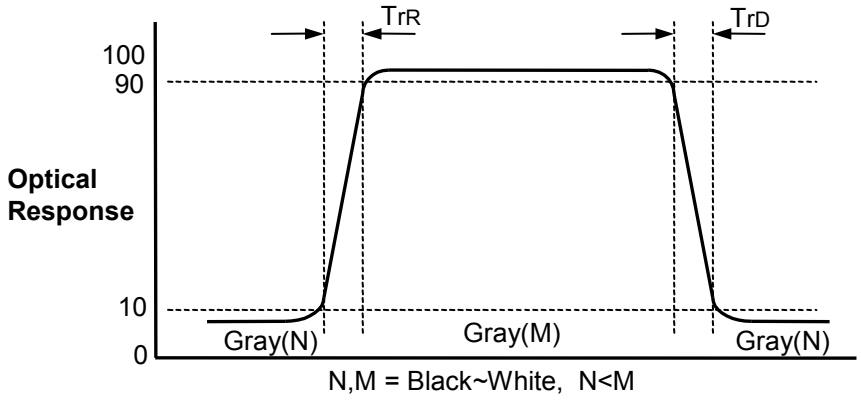


FIG. 11 Response Time

Dimension of viewing angle range

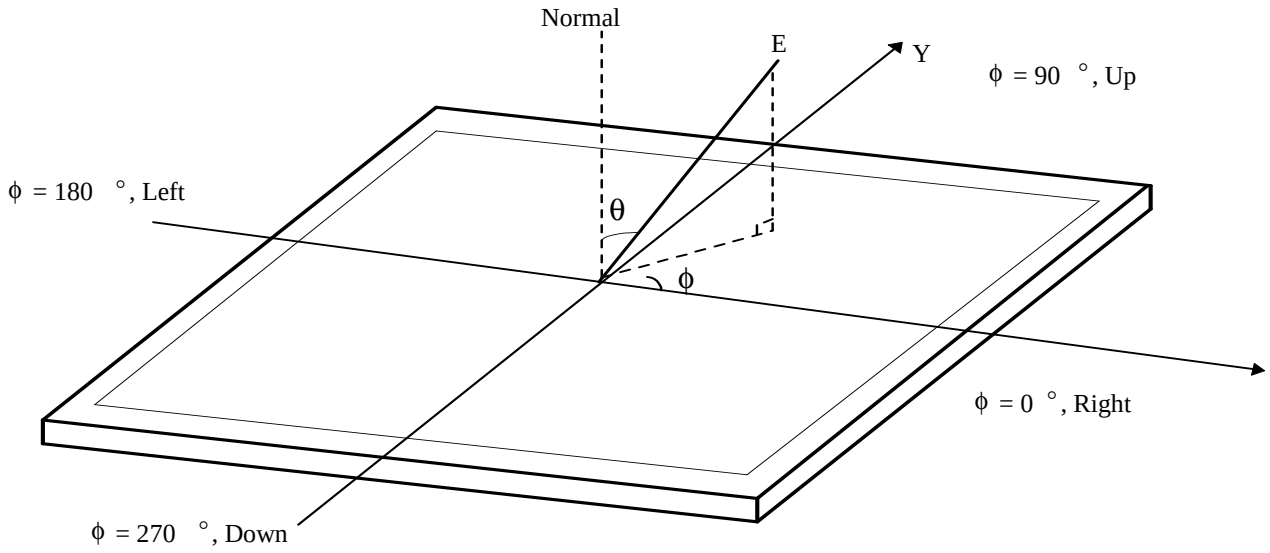


FIG.12 Viewing Angle

5. Mechanical Characteristics

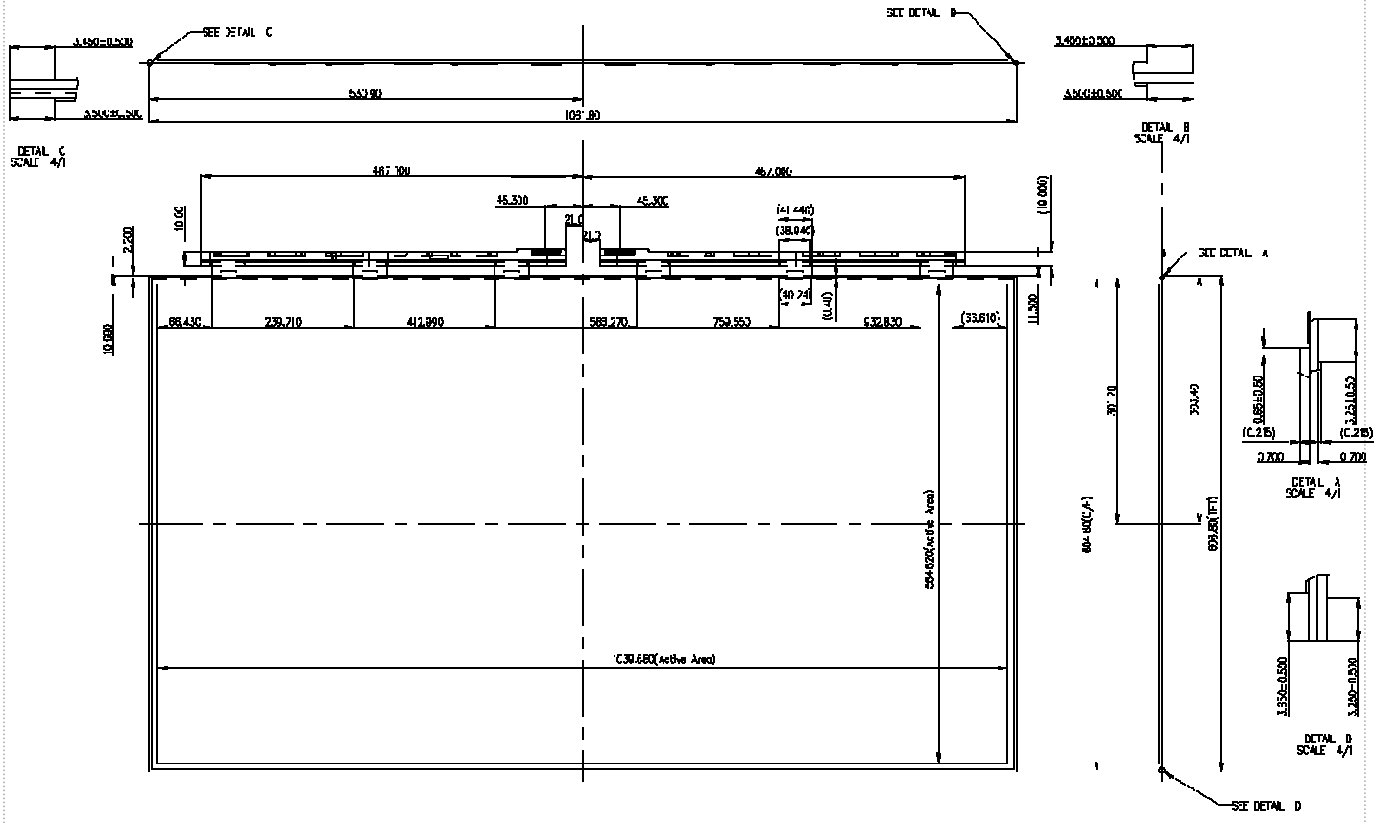
Table 8 provides general mechanical characteristics.

Table 8. MECHANICAL CHARACTERISTICS

Item	Value	
Outline Dimension (Only Glass)	Horizontal	1061.8 mm
	Vertical	606.8 mm
	Thickness	1.75 mm
Active Display Area	Horizontal	1039.68 mm
	Vertical	584.82 mm
Weight	2.6kg(typ), 2.9Kg(Max)	
Surface Treatment	Hard coating(3H) Anti-glare treatment of the front polarizer(<1%)	

Note : Please refer to a mechanic drawing in terms of tolerance at the next page.

[FRONT VIEW]


SEE DETAIL C
SEE DETAIL B
DETAIL C
SCALE 4/1
DETAIL B
SCALE 4/1
SEE DETAIL A
DETAIL A
SCALE 4/1
DETAIL D
SCALE 4/1
SEE DETAIL D
(Active Area)
(Active Area)

6. Reliability

Table 9. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Humidity condition Operation	Ta= 40 °C ,90%RH
6	Altitude operating storage / shipment	0 - 15,000 ft 0 - 40,000 ft

Note : Before and after Reliability test, Board ass'y should be operated with normal function.

7. International Standards

7-1. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

8. Packing

8-1. Packing Form

a) Package quantity in one Pallet : 70 pcs

b) Pallet Size :1250 mm(L) X 800 mm(W) X 1088 mm(H)

9. Precautions

Please pay attention to the followings when you use this TFT LCD panel.

9-1. Assembly Precautions

(1) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(2) You should adopt radiation structure to satisfy the temperature specification.
(3) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(4) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(5) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer
(6) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(7) Board ass'y should be put on the mold frame properly.
(8) FFC Cable should be connected between System board and Source PCB correctly.
(9) Mechanical structure for backlight system should be designed for sustaining board ass'y safely.

9-2. Operating Precautions

(1) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(2) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer
(3) Be careful for condensation at sudden temperature change.Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(6) Please do not give any mechanical and/or electrical impact to board assy. Otherwise, it can't be operated its full characteristics perfectly.

9-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly. Panel ground path should be connected to metal ground.

9-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-5. Storage

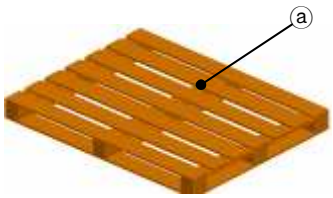
When storing the board ass'y as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the board ass'y to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

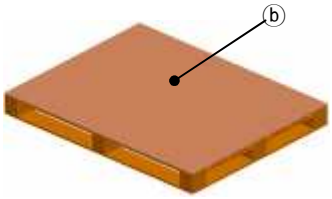
APPENDIX-I

■ Pallet Ass'y

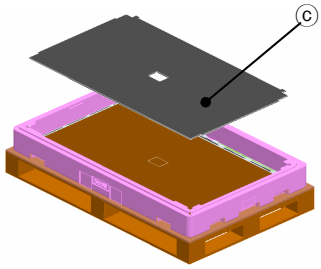
①



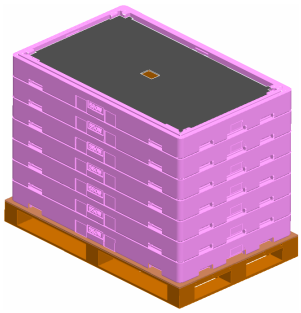
②



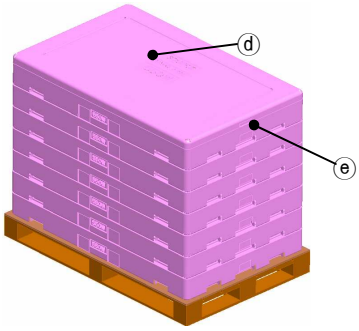
③



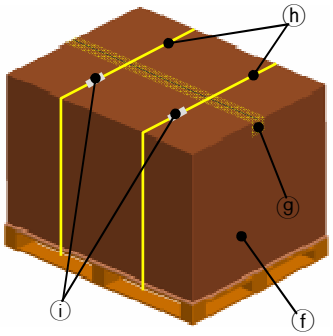
④



⑤



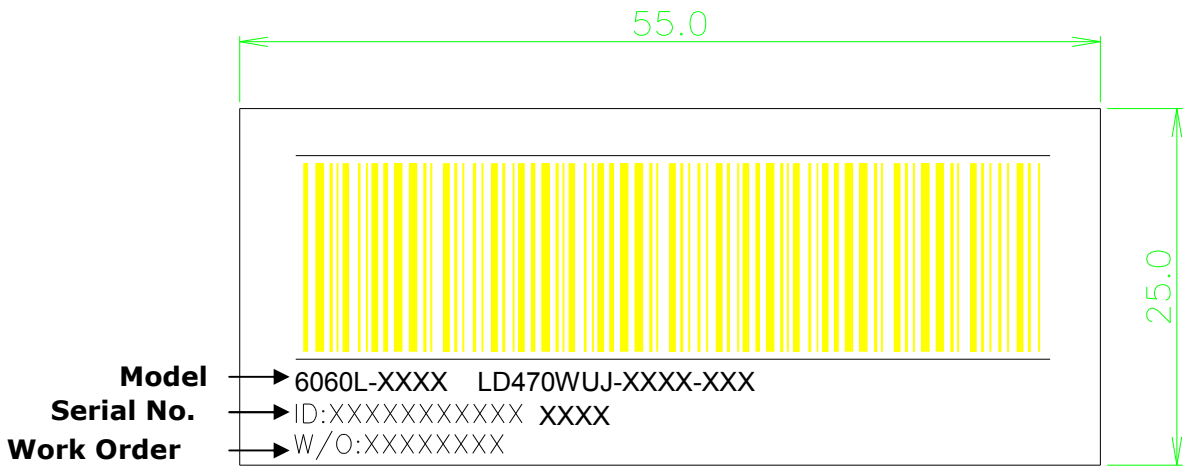
⑥



No.	Description	Material
ⓐ	Pallet	Plywood
ⓑ	SHEET	Single Wall
ⓒ	PE Sheet	PE
ⓓ	Top Packing	EPP
ⓔ	Bottom Packing	EPP
ⓕ	Angle Packing	Single Wall
ⓖ	Tape	OPP
ⓗ	Band	PP
ⓘ	Clip	Steel

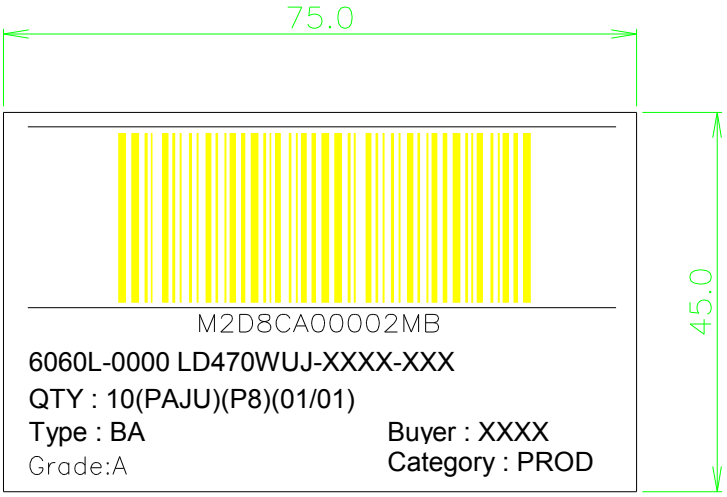
 # APPENDIX- II-1

■ Board Ass'y ID Label

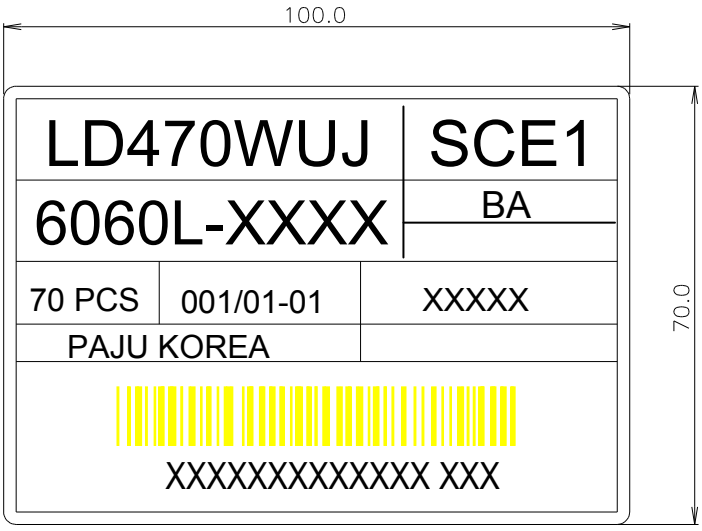


 # APPENDIX- II-2

■ BOX Label

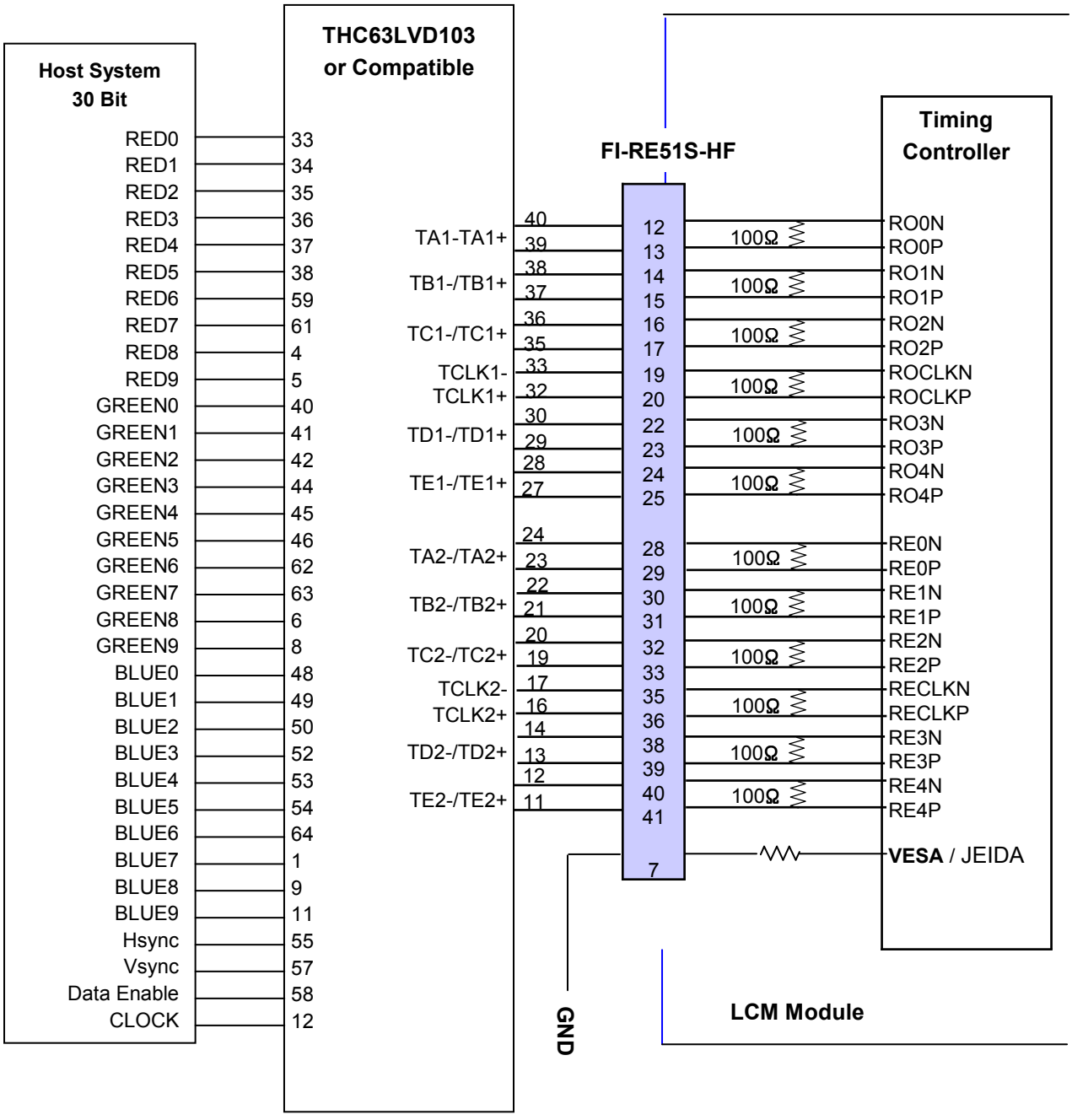


■ Pallet Label



APPENDIX-I-1

■ Required signal assignment for Flat Link (Thine : THC63LVD103) Transmitter(Pin7="L or NC")



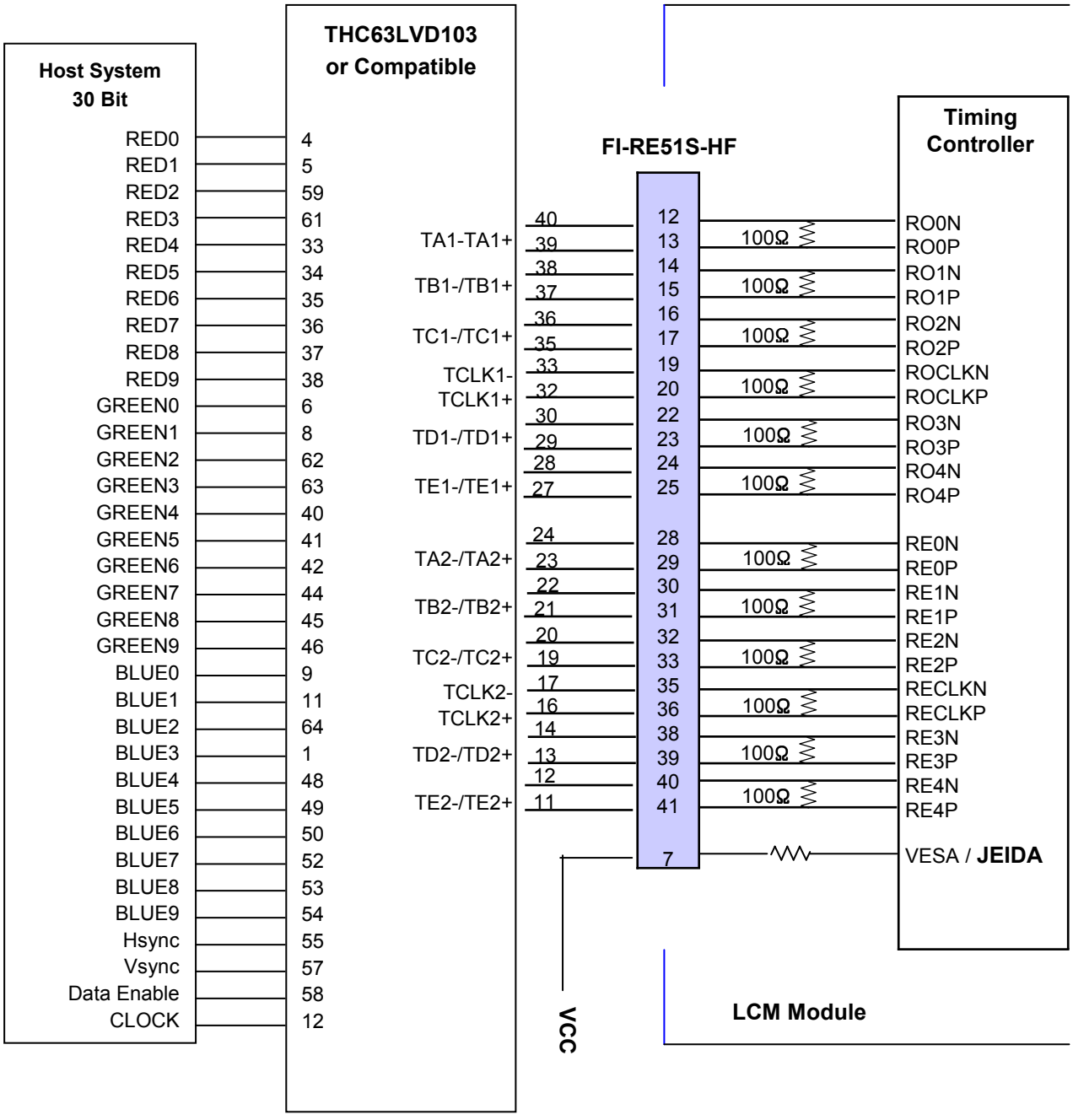
Note: 1. The LCD module uses a 100 Ohm[Ω] resistor between positive and negative lines of each receiver input.

2. Refer to LVDS Transmitter Data Sheet for detail descriptions. (THC63LVD103 or Compatible)

3. '9' means MSB and '0' means LSB at R,G,B pixel data.

APPENDIX-I-2

■ Required signal assignment for Flat Link (Thine : THC63LVD103) Transmitter(Pin7="H")



Note :1. The LCD module uses a 100 Ohm[Ω] resistor between positive and negative lines of each receiver input.

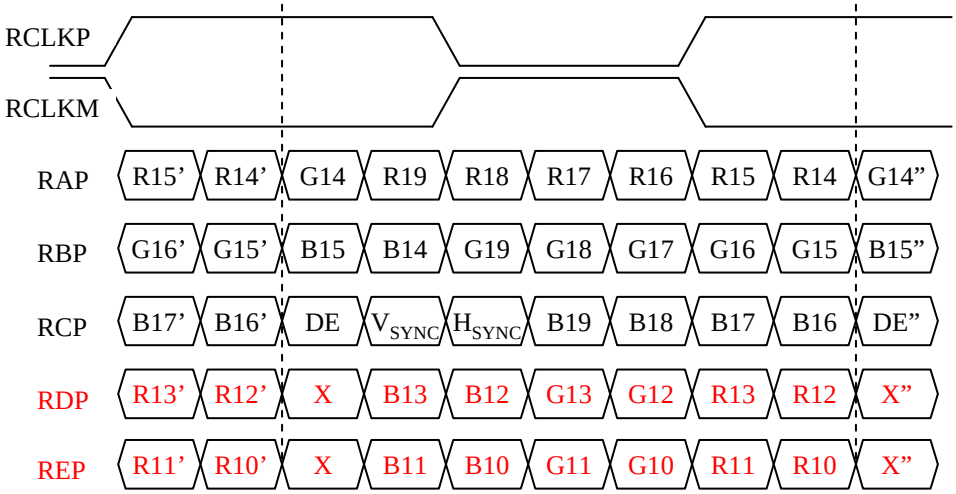
2. Refer to LVDS Transmitter Data Sheet for detail descriptions. (THC63LVD103 or Compatible)

3. '9' means MSB and '0' means LSB at R,G,B pixel data.

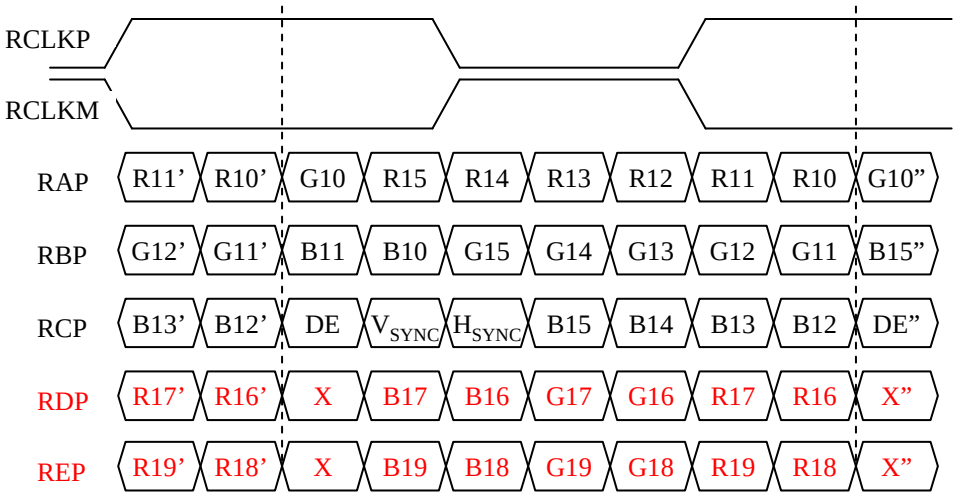
 # APPENDIX- II-1

LVDS Data-Mapping info. (10bit)

■ LVDS Select : “H” Data-Mapping (JEIDA format)



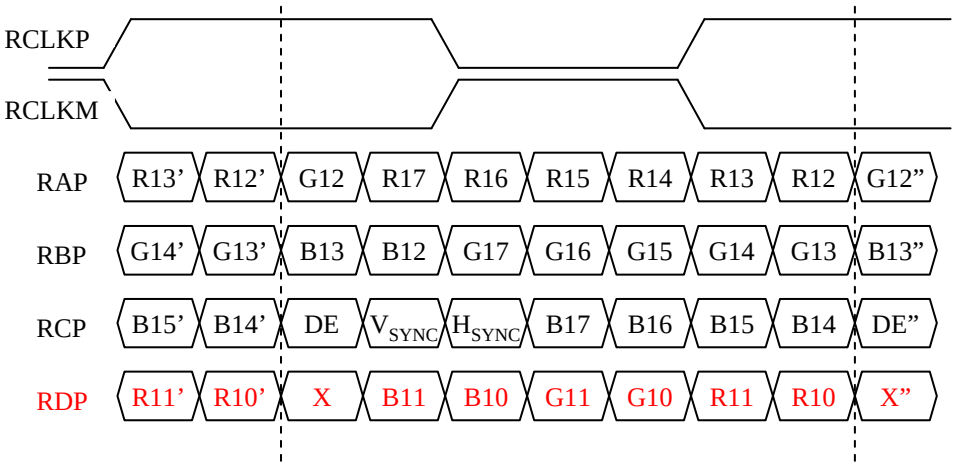
■ LVDS Select : “L” Data-Mapping (VESA format)



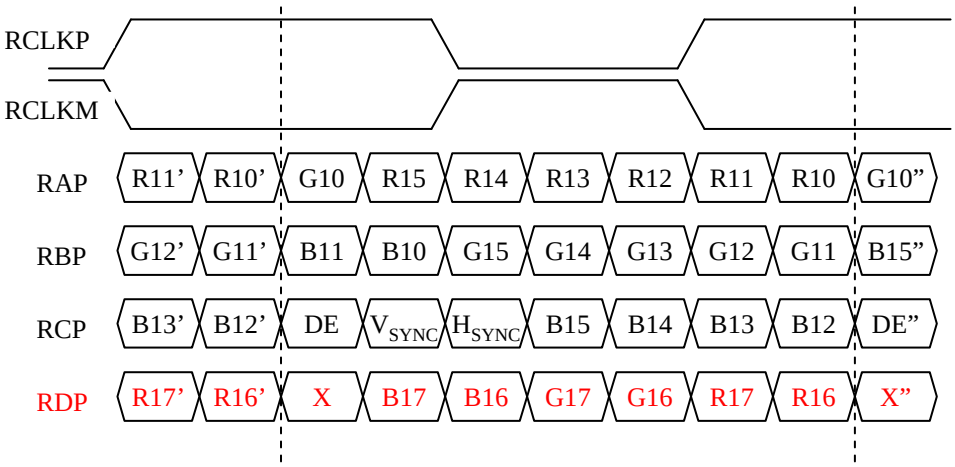
 # APPENDIX- II-2

LVDS Data-Mapping info. (8bit)

■ LVDS Select : “H” Data-Mapping (JEIDA format)



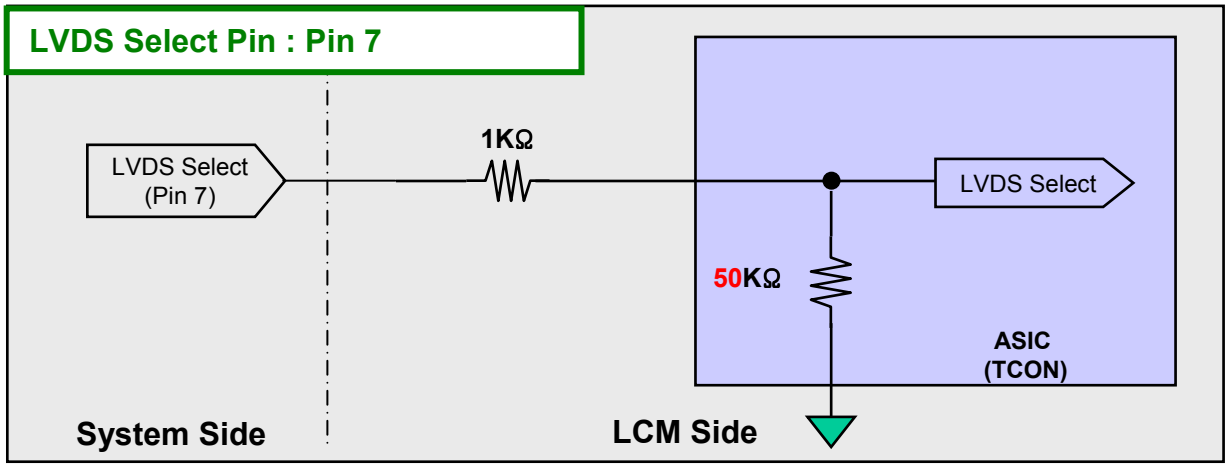
■ LVDS Select : “L” Data-Mapping (VESA format)



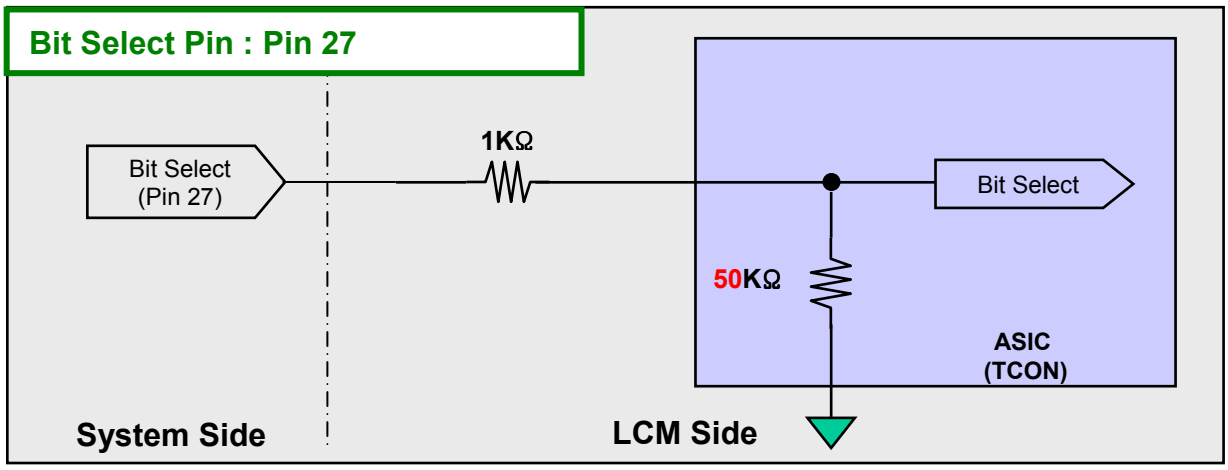
APPENDIX- VI

■ Option Pin Circuit Block Diagram

1) Circuit Block Diagram of **LVDS Format** Selection pin



2) Circuit Block Diagram of **Bit Format** Selection pin



3) Circuit Block Diagram of **AGP Option** Selection pin