Primary-Side Quasi-Resonant Controller, Operating in CV/CC Mode

REV. 00

General Description

The LD5516C is a primary-side Quasi-Resonant feedback controller capable to operate in CV/CC mode for small power AC/DC charger and adapter, a superior solution for Pump Express Plus™ based application. It minimizes the components counts and is available in a tiny SOT-26 package. Those make it an ideal design for low cost and high performance applications.

The LD5516C provides fixed constant current operation to boost more power. Both of them are programmable constant voltage, requiring neither photo-coupler nor secondary-side control circuit. Also, the LD5516C feature feedback loop open protection, internal OTP (Over Temperature Protection), wide-range and different output voltage level OVP (Over Voltage Protection)… etc., to prevent the circuit from being damaged under abnormal conditions.

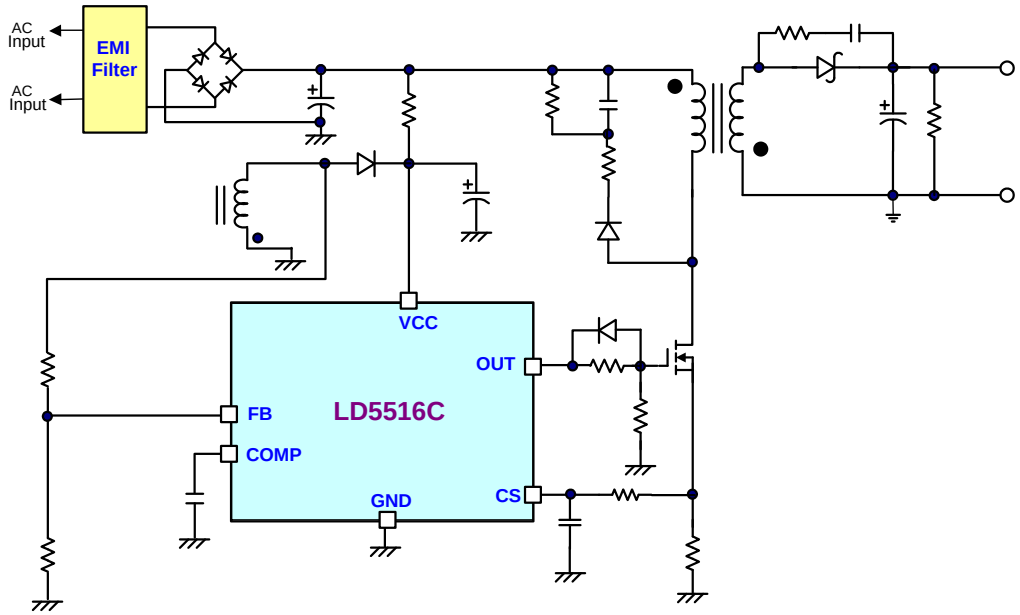
Features

- Speedy Charge™ technology
- Pump Express Plus™ protocol compatible
- Normally 5V output
- Programmable output voltage
- 9V, 7V, and 5V to 3.6V in 0.2V step
- Meet CoC Tier-2 no load power saving for 75mW
- Adjustable constant current control
- Adjustable load regulation compensation
- Ultra low Startup current
- 75kHz maximum switching frequency
- LEB (Leading-Edge Blanking) on CS Pin
- Up to 29V OVP (Over Voltage Protection) on VCC
- 120mA/-200mA unbalanced MOS driving capability

Applications

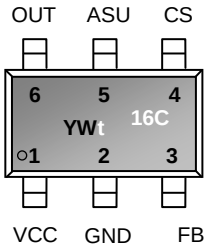
- Pump Express Plus™ based Charger
- AC/DC Adaptor for Phone and Tablet

Typical Application



Pin Configuration

SOT-26 (TOP VIEW)
LD5516C



Ordering Information

Part number	Package	Top Mark	Shipping
LD5516C GL	SOT-26	YWt/16C	3000 /tape & reel

The LD5516C is ROHS compliant.

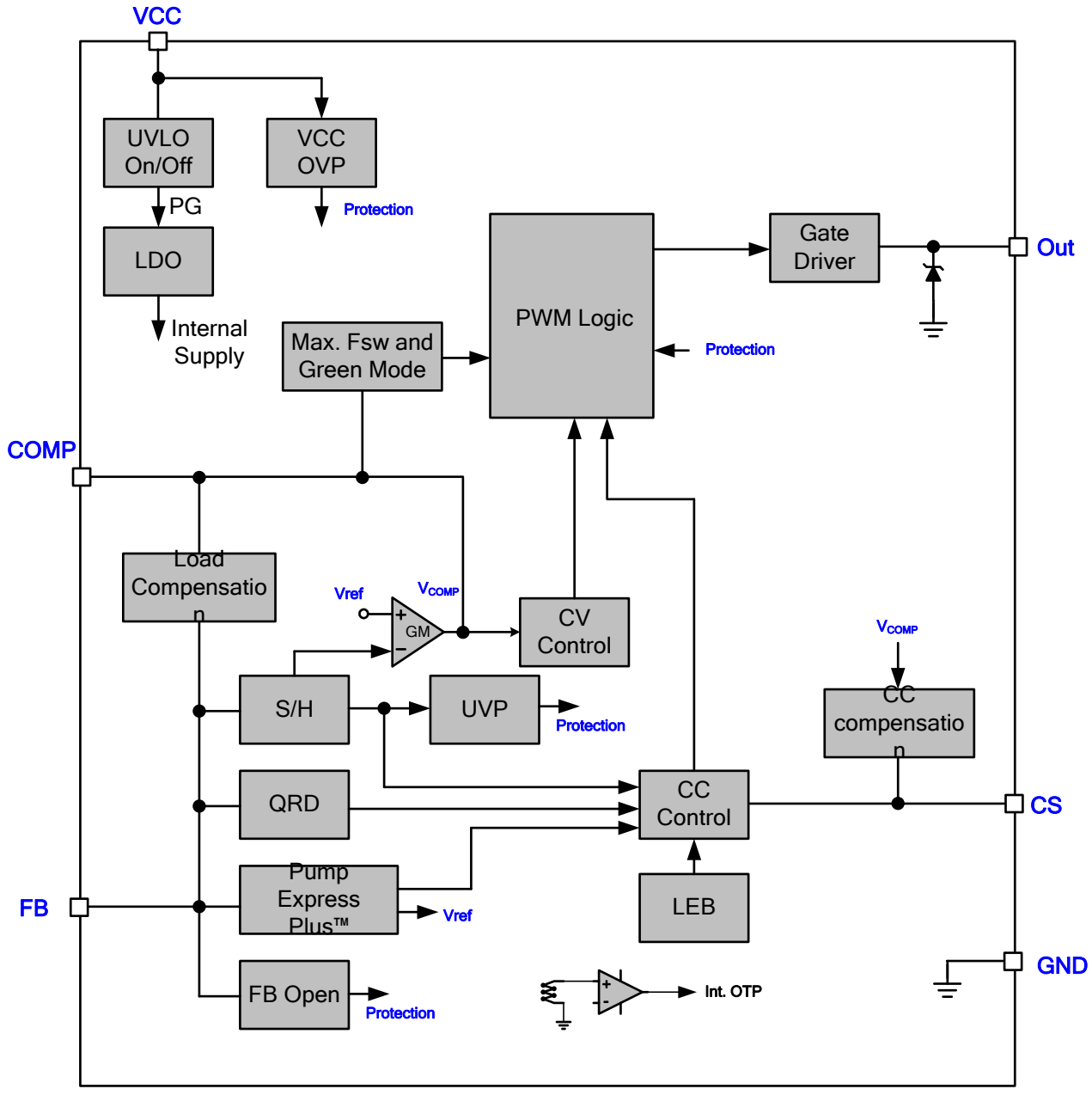
Protection Mode

Part number	VCC_OVP	FB_UVP	OTP(Internal)
LD5516C	Auto-Restart	Auto-Restart	Auto-Restart

Pin Descriptions

PIN	NAME	FUNCTION
1	VCC	Supply voltage pin
2	GND	Ground
3	FB	Voltage Feedback Sense pin. It detects the output voltage information from auxiliary winding
4	CS	Current sense pin, connect it to sense the MOSFET current
5	COMP	Output of the error amplifier for voltage compensation
6	OUT	Gate drive output to drive the external MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC,	-0.3V ~ 40V
OUT	-0.3V ~ 40V
COMP, FB	-0.3V ~ 4.0V
CS	-0.3V ~ 4.0V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	200°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 60°C)	200mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5kV
ESD Voltage Protection, Machine Model	250V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
VCC Capacitor	4.7	10	μF
Start-up resistor Value (AC Side, Half Wave)	1M	6.6M	Ω
COMP Pin Capacitor	470	4700	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF ~ 0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=12.0V)

PARAMETER	CONDITIONS	Symbol	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current	VCC=UVLO(ON) - 50mV	I_{CC_ST}	0.13	1	1.5	μA
Operating Current	V_{COMP}=0V, OUT=open, FB=2V	I_{CC_OP2}	0.55	0.65	0.75	mA
	OVP/FB UVP tripped, FB=0V	I_{CC_OPA}	0.35	0.5	0.65	mA
UVLO(OFF)		V_{CC_OFF}	5.5	6.0	6.5	V
UVLO(ON)		V_{CC_ON}	14	15	16	V
VCC OVP Level		V_{CC_OVP}	27	29	31	V
Error Amplifier (COMP Pin)						
Reference Voltage, V_{REF}	For 5V output	V_{REF_5V}	0.98	1.00	1.02	V
	For 7V output*	V_{RED_7V}		1.37		V
	For 9V output	V_{REF_9V}	1.65	1.73	1.78	V
Load Compensation Current	V_{COMP}=2.5V	I_{Load_Comp}	16	20	24	μA
Current Sensing (CS Pin)						
Maximum Input Voltage, V_{CS-OFF}		V_{CS_MAX}	0.74	0.8	0.85	V
Minimum V_{CS-OFF}	V_{COMP} < 0.45V	V_{CS_MIN}	0.07	0.1	0.13	V
Leading Edge Blanking Time		T_{LEB}	310	430	550	ns
QRD (Quasi Resonant Detection, FB Pin)						
QRD Trip Level	*	V_{QRD}		150		mV
	Hysteresis*	V_{QRD_HYS}		50		mV
Oscillator for Switching Frequency						
Maximum Frequency		F_{SW_MAX}	65	75	85	kHz
Green Mode Frequency	*	F_{SW_GREEN}		25		kHz
Minimum Frequency		F_{SW_MIN}	0.5	0.7	0.89	kHz
Output Drive (OUT Pin)						
Maximum On Time		T_{ON_MAX}	18	27	40	μs
FB Under Voltage Protection (UVP, FB Pin)						
Under Voltage Level		V_{FB_UVP}	0.5	0.55	0.65	V
UVP Delay Time	After start up*	T_{D_FBUVP}		20		ms
On Chip OTP (Over Temperature)						
OTP Level	*	T_{INOTP}		140		°C
OTP Hysteresis	*	T_{INOTP_HYS}		15		°C

*: Guaranteed by design

Typical Performance Characteristics

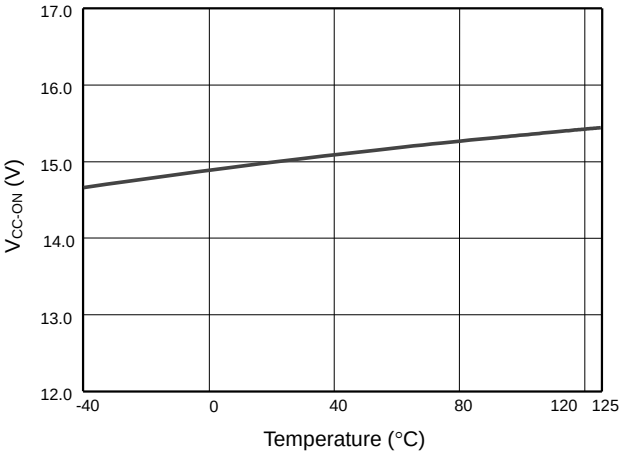


Fig. 1 UVLO (on) vs. Temperature

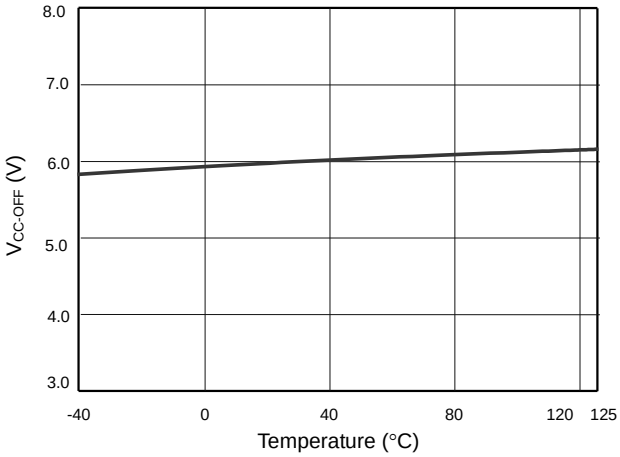


Fig. 2 UVLO (off) vs. Temperature

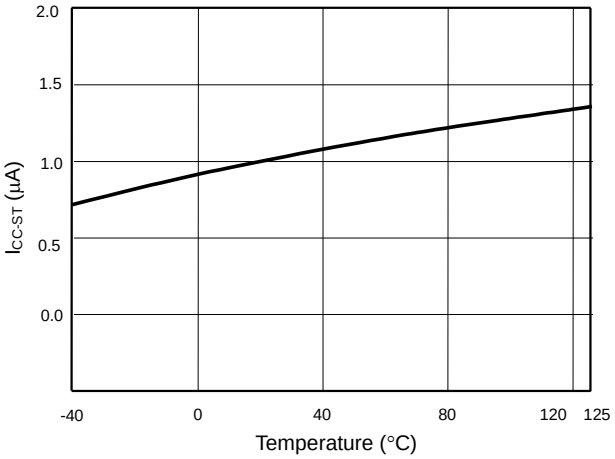


Fig. 3 Startup Current vs. Temperature

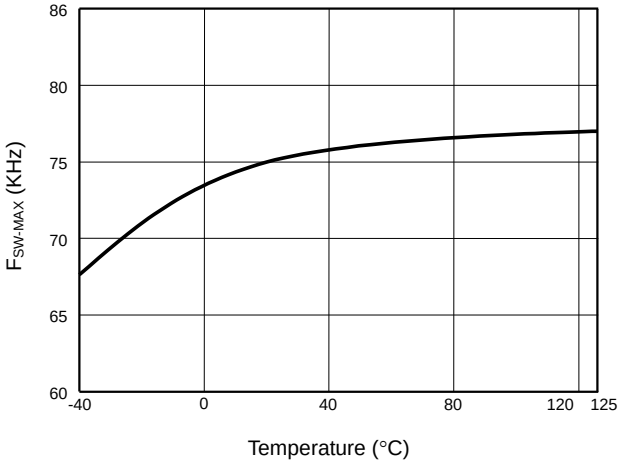


Fig. 4 Max Frequency vs. Temperature

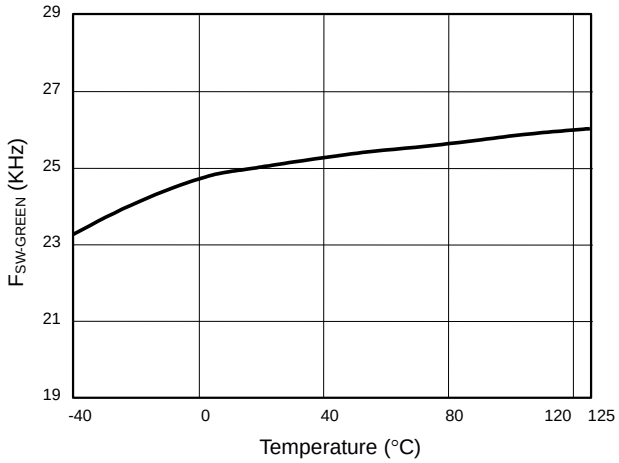


Fig. 5 Green Mode Frequency vs. Temperature

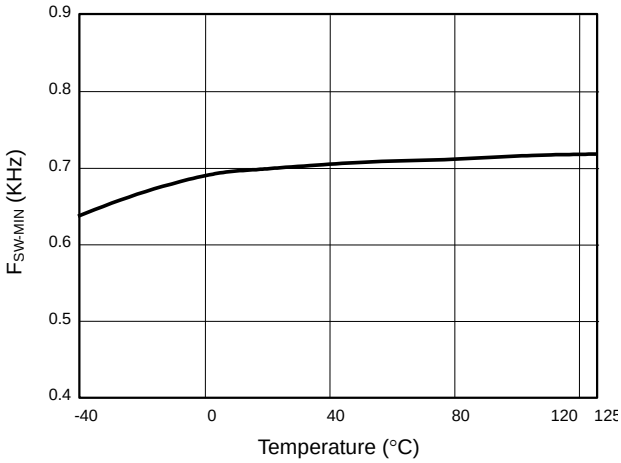


Fig. 6 Min Frequency vs. Temperature

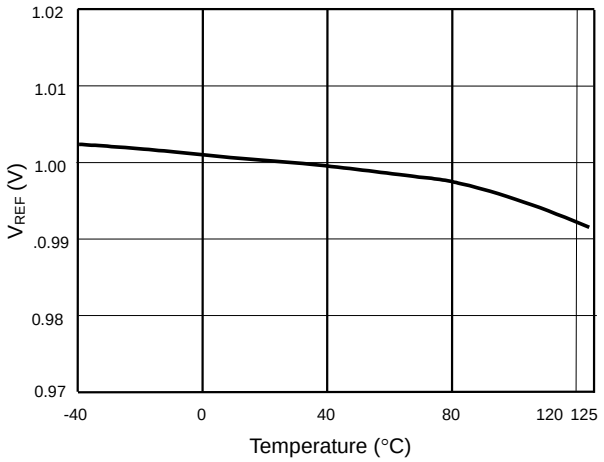


Fig. 7 Reference Voltage vs. Temperature

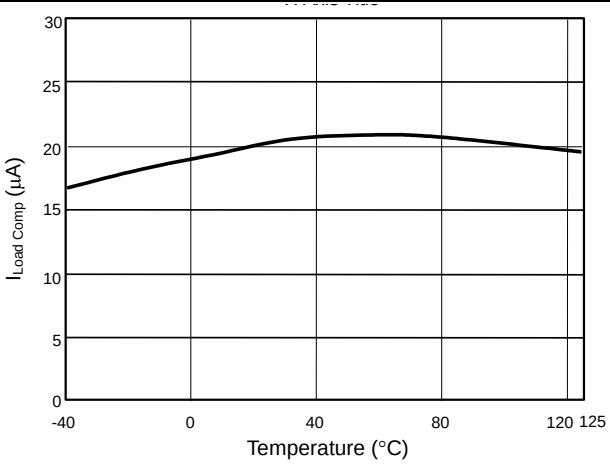


Fig. 8 Load Compensation vs. Temperature

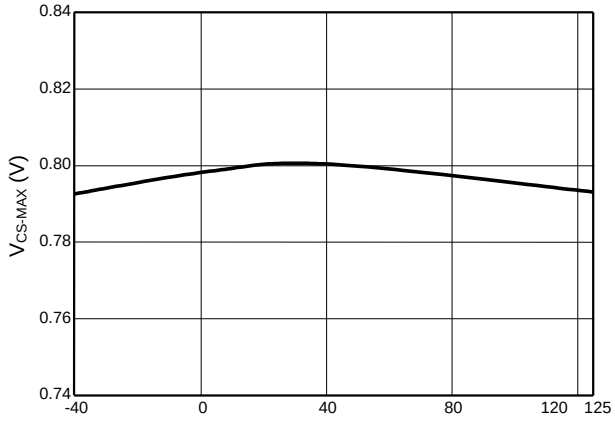


Fig. 9 V_{CS} (off) vs. Temperature

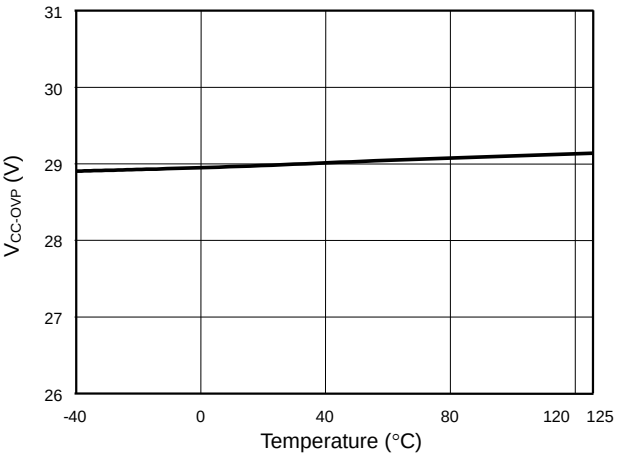


Fig. 10 VCC OVP vs. Temperature

Application Information

Operation Overview

The LD5516C is an excellent primary side feedback controller with Quasi-Resonant operation to provide high efficiency and better EMI performance. The LD5516C remove the need for secondary feedback circuits while achieving excellent line and load regulation. They meet the Green Power requirement and are intended for the use in those modern switching power suppliers and linear adaptors that demand higher power efficiency and power-saving. They integrate with more functions to reduce the external components counts and the size. Their major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage across VCC pin. It would assure the supply voltage enough to turn on the LD5516C PWM controllers and further to drive the power MOS. As shown in Fig. 11, a hysteresis is built in to prevent shutdown from voltage dip during startup.

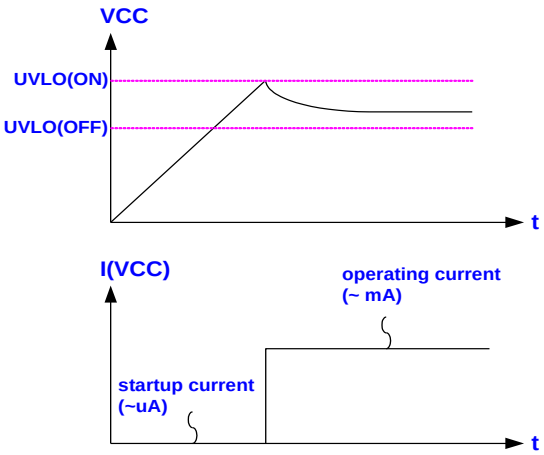


Fig. 11

Startup Current and Startup Circuit

The typical startup circuit to generate VCC of the LD5516C is shown in Fig. 12. During startup transient, the VCC sinks below the UVLO threshold, so there's no pulse delivering out from the LD5516C to drive the power MOS. Therefore, the current through R1 will be used to charge the capacitor C1. Until the VCC is fully charged to enable the LD5516C and to deliver the drive-out signal, the auxiliary winding will provide the supply current instead. If PWM controller requires less current to start up, it will allow less power consumption on R1. By using CMOS process and some unique circuit design, the LD5516C requires only 1.5μA max to start up. Higher resistance of R1 will spend much more time to start up. The user is recommended to select proper value of R1 and C1 to optimize the power consumption and startup time.

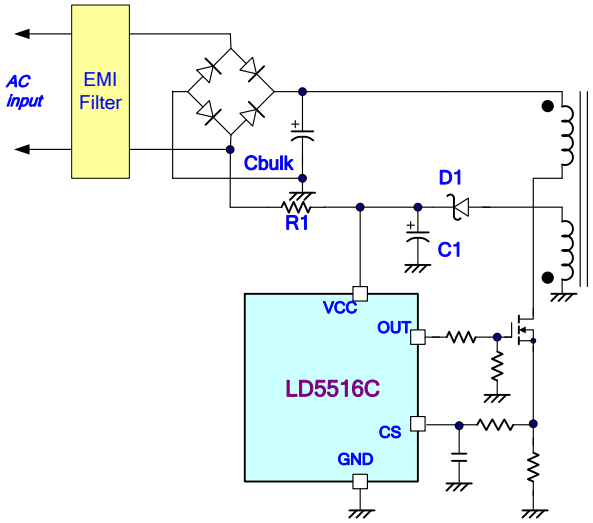


Fig. 12

Principle of CV Operation

In the DCM Flyback converter, it senses the output voltage by auxiliary winding. LD5516C samples the auxiliary winding on the primary-side to regulate the output voltage, as shown in the Fig. 13. The voltage induced in the auxiliary winding is a reflection of the secondary winding voltage while the power MOS is in off state. Via a resistor divider connected between the auxiliary winding and FB pin, the auxiliary voltage is sampled after a sample delay time and will be hold until the next sampling. The sampled voltage is compared with internal reference V_{REF} and the error will be amplified. The error amplifier output COMP reflects the load condition and controls the duty cycle to regulate the output voltage,

thus constant output voltage can be achieved. The output voltage is given as:

$$V_{OUT} = 1.0V(1+\frac{Ra}{Rb})(\frac{Ns}{Na}) - V_F$$

Where V_F indicates the drop voltage of the output Diode, Ra and Rb are top and bottom feedback resistor value, Ns and Na are the turns of transformer secondary and auxiliary.

In case that the output voltage is sensed through the auxiliary winding; the leakage inductance will induce ringing to affect output regulation. To optimize the collector voltage clamp circuit will minimize the high frequency ringing and achieve the best regulation. Fig. 14 shows the desired collector voltage waveform in compare to those with large undershoot due to leakage inductance induced ring (Fig. 15). This will make the sample error and cause poor performance for output voltage regulation. A proper selection for resistor RS, in series with the RC filter, may reduce any large undershoot.

LD5516C supported Pump Express Plus™ fast charge agreement, the MCU can send current pattern to increase the charger output voltage, as shown in the Fig. 16. This method can achieve the effect of fast charging time.

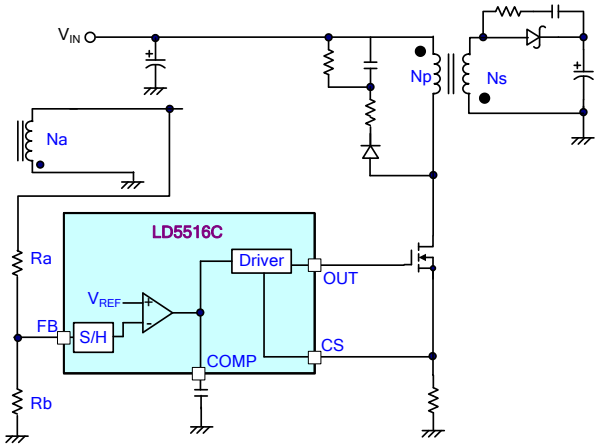


Fig. 13

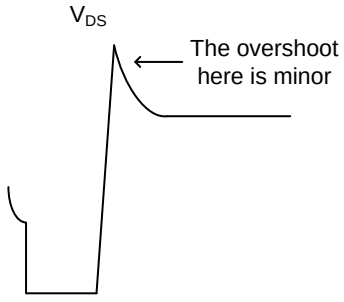


Fig.14

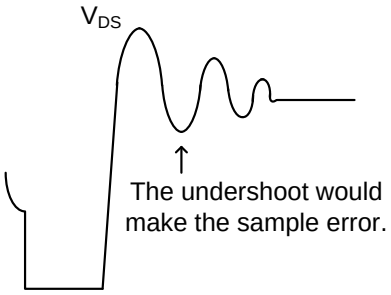


Fig.15

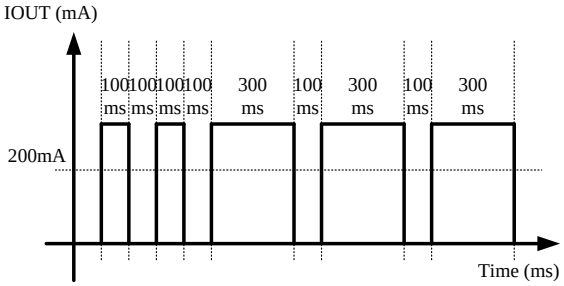


Fig.16

Load Regulation Compensation

The LD5516C is implemented with load regulation compensation to compensate the cable voltage droop and achieve a better voltage regulation. The offset voltage is created across FB by an internal sink current source which feeds out the FB during the sampling period. The internal sink current source is proportional to the value of V_{COMP}, as shown in Fig. 17. As a result, the drop due to the cable loss can be compensated. So that, the offset voltage decreases as the V_{COMP} decrease in condition from full-load to no-load. It can also be programmed by adjusting the resistance of the divider to compensate the drop for various cable lines used. The equation of internal sink current source is shown as below.

$$I_{FB} = (V_{COMP} - 0.45) * 9.75 \ (\mu A)$$

The percentage of maximum compensation is shown as below.

$$\frac{\Delta V}{Vo} = \frac{I_{FB} \times (Ra // Rb)}{2} \times 100\%$$

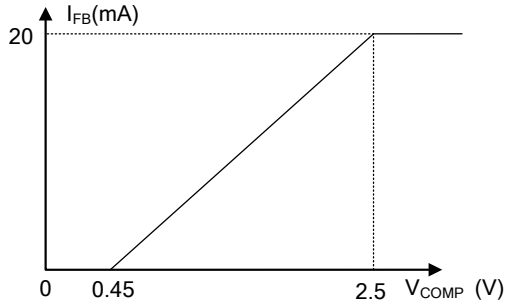


Fig. 17

Quasi-Resonant Mode Detection

The LD5516C employs quasi-resonant (QR) switching scheme to switch valley-mode either in CV or CC operation. This property feature greatly reduces the switching loss and dv/dt in the entire operating range for the power supply. The QR detection block will detect auxiliary winding signal to drive power MOS as FB pin voltage drops to 0.15V. The QR comparator would not operate if FB pin voltage remains above 0.2V. The 4ms of time-out-2 generates a power MOS turn-on signal as the driver output drops to low level for more than 4ms with the falling edge of the driver output.

Multi-Mode Operation

The LD5516C is a QR controller operating in multi-modes. The controller changes operation modes according to line voltage and load conditions. At heavy-load (V_{COMP}>1.6V, Fig. 18), there might be two situations to meet. If the system AC input is in low line, the LD5516C will turn on in first valley. If in high line, the switching frequency will increase till over the clamp of 75kHZ and skip the first valley to turn on in 2nd valley. The switching frequency would vary depending on the line voltage and the load conditions when the system is operated in QR mode.

At medium or light load conditions, the frequency clamp is reduced to 25 kHz maximum as V_{COMP} down to V_{SG1}. However, the valley switching characteristic behaves as well in these conditions. The LD5516C will jump to turn on in 3rd, 4th…. Valley. That is, when load decreases, the system automatically skip more valleys and the switching frequency is thus reduced. In such way, a smooth frequency fold back is realized and high power efficiency is achieved.

At zero load or very light load conditions (V_{COMP}<0.3V), the system operates in green mode for power saving. In green mode, the system modulates the frequency according to the load and V_{COMP} conditions. Once V_{COMP} is lower than V_{SG2}, the switching frequency starts to linearly decrease from 25 kHz to 0.7 kHz.

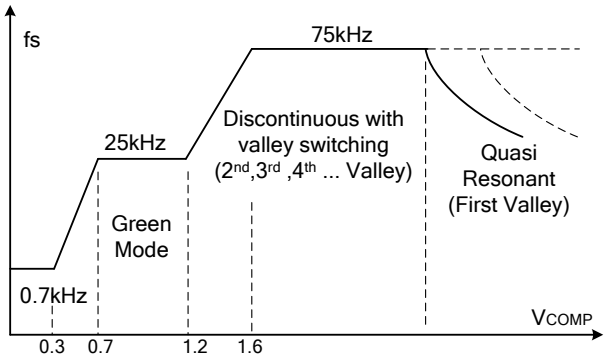


Fig. 18

Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 19, the LD5516C detects the primary power MOS current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.8V. From above, the power MOS peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.8V}{R_S}$$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current

spike. The LD5516C can deliver more constant current at high input voltage than at low input voltage. To compensate this, an offset voltage is added to the RS signal by an internal current source (I_{CC}) and an external resistor (R_1) in series between the sense resistor (Rs) and the CS pin, By selecting a proper value of the resistor in series with the CS pin, the amount of compensation can be adjusted. The value of I_{CC} (300 μA) depends on the COMP voltage(V_{COMP}>1.2V). The equation of I_{CC} (300 μA) is decreased as:

$$V_{CS} = V_S + (300\mu A \times R_1)$$

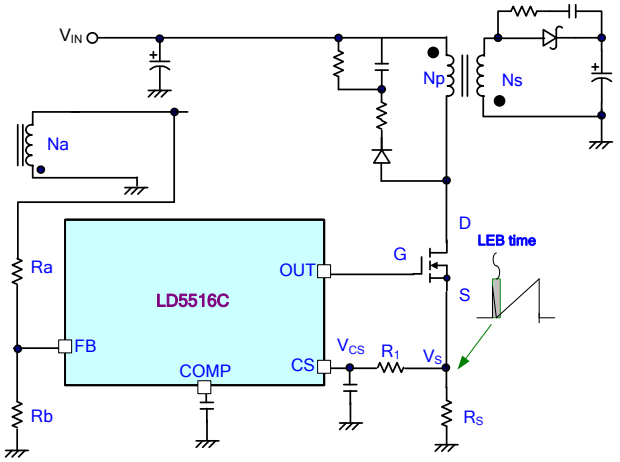


Fig. 19

Principle of CC Operation

The primary side control scheme is applied to eliminate secondary feedback circuit or opto-coupler, which will reduce the system cost. The switching waveforms are shown in Fig. 20. The output current Io can be expressed as:

$$Io = \frac{1}{2}\frac{i_{S,PK} \times T_{DIS}}{T_S} = \frac{1}{2}\frac{N_P}{N_S} \times i_{P,PK} \times \frac{T_{DIS}}{Ts} = \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS}}{R_S} \times \frac{T_{DIS}}{T_S}$$

The primary peak current $i_{P,PK}$, inductor current discharge time (T_{DIS}) and switching period (T_S) can be detected by the IC. The ratio of $V_{CS}*T_{DIS}/T_S$ will be modulated as a constant ($V_{CS}*T_{DIS}/T_S$ =1/3). I_O can be induced finally by

$$Io \cong \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS}}{R_S} \times \frac{T_{DIS}}{T_S} \cong \frac{1}{2}\frac{N_P}{N_S} \times \frac{1}{R_S} \times \frac{1}{3}$$

However this is an approximate equation. The user may fine-tune it according to the experiment result.

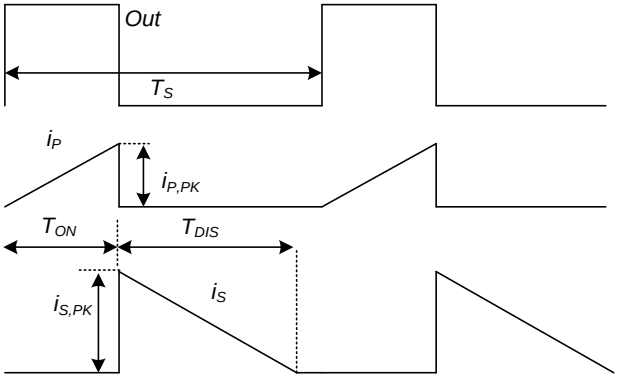


Fig. 20

OVP (Over Voltage Protection) on VCC – Auto Recovery

The LD5516C are implemented with OVP function over VCC. As the VCC voltage rises over the OVP threshold voltage, the output drive circuit will be shutdown simultaneously thus to stop the switching of the power MOS until the next UVLO(ON) arrives. The VCC OVP function of LD5516C are an auto-recovery type protection. The Fig. 21 shows its operation. On the other hand, if the OVP condition is removed, the Vcc level will get back to normal level and the output will automatically return to the normal operation.

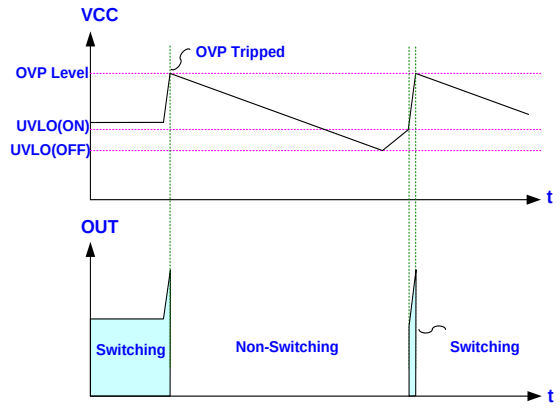


Fig. 21

FB Under Voltage Protection (FB UVP) – Auto Recovery

The LD5516C is implemented with an UVP function over FB pin. If the FB voltage falls below 0.55V for over the delay time of FB UVP, the protection will be activated to stop the switching of the power MOS until the next UVLO(ON) arrives. The FB UVP function in the LD5516C is an auto-recovery type protection. The Fig. 22 shows its operation. The FB UVP is disabled during the soft start.

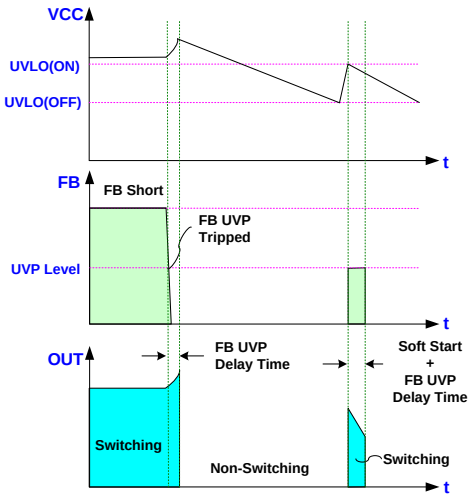
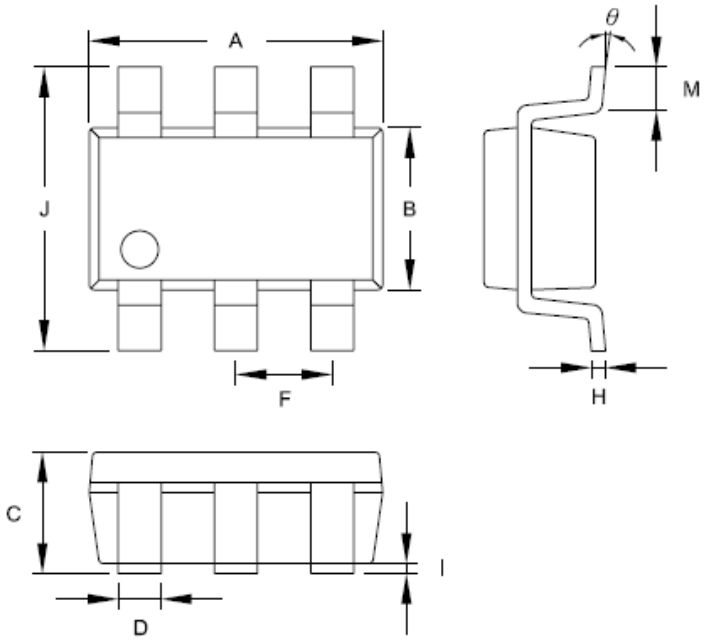


Fig. 22

Package Information

SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	--------	1.450	--------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP.		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	08/10/2016	Original Specification