# Quasi-Resonant PWM Controller with Frequency Swapping and Integrated Protections

***REV: 00***

## General Description

The LD5520 is built with several functions, protection and EMI-improved solution in a tiny package. It takes less components counts or circuit space, especially ideal for those total solutions of low cost.

The implemented functions include low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. It also features more protections like OLP (Over Load Protection), FB pin OVP (FB pin Over Voltage Protection) and OVP (Over Voltage Protection) to prevent circuit damage occurred under abnormal conditions.

Furthermore, the adjustable frequency swapping function is to reduce the noise level and thus helps the power circuit designers to easily deal with the EMI filter design by spending minimum amount of component cost and developing time.

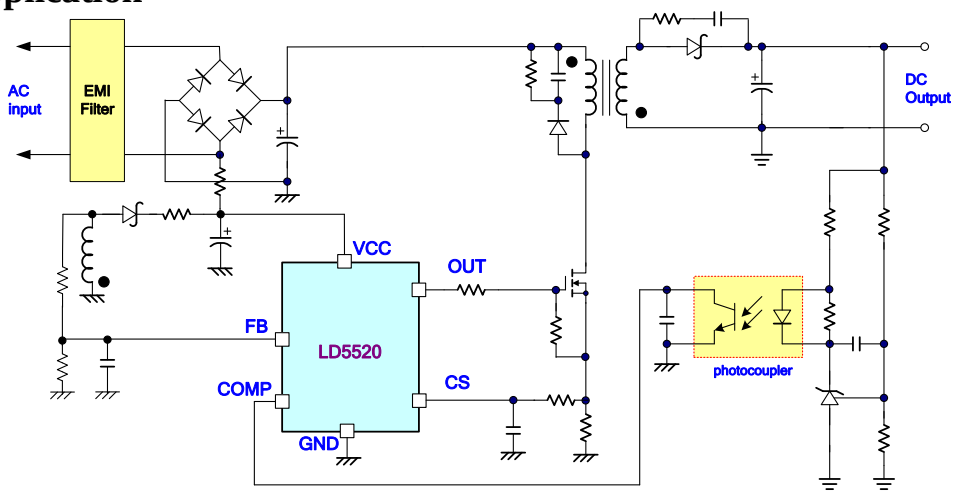
## Features

- Secondary -side Feedback Control with quasi-resonant Operation
- Built-in Load Regulation Compensation
- Low Startup Current (<12μA)
- 0.5mA Ultra-low Operating Current at Light Load
- 130kHz Maximum Switching Frequency.
- Current Mode Control with Cycle-by-Cycle Current Limit
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- VCC OVP (Over Voltage Protection)
- Adjustable OVP (Over Voltage Protection) on FB pin.
- Adjustable Frequency Swapping Range on FB pin.
- OLP (Over Load Protection)
- Internal OTP (Over Temperature Protection)
- Gate Source/Sink Capability: 100mA/-150mA

## Applications

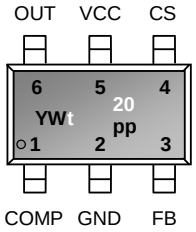
- Switching AC/DC Adaptor and Battery Charger

## Typical Application



## Pin Configuration

SOT-26 (TOP VIEW)




YY, Y : Year code (D: 2004, E: 2005…..)
WW, W : Week code
PP : Production code
t20 : LD5520

## Ordering Information

| Part number | Package | Top Mark | Shipping |
|---|---|---|---|
| LD5520 GL | SOT-26 | YWt/20 | 3000 /tape & reel |

The LD5520 is ROHS compliant/ Green packaged

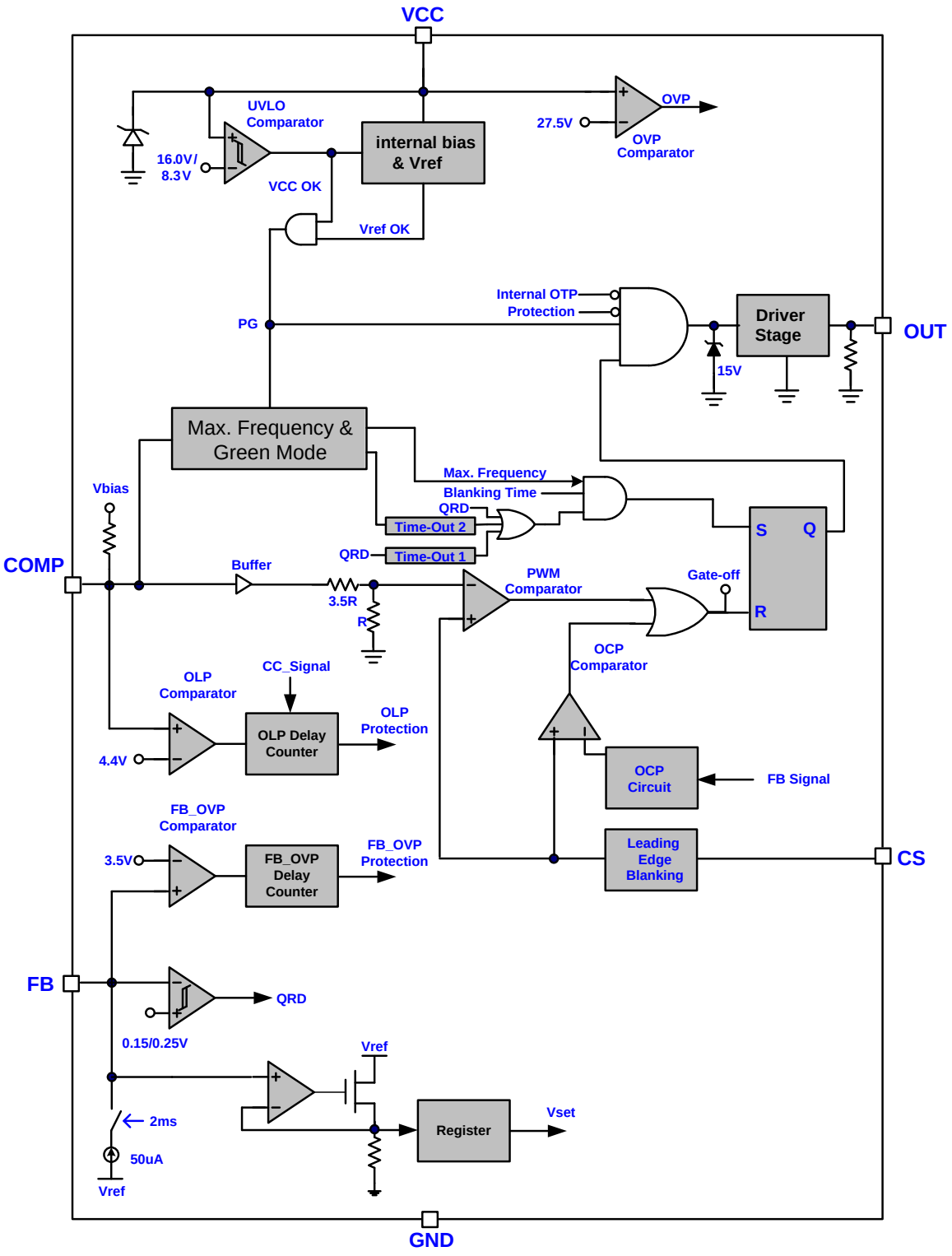
## Protection Mode

| Switching Freq. | VCC OVP | FB_OVP | OLP & CC OLP |
|---|---|---|---|
| 130kHz | Auto recovery / 64μs | Auto recovery / 128μs | Auto recovery/ 65ms |

## Pin Descriptions

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | COMP | Voltage feedback pin (same as the COMP pin in UC384X). Connect a photo-coupler to close the control loop and achieve the regulation. |
| 2 | GND | GND |
| 3 | FB | Adjustable frequency swapping range, OVP and Quasi Resonant detection. |
| 4 | CS | Current sense pin, connect it to sense the MOSFET current. This pin is also connected to an auxiliary winding of the PWM transformer through a resistor and a diode for output over-voltage protection. |
| 5 | VCC | Supply voltage pin |
| 6 | OUT | Gate drive output to drive the external MOSFET |

## Block Diagram



## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage VCC | -0.3V ~30V |
| COMP, FB, CS | -0.3V ~7V |
| OUT | -0.3V ~Vcc+0.3V |
| Maximum Junction Temperature | 150°C |
| Storage Temperature Range | -65°C to 150°C |
| Package Thermal Resistance (SOT-26, $\theta_{JA}$) | 200°C/W |
| Power Dissipation (SOT-26, at Ambient Temperature = 85°C) | 200mW |
| Lead temperature (Soldering, 10sec) | 260°C |
| ESD Voltage Protection, Human Body Model | 2.5 KV |
| ESD Voltage Protection, Machine Model | 250 V |

**Caution:**

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

## Recommended Operating Conditions

| Item | Min. | Max. | Unit |
|---|---|---|---|
| Operating Junction Temperature | -40 | 125 | °C |
| Supply VCC Voltage | 9 | 26.5 | V |
| VCC Capacitor | 3.3 | 10 | μF |
| Start-up resistor Value (AC Side, Half Wave) | 400K | 1.8M | Ω |
| Comp Pin Capacitor | 1 | 100 | nF |
| CS Pin Capacitor Value | 47 | 390 | pF |

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

## Electrical Characteristics

($T_A$ = +25°C unless otherwise stated, $V_{CC}$=15.0V)

| PARAMETER | CONDITIONS | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Supply Voltage (Vcc Pin)** | | | | | | |
| Startup Current | | $I_{CC\_ST}$ | 3 | 10 | 12 | μA |
| Operating Current (with 1nF load on OUT pin) | $V_{COMP}$=0V | $I_{CC\_OP1}$ | | 0.6 | | mA |
| | $V_{COMP}$=3V | $I_{CC\_OP2}$ | | 0.8 | | mA |
| | OVP/OLP Tripped/ Auto | $I_{CC\_OPA}$ | | 0.55 | | mA |
| UVLO (off) | | $V_{CC\_OFF}$ | 7.8 | 8.3 | 8.8 | V |
| UVLO (on) | | $V_{CC\_ON}$ | 15 | 16 | 17 | V |
| $V_{CC}$ OVP Level | | $V_{CC\_OVP}$ | 26.5 | 27.5 | 28.5 | V |
| OVP pin de-bounce time | | $T_{D\_VCCOVP}$ | | 80 | | μs |
| **Voltage Feedback (Comp Pin)** | | | | | | |
| Short Circuit Current | $V_{COMP}$=0V | $I_{COMP}$ | 0.125 | 0.15 | 0.175 | mA |
| Open Loop Voltage | COMP pin open | $V_{COMP\_OPEN}$ | 5.05 | 5.30 | 5.55 | V |
| Input voltage to CS attenuation(1) | | AV | | 1/4.5 | | V/V |
| OLP Trip Level | | $V_{OLP}$ | 4.2 | 4.4 | 4.6 | V |
| Maximum Frequency Mode Threshold VCOMP | * | $V_N$ | | 1.8 | | V |
| Green Mode Threshold $V_{COMP1}$, $V_{SG1}$ | * | $V_G$ | | 1.4 | | V |
| Burst Mode, $V_{BURST}$ | | $V_{ZDC}$ | | 0.9 | | V |
| | Hysteresis | $V_{ZDCH}$ | | 100 | | mV |
| **Current Sensing (CS Pin)** | | | | | | |
| Maximum Input Voltage, $V_{CS}$(off) | | $V_{CS\_MAX}$ | 0.825 | 0.85 | 0.875 | V |
| Leading Edge Blanking Time | | $T_{LEB}$ | | 320 | | ns |
| Input impedance | | $Z_{CS}$ | 1 | | | MΩ |
| Delay to Output | | $T_{PD}$ | | 100 | | ns |

## Electrical Characteristics

($T_A$ = +25°C unless otherwise stated, $V_{CC}$=15.0V)

| PARAMETER | CONDITIONS | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **QRD (Quasi Resonant Detection, FB Pin)** | | | | | | |
| Upper Clamp Voltage | $I_{DET}$=100μA | FB_UP | 4.3 | 4.6 | 4.9 | V |
| Lower Clamp Voltage | $I_{DET}$=-1mA | FB_DN | 0 | | -0.3 | V |
| OVP Trip voltage Level | | $V_{FB\_OVP}$ | | 3.5 | | V |
| OVP De-bounce Cycle | * | $T_{D\_FBOVP}$ | | 128 | | μs |
| Lower Clamp Voltage | $I_{DET}$=-1mA | FB_CLAMP | 0 | | -0.3 | V |
| QRD Trip Level | | QRD | | 150 | | mV |
| | *Hysteresis | QRDH | | 100 | | mV |
| QRD Delay Time | * | $T_{QRD}$ | | 150 | | ns |
| QR Mode Time Out 1 | | $T_{TIME\_1}$ | 4.5 | 6 | 7.5 | μs |
| Max Frequency Clamp Time Out 2 | | $T_{TIME\_2}$ | | 150 | | μs |
| | *During soft-start | $T_{TIME\_S\_2}$ | | 100 | | μs |
| QR Mode Blanking Time | | $T_{QR\_LEB}$ | | 2 | | μs |
| Input bias current | *$V_{FB}$=1V~5V, OUT=OFF | $I_{BIAS}$ | 0 | | 1.0 | μA |
| **Oscillator for Switching Frequency** | | | | | | |
| Maximum Frequency | COMP=3V | $F_{SW}$ | 122 | 130 | 138 | kHz |
| Swapping Frequency | 1.7V<VFB | $F_{SW\_MOD}$ | | ±6% | | kHz |
| Green Mode Frequency | | $F_{SW\_GREEN}$ | 21.5 | 25 | 28 | kHz |
| Temp. Stability | * | $F_{SW\_TS}$ | 0 | 3 | 5 | % |
| Voltage Stability | * ($V_{CC}$=9V-24V) | $F_{SW\_VS}$ | 0 | | 1 | % |
| **Maximum ON Time** | | | | | | |
| Maximum On Time | | $T_{ON\_MAX}$ | | 18 | | μs |
| **Adjustable Jitter Frequency on ZCD pin.** | | | | | | |
| Jitter Frequency | $V_{FB}$<0.7 | $F_{SET\_1}$ | | ±0% | | kHz |
| | 0.7V<$V_{FB}$<1.1 | $F_{SET\_2}$ | | ±2% | | kHz |
| | 1.1V<$V_{FB}$<1.7 | $F_{SET\_3}$ | | ±4% | | kHz |
| | 1.7V<$V_{FB}$ | $F_{SET\_4}$ | | ±6% | | kHz |

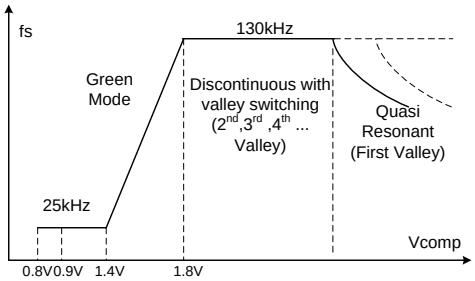



**Fig 1. $V_{COMP}$ vs. Maximum Frequency**

## Electrical Characteristics

($T_A$ = +25°C unless otherwise stated, $V_{CC}$=15.0V)

| PARAMETER | CONDITIONS | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Gate Drive Output (OUT Pin)** | | | | | | |
| Output Low Level | $V_{CC}$=15V, Io=20mA | $V_{OL}$ | 0 | | 1 | V |
| Output High Level | $V_{CC}$=15V, Io=20mA | $V_{OH}$ | 9 | | VCC | V |
| Output High Clamp Level | $V_{CC}$=9V, Out pin open | $V_{O\_CLAMP}$ | 7 | | VCC | V |
| Rising Time | *$V_{CC}$=15V, $C_L$=1000pF | $T_r$ | | 200 | | ns |
| Falling Time | *$V_{CC}$=15V, $C_L$ =1000pF | $T_f$ | | 80 | | ns |
| Output High Clamp Level | $V_{CC}$=18V | $V_{CLAMP}$ | 13 | 15 | 17 | V |
| **Soft Start** | | | | | | |
| Soft Start Time | * $V_{CS}$-off from 0.2V to 0.85V | $T_{SS}$ | 6 | 7 | 8 | ms |
| C.C. Start-Up Disable Level | * | $V_{C.C}$ | | 1.5 | | V |
| C.C. Start-Up Disable Time | * VFB<2.5V | $T_{C.C}$ | | 20 | | ms |
| **Open Loop Protection** | | | | | | |
| OLP delay time | | $T_{OLP}$ | | 66 | | ms |
| **On Chip OTP (Over Temperature)** | | | | | | |
| OTP Level(1,2) | | $T_{INOTP}$ | | 140 | | °C |
| OTP Hysteresis(1,2) | | $T_{INOTP\_HYS}$ | | 30 | | °C |

**Notes:**

**1.*: Guaranteed by design**

**2.The threshold temperature to enable the output again and reset the latch after OTP is activated.**

## Typical Performance Characteristics

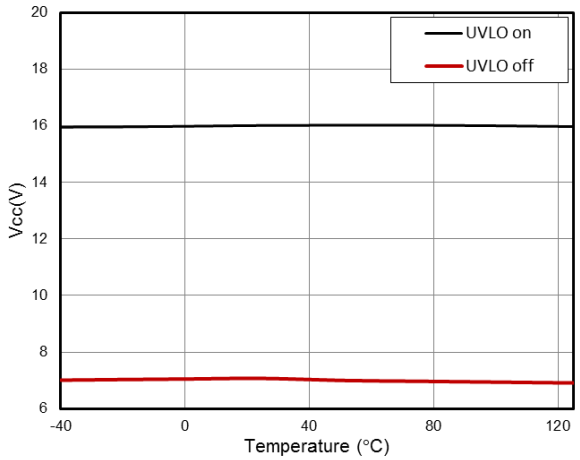


Fig. 2 UVLO level vs.Temperature

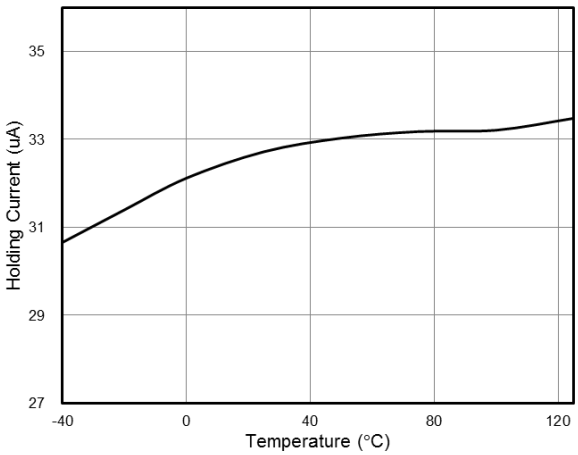


Fig. 3 Holding Current vs.Temperature

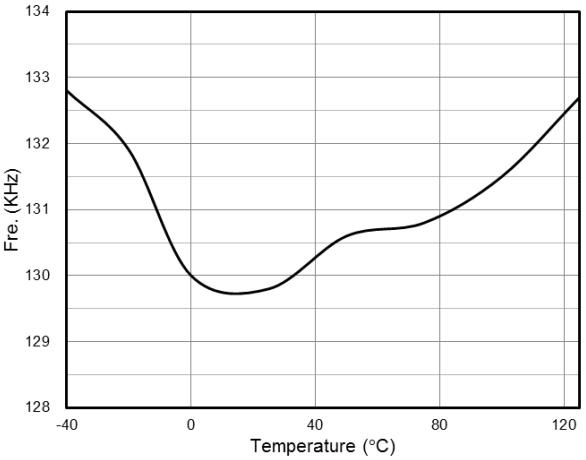


Fig. 4 Max. Frequency vs.Temperature

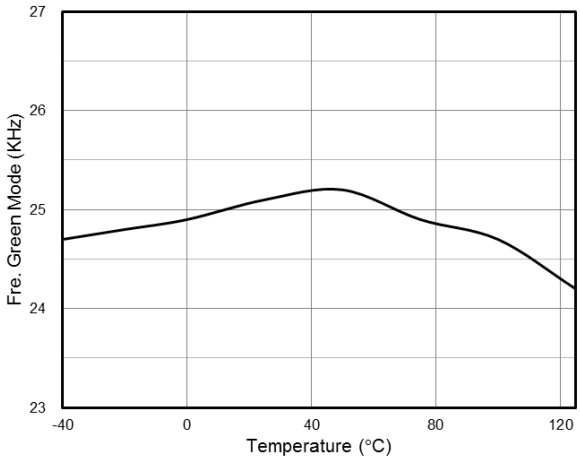


Fig. 5 Fre. Green Mode vs.Temperature

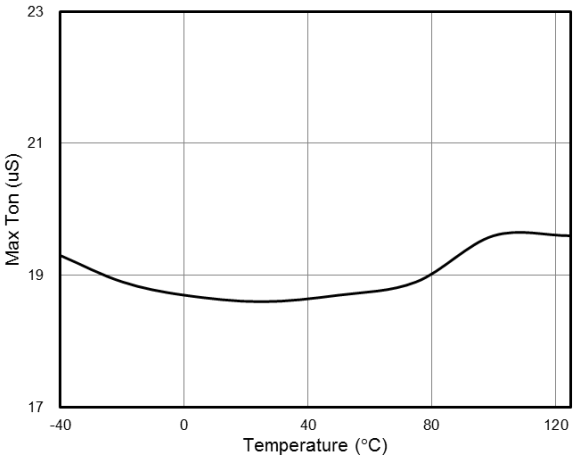


Fig. 6 Max Ton vs.Temperature

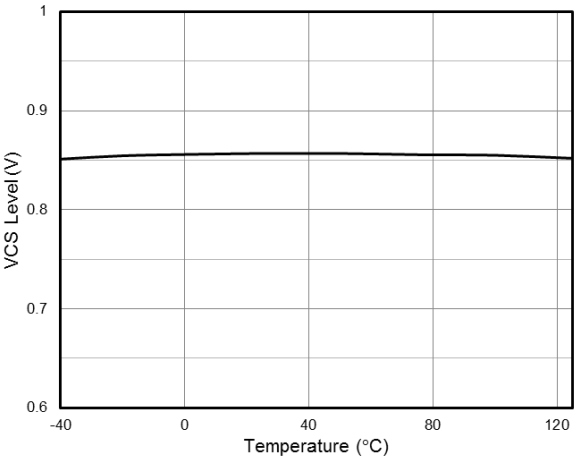


Fig. 7 Limit level vs.Temperature

## Typical Performance Characteristics

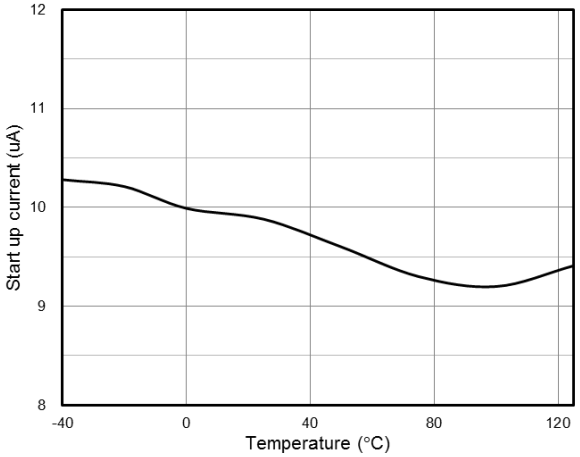


Fig. 8 Start up current vs.Temperature

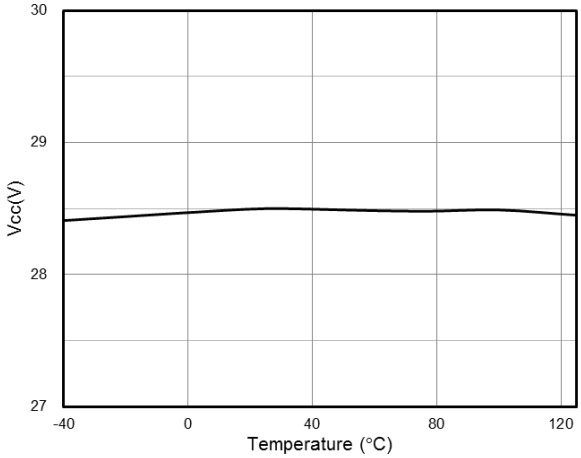


Fig. 9 Vcc OVP Level vs.Temperature

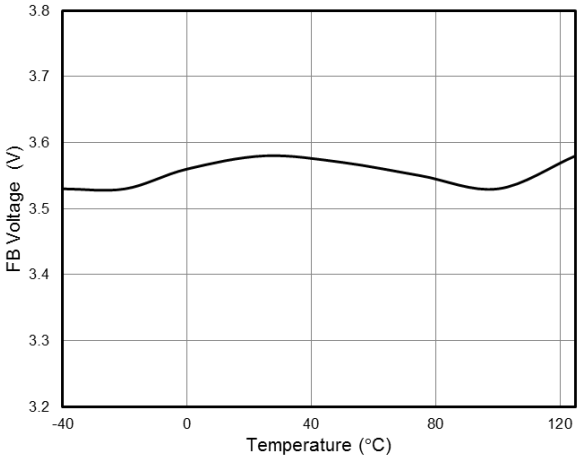


Fig. 10 FB OVP Level vs.Temperature

# Application Information

## Operation Overview

The LD5520 meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving by Quasi-Resonant flyback. It integrates more functions to reduce the external components counts and the size. Its major features are described as below.

## Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage across the VCC pin. It would assure the supply voltage enough to turn on the LD5520 PWM controller and further to drive the power MOSFET. As shown in Fig. 11, a hysteresis is built in to prevent shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.0V and 8.3V, respectively.

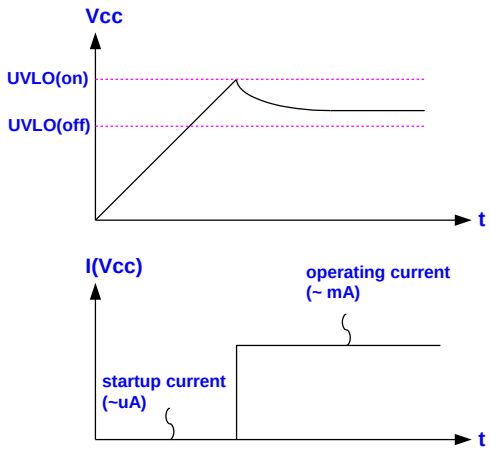



**Fig. 11**

## Startup Current and Startup Circuit

The typical startup circuit to generate $V_{CC}$ of the LD5520 is shown in Fig. 12. During the startup transient, the $V_{CC}$ is below UVLO threshold. Before it has sufficient voltage to develop OUT pulse to drive the power MOSFET, R1 will provide the startup current to charge the capacitor C1. Once $V_{CC}$ obtains enough voltage to turn on the LD5520 and further to deliver the gate drive signal, it will enable the auxiliary winding of the transformer to provide supply current. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current for LD5520 is only 12μA.

If a higher resistance value of the R1 is selected, it usually spends more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

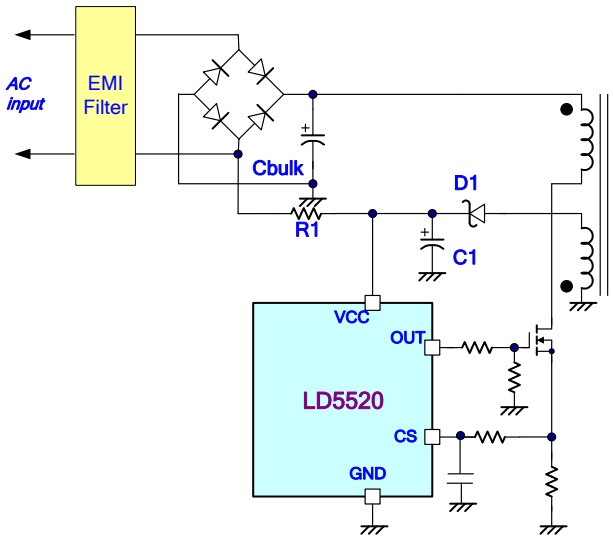



**Fig. 12**

## Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 13, the LD5520 detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current is concluded as below.

$$I_{PEAK\,(MAX)} = \frac{0.85V}{R_S}$$

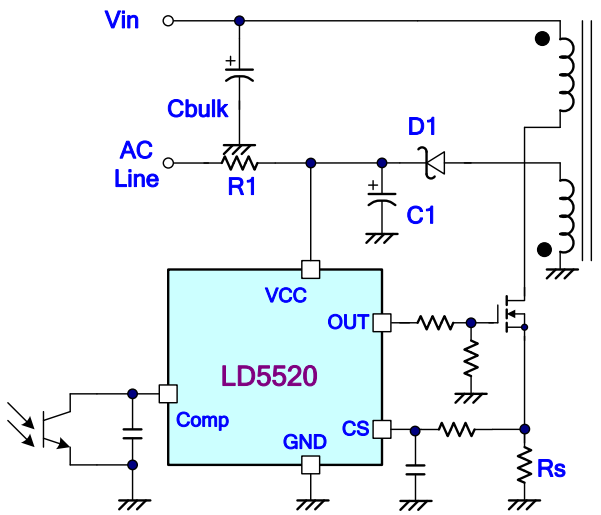



**Fig. 13**

A 250nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent false-triggering from the current spike. In those low power applications, if the total pulse width of the turn-on spikes is less than 150nS and the negative spike on the CS pin below -0.3V, the R-C filter is free to eliminate. (As shown in Fig. 14).

However, the total pulse width of the turn-on spike is subject to output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in Fig. 15) for large power application to avoid the CS pin being damaged by the negative turn-on spike.

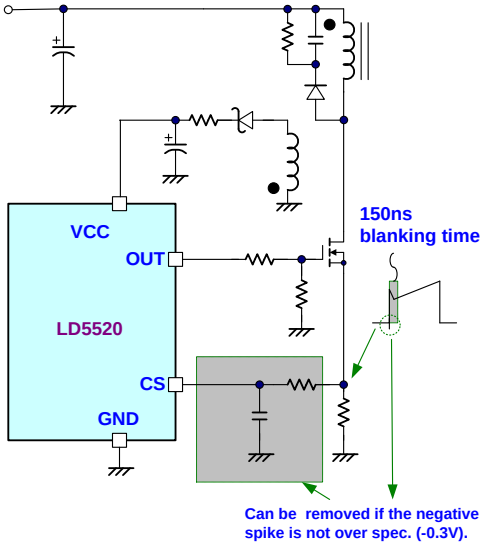



**Fig. 14**

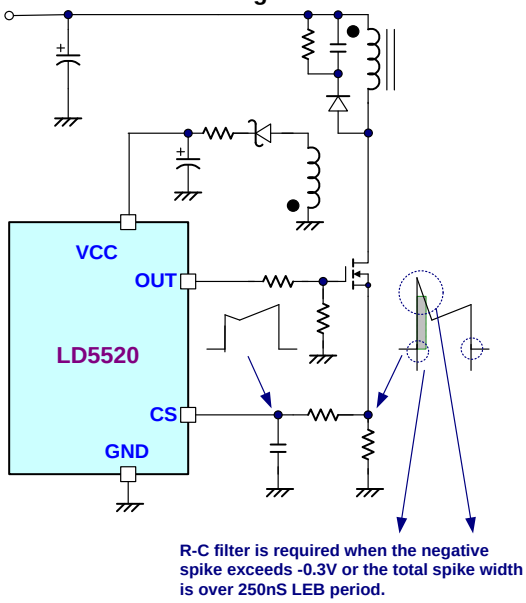



**Fig. 15**

## Output Stage and Maximum ON Time

An output stage of a CMOS buffer, with typical 100mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum on time of LD5520 is limited to 18us to avoid the transformer saturation.

## Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD5520. Similar to UC3842, the

LD5520 would without any voltage offset at the stage to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{RB}{RA+RB} \times V_{COMP}$$

A pull-high resistor is embedded internally and therefore no external one is required.

## Q-R Mode Detection

The transformer will be demagnetized after the main power MOSFET turns off. A quasi resonant signal will be detected from auxiliary winding by FB pin through the external resister.

As soon as the current of the secondary side diode is down to zero during MOSFET-off period, the transformer's core is demagnetized completely. $V_{DS}$ of MOSFET will resonate in discontinuous current mode. The resonance frequency ($F_{QR}$) will be obtained as below.

$$F_{QR} = \frac{1}{2\pi\sqrt{L_m * C_R}} (HZ)$$

$L_M$ = Inductance of primary winding
$C_R$ = Resonance equivalent parasitic capacitance

If $V_{DS}$ voltage falls to resonant valley level from max plateau value, the QRD comparator will be tripped while FB pin voltage is close to 150mV.

## On/Off Control

To pull COMP below 0.9V can disable the gate output pin of the LD5520. The off-mode can be released when the pull-low signal is removed.

## Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage in over-load short or open-loop condition, the LD5520 is implemented with smart OLP function. It also features auto recovery function; see Fig. 16 for the waveform. In case of fault condition, the feedback system will force the voltage loop enter toward saturation and then pull the voltage high on COMP pin (VCOMP). When the $V_{COMP}$ ramps up to the OLP threshold of 4.4V and continues over OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

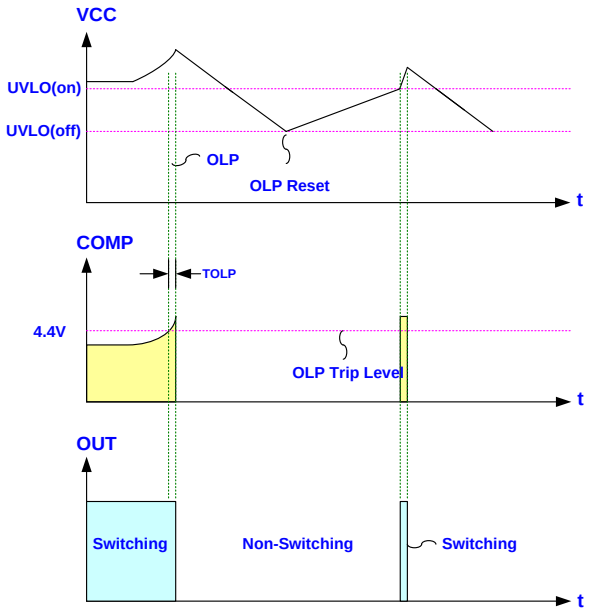



**Fig. 16**

## FB PIN OVP (FB PIN Over Voltage Protection) - Auto Recovery

An output overvoltage protection is implemented in the LD5520, as shown in Fig. 17. This works for the LD5520 by sensing the auxiliary voltage via the divided resistors. The auxiliary winding voltage is reflected from secondary winding and therefore the flat voltage on the FB pin is proportional to the output voltage.

LD5520 can sample this flat voltage level after a delay time to perform output over-voltage protection. The sampling voltage level is compared with internal threshold voltage 3.5V. The equation of FB_OVP is showing below.

$$3.5V = \frac{R_2}{R_1+R_2} \times VAUX$$

If the sampling voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP events.

The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. However, typically, if any 128μs of subsequent OVP event is detected, the OVP circuit will switch the power MOSFET off due to its auto-recovery mode of protection.

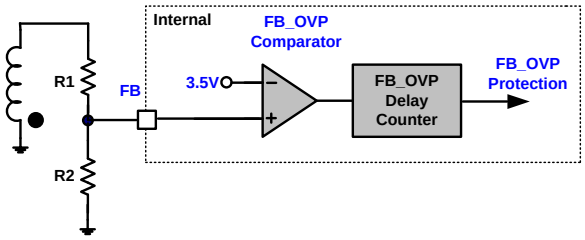



**Fig. 17**

## OVP (Over Voltage Protection) on Vcc – Auto Recovery

The maximum VGS ratings of the power MOSFETs are mostly for 30V. To prevent the VGS enter fault condition, LD5520 series are implemented with OVP function on Vcc. Whenever the Vcc voltage is higher than the OVP threshold, the output gate drive circuit will be shutdown simultaneously and the switching of the power MOSFET is disabled until the next UVLO(on).

The Vcc OVP functions of LD5520 are auto-recoverable. If the OVP condition, usually caused by open-loop of feedback, is not released, the Vcc will tripped the OVP level again and re-shutdown the output. The Vcc works in hiccup mode. Figure 18 shows its operation.

Otherwise, when the OVP condition is removed, the Vcc level will be resumed and the output will automatically return to the normal operation.

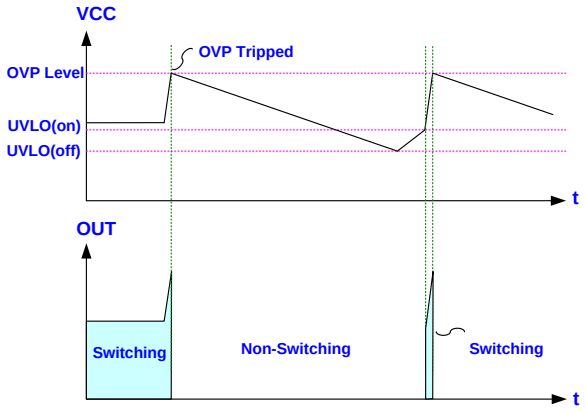



**Fig. 18**

## Adjustable Frequency Swapping Range on FB pin

The LD5520 is implemented with Frequency Swapping function which helps the power supply designers optimize EMI performance and reduce system cost. The frequency swapping range is adjusted, and swap range can setting between of 0% ~ ±6% for different system.

Initial conditions, when VCC voltage is higher than UVLO ON. The FB PIN will provide a current to change resistor of FB side and OUT PIN is still no signal. In this time, the IC will detect the FB voltage and regulate frequency swapping range as Figure 19. This FB voltage divider at the ratio of R1 and R2, that is,

$$R_{total} = \frac{R_1 \times R_2}{R_1 + R_2}$$

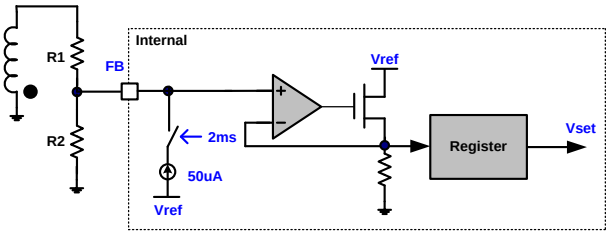



**Fig. 19**

Table 1 shows the result between FB voltage and frequency swapping range.

| $R_{TOTAL}$ ideal | $V_{FB}$ Range | Suggestion $R_{TOTAL}$ | Swapping Range |
|---|---|---|---|
| 40k< $R_{TOTAL}$ | 1.7<$V_{FB}$ | 42k | 6% |
| 22k<$R_{TOTAL}$<40k | 1.1<$V_{FB}$<1.7 | 30k | 4% |
| 14k<$R_{TOTAL}$<22k | 0.7<$V_{FB}$<1.1 | 18k | 2% |
| $R_{TOTAL}$ <14k | $V_{FB}$<0.7 | 12k | 0% |

**Table 1**

## Green-Mode Operation

By using the green-mode control, the switching frequency can be enhanced under light load condition. The green-mode control is Leadtrend Technology's own property.

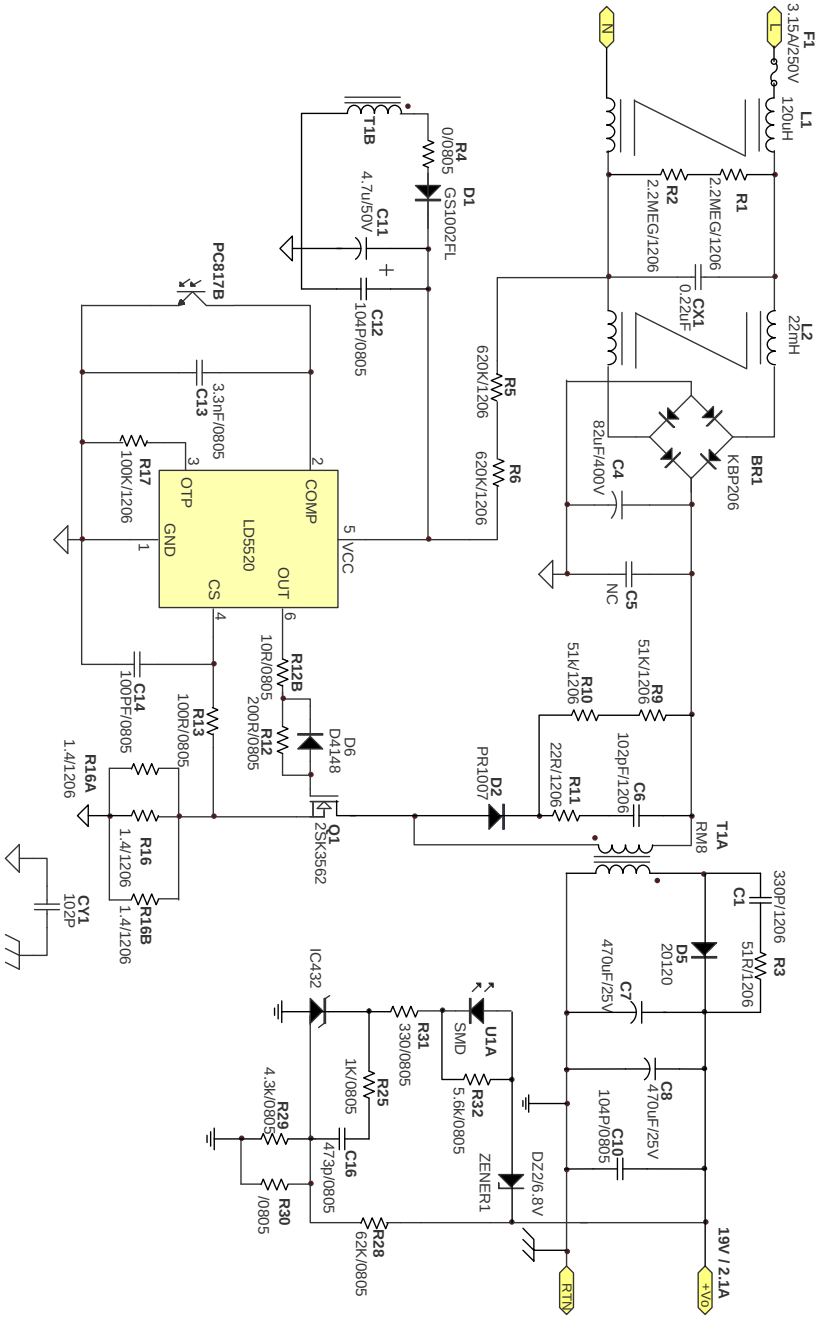
## Fault Protection

There are several critical protections integrated in the LD5520 to prevent from damage for the power supply. Those damages usually came from open or short conditions on LD5520.

In case under the conditions listed below, the gate output will turn off immediately to protect the power circuit.

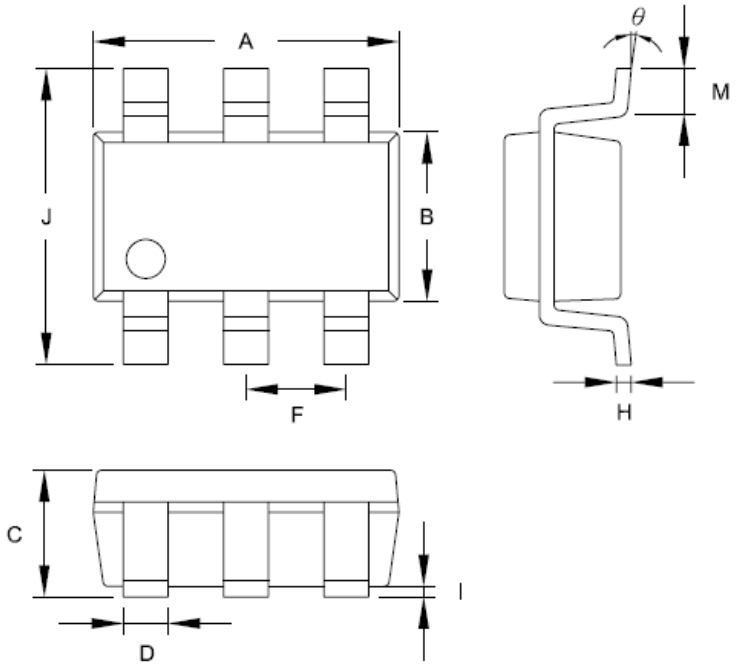
1. CS pin floating
2. COMP pin floating

## Reference Application Circuit --- 40W (19V/2.1A) Adapter



# Package Information

**SOT-26**




| Symbol | Dimension in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 2.692 | 3.099 | 0.106 | 0.122 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| C | ------- | 1.450 | ------- | 0.057 |
| D | 0.300 | 0.500 | 0.012 | 0.020 |
| F | 0.95 TYP | | 0.037 TYP | |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| I | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 2.600 | 3.000 | 0.102 | 0.118 |
| M | 0.300 | 0.600 | 0.012 | 0.024 |
| θ | 0° | 10° | 0° | 10° |

### Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

## Revision History

| REV. | Date | Change Notice |
|---|---|---|
| 00 | 05/17/2016 | Original Specification. |