Multi-Mode PWM Controller of Flyback with Frequency Swapping and Integrated Protection

REV.00

General Description

In order to enhance the efficiency performance, the LD5523M1 integrates the multi-mode PWM controller, which consists of Quasi-Resonant (QR) PWM control for light load condition and peak load mode for heavy load condition. Moreover, the QR controller not only gains the system performance, but also brings the worse EMI capability, while the frequency swapping function of LD5523M1 can reduce the EMI emission of SMPS and helps the power circuit designers to simply deal with EMI filter and saves several component and developing time.

The LD5523M1 is implemented in SOT-26 package, and includes the comprehensive protection function, such as Over Power Protection (OPP), Over Voltage Protection (OVP), Output Short Circuit Protection (OSCP) and internal Over Temperature Protection (OTP). Furthermore, the programmable brown-in/out protection is built-in.

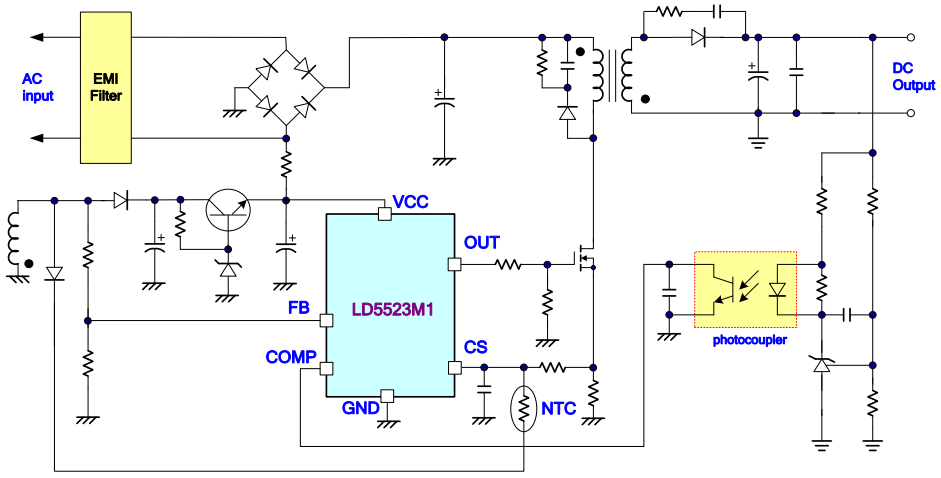
Features

- Low Startup Current (<1μA)
- 0.26mA Ultra-low operating current at light load
- Current Mode Control with Cycle-by-Cycle Current Limit
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- VCC OVP (Over Voltage Protection)
- Adj. OVP (Over Voltage Protection) on FB pin.
- OPP (Over Power Protection)
- External OTP (Over Temperature Protection) on CS Pin
- Internal OTP (Over Temperature Protection)
- SDSP (Secondary Diode Short Protection)
- Gate Source/Sink Capability: 190mA/-150mA @ output pin with 33nF capacitor.

Applications

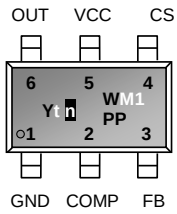
- Switching AC/DC Adaptor

Typical Application



Pin Configuration

SOT-26 (TOP VIEW)



Y : Year code (D: 2004, E: 2005…..)
W : Week code
PP : Production code
t n M1 : LD5523M1

Ordering Information

Part number	Package		TOP MARK	Shipping
LD5523M1GL	SOT-26	(Green Package)	Ytn / WM1 / PP	3000 / tape & reel

The LD5523M1 is RoHs compliant/ green packaged.

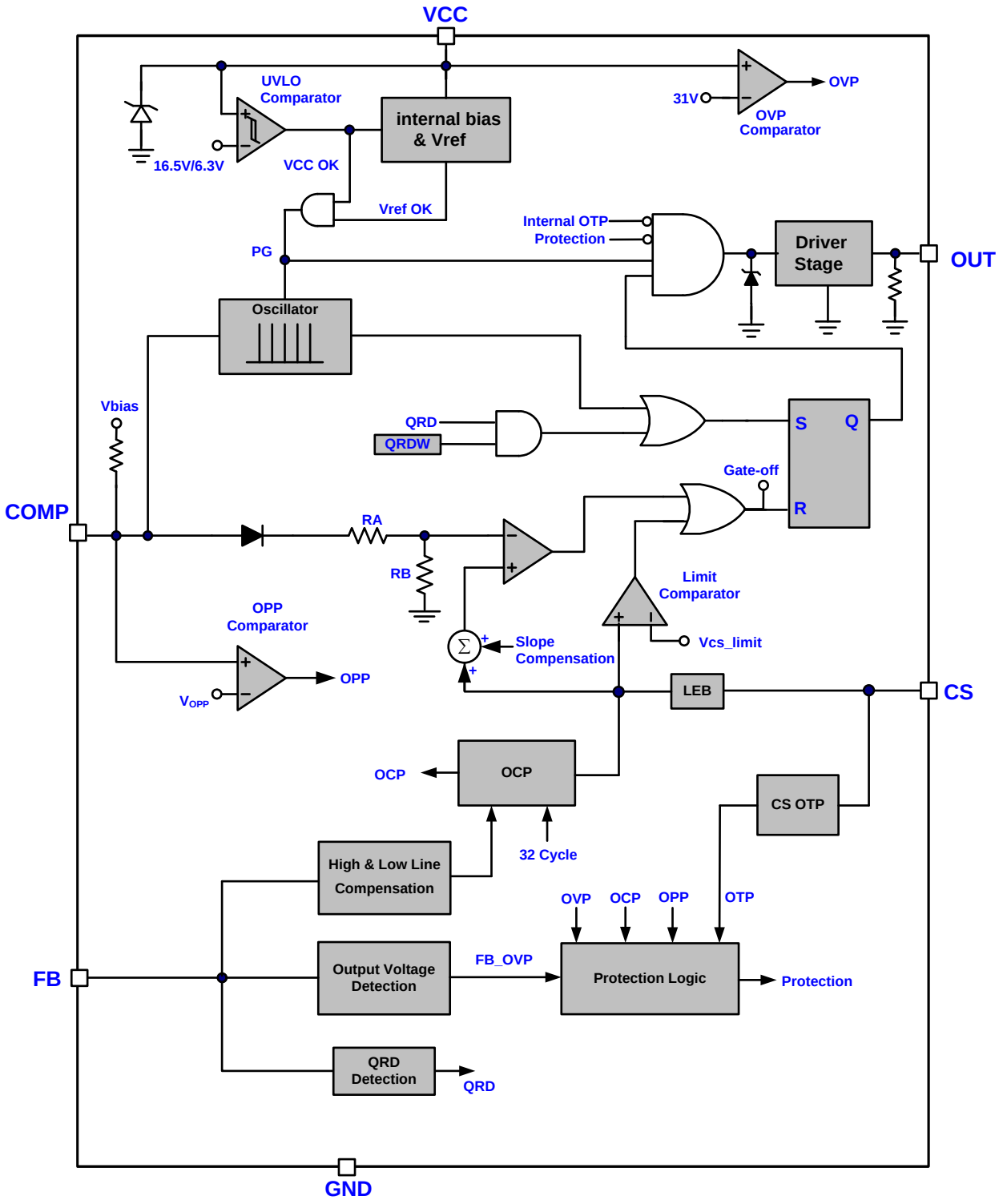
Protection Mode

Product Name	Switching Freq.	VCC_OVP	FB_OVP	OCP / OPP	CS_OTP	Int. OTP
LD5523M1	65k /130k Hz	Latch	Latch	Latch	Latch	Auto recovery

Pin Descriptions

NAME	PIN (SOT-26)	FUNCTION
GND	1	Ground
COMP	2	Output of the error amplifier for voltage compensation
FB	3	Auxiliary voltage sense, brown in/out and Quasi Resonant detection
CS	4	Current sense pin, connect to sense the MOSFET current
VCC	5	Supply voltage pin
OUT	6	Gate drive output to drive the external MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V ~ 32V
COMP	-0.3V ~ 12V
FB, CS	-0.3V ~ 7V
OUT	-0.3V ~ VCC+0.3V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	200°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	200mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stress above recommended operating conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.0	26.5	V
VCC Capacitor	3.3	10	μF
Start-up resistor Value (AC Side, Half Wave)	400K	2M	Ω
Comp Pin Capacitor (X7R type)	330	4700	pF
CS Pin Capacitor Value	47	470	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF ~ 0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible.
2. It's also essential to connect a capacitor to COMP to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current		I_{CC_ST}			1	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V, OUT=1nF	I_{CC_OP1}		0.26		mA
	V_{COMP}=1.7V, OUT=1nF I_{FB}=200μA	I_{CC_OP2}		2.44		mA
	OLP current	I_{CC_OPA1}		0.75		mA
	Brown in (Before the first pulse)/ Brown out	I_{CC_OPA3}		1.1		mA
UVLO(OFF)		V_{CC_OFF}	5.3	6.3	7.3	V
UVLO(ON)		V_{CC_ON}	15.5	16.5	17.5	V
VCC OVP Level		V_{CC_OVP}	30	31	32	V
VCC OVP de-bounce time		T_{VCC_OVP}		8		Cycle
Latch-Off Release Voltage		V_{PDR}		5		V
Voltage Feedback (COMP Pin)						
Short Circuit Current	V_{COMP}=0V	I_{COMP}		0.110		mA
Open Loop Voltage	(1)	V_{COMP_OPEN}		3.2		V
Min. OCP Compensation Current	I_{FB} =100μA (1)	I_{OCP_MIN}		78.75		μA
Max. OCP Compensation Current	I_{FB} =300μA	I_{OCP_MAX}		225		μA
Current Sensing (CS Pin)						
Maximum Input Voltage		V_{CS_LIMIT}	0.584	0.615	0.645	V
OCP Voltage	V_{FB} < 0.85	V_{CS_1}	0.296	0.315	0.334	V
	0.85 < V_{FB} < 1.2V	V_{CS_2}	0.353	0.375	0.397	V
	V_{FB} > 1.25	V_{CS_3}	0.437	0.465	0.492	V
Leading Edge Blanking Time		T_{LEB}	240	400	560	ns
Internal Slope Compensation	*ton>3μs to D_{MAX}. (Linearly increase), (1)	V_{SLP_L}		165		mV
Delay to Output	(1)	T_{PD}		80		ns

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
QRD (Quasi Resonant Detection, FB Pin)						
FB OVP Trip voltage Level		V_{FB_OVP}	2.65	2.8	2.95	V
FB OVP De-bounce Time		T_{FB_OVP}	6	8	10	Cycle
QRD Trip Level	(1)	I_{QRD}		10		μA
BNO Protection (FB Pin)						
Brown In Trip Level		I_{BNI}		145		μA
BNO Hysteresis		I_{BNO_HYS}		15		μA
Brown Out De-bounce Time	V_{COMP}=1.7V	T_{DB_BNO}	28	44	60	ms
OTP (Over Temperature, CS Pin)						
CS OTP Level	V_{FB}=1V~3V(1)	V_{CS_OTP}		0.25*V_{FB}		V
CS OTP de-bounce time	(1)	T_{CS_OTP}	2	5.4	13	ms
Oscillator for Switching Frequency						
Frequency for Low Line	I_{FB}<360uA (1)	F_{SW_H}	60	65	70	kHz
Frequency for High Line	I_{FB}<330uA (1)	F_{SW_L}		130		kHz
Frequency Swapping		F_{SW_MOD}		±8		%
Green Mode Frequency		F_{SW_GREEN}	21	24	27	kHz
Temp. Stability	(1)	F_{SW_TS}		3	5	%
Voltage Stability	VCC =9V~24V(1)	F_{SW_VS}			1	%
Maximum Duty		D_{MAX}		81		%
Gate Drive Output (OUT Pin)						
Output Low Level	VCC =15V, Io=20mA	V_{OL}			1	V
Output High Level	VCC =15V, Io=20mA	V_{OH}	10		15	V
Rising Time	VCC =15V C_L=1000pF	T_r		280		ns
Falling Time	VCC =15V C_L =1000pF	T_f		60		ns
Output High Clamp Level	VCC =18V	V_{O_CLAMP}		14		V
Soft Start						
Soft Start Time	V_{CS_OFF} from 0.2V to 0.5V (1) (COMP > V_{COMP_OPP})	T_{SS}		7		ms
SDSP (Secondary Diode Short Protection)						
SDSP CS Pin Level	Secondary diode short	V_{CS_SDSP}		1.15		V
De-bounce Cycle	(1)	T_{D_SDSP}	2	4	6	Cycle

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
OPP (Over Power Protection)						
OPP Trip Level		V_{COMP_OPP}	2.85	3	3.15	V
OPP Delay Time	After soft-start	T_{D_OPP}	55	88	120	ms
OCP (Over Current Protection)						
OCP Delay Time	After soft-start	T_{D_OCP}	120	225	330	ms
OCP Reset Time	(1)	T_{R_OCP}		32		Cycle
On Chip OTP (Over Temperature Protection)						
OTP Level	(1,2)	T_{INOTP}		140		°C
OTP Hysteresis	(1,2)	T_{INOTP_HYS}		12		°C

Notes:
1. Guaranteed by design.
2. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.

Typical Performance Characteristics

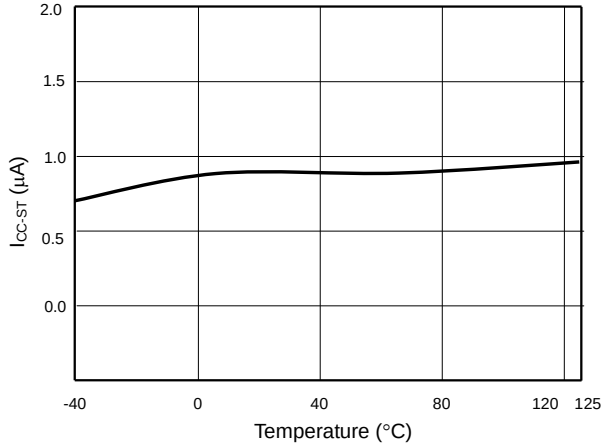


Fig. 1 Startup Current vs. Temperature

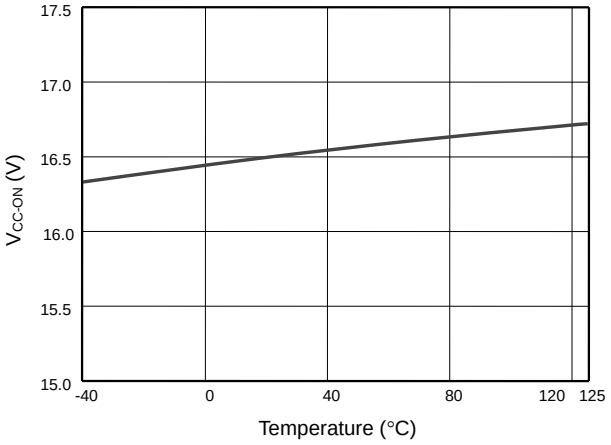


Fig. 2 UVLO (on) vs. Temperature

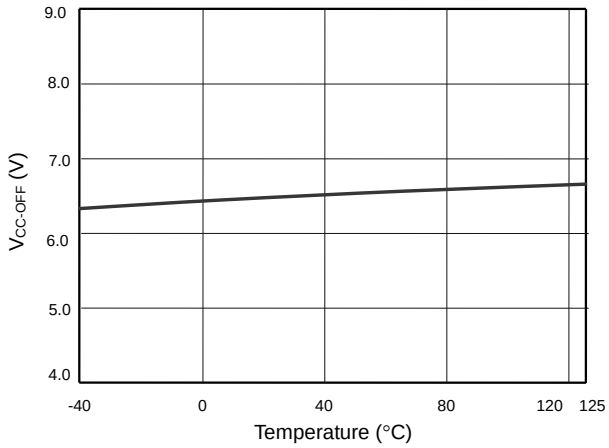


Fig. 3 UVLO (off) vs. Temperature

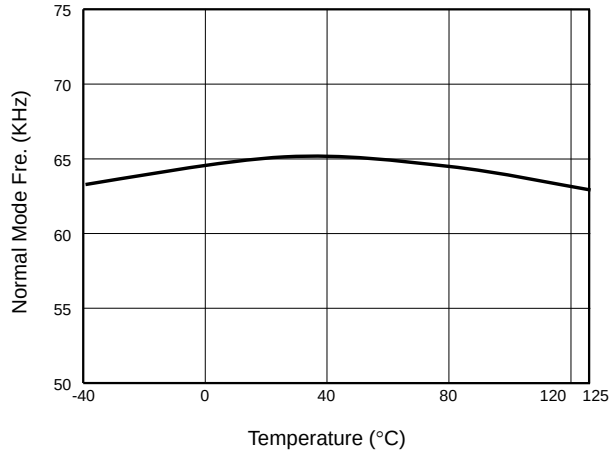


Fig. 4 Normal Mode Fre. vs. Temperature

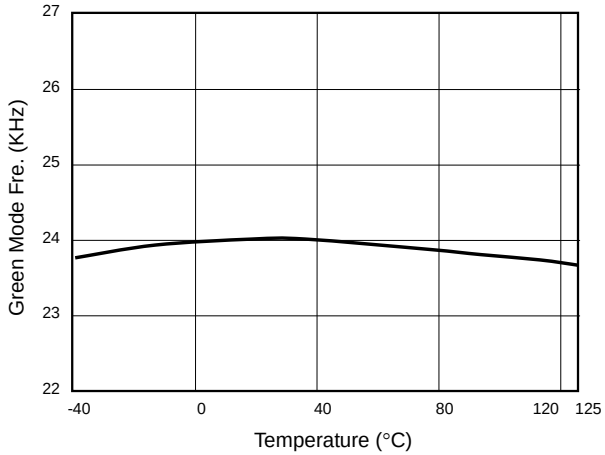


Fig. 5 Green Mode Fre. vs. Temperature

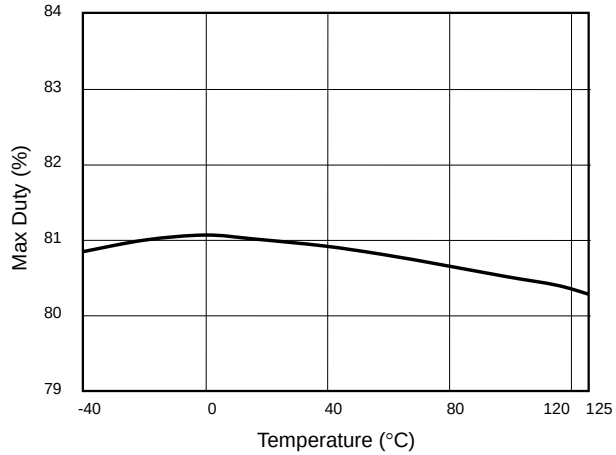


Fig. 6 Max Duty vs. Temperature

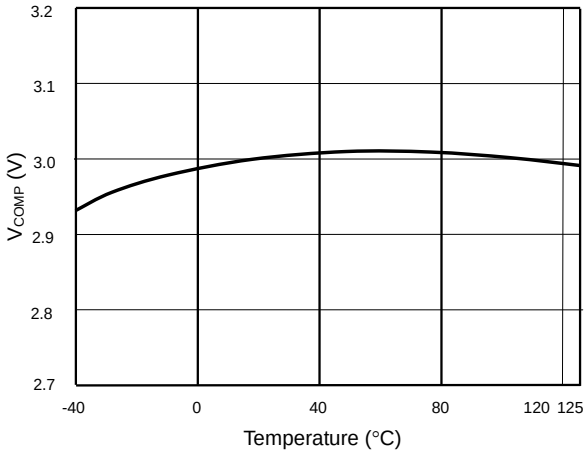


Fig. 7 VOPP vs. Temperature

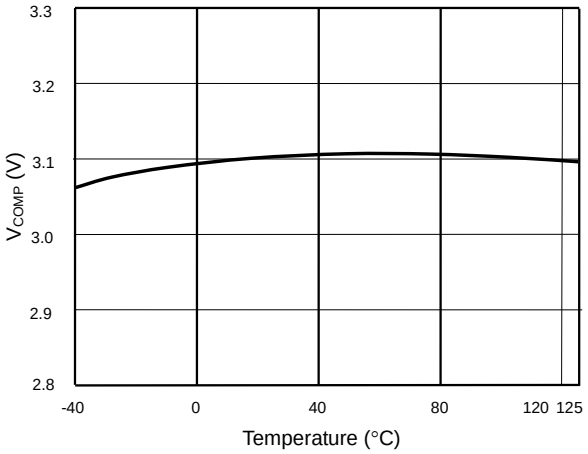


Fig. 8 Open Loop Voltage vs. Temperature

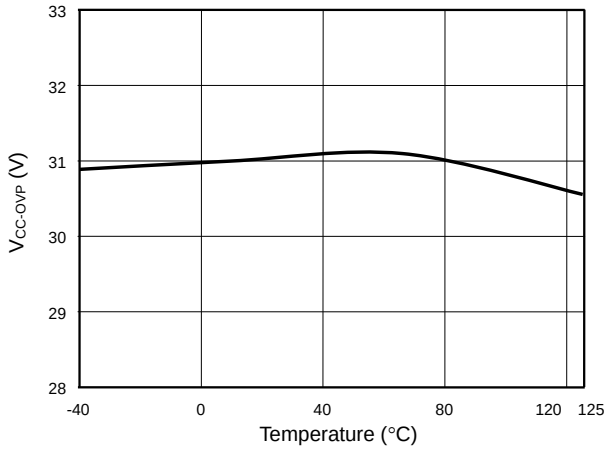


Fig. 9 VCC OVP vs. Temperature

Application Information

Operation Overview

The LD5523M1 is built in the multi-mode PWM controller, in which operates a high frequency to avoid the transformer saturation in over load condition. For demanding higher power efficiency and power-saving in light load condition, the LD5523M1 implements QR function to allow the valley switching and accomplish zero voltage switching (ZVS). Under different load conditions, LD5523M1 provides the different solutions for achieving higher efficiency and performance.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD5523M1 PWM controllers and further to drive the power MOSFET. As shown in Fig. 10, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.5V and 6.3V, respectively.

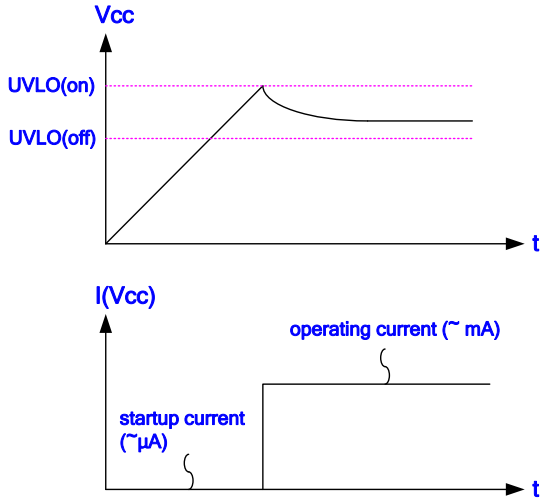


Fig. 10

Startup Current and Startup Circuit

The typical startup circuit to generate the LD5523M1 VCC is shown in Fig. 11. During the startup transient, the VCC is lower than the UVLO threshold thus there is no gate pulse produced from LD5523M1 to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the VCC voltage is high enough to turn on the LD5523M1 and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer.

Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD5523M1 is only 1μA. If a higher resistance value of R1 is chosen, it usually takes more time to start up. To select the value of R1 and C1 carefully will optimize the power consumption and startup time.

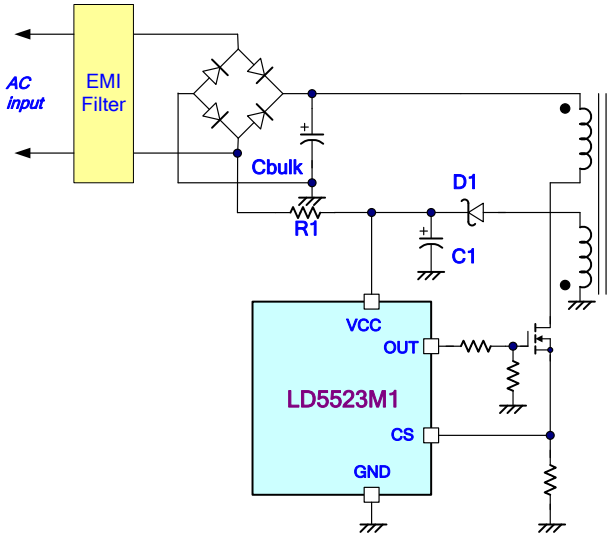


Fig. 11

QR Mode Detection

The transformer will be demagnetized after the main power MOSFET turns off. A quasi resonant signal will be detected from auxiliary winding by FB pin through the external resister.

As soon as the current of the secondary side diode is down to zero during MOSFET-off period, the transformer's core is demagnetized completely. V_{DS} of MOSFET will resonate in discontinuous current mode. The resonance frequency (F_{QR}) will be obtained as below.

$$F_{QR} = \frac{1}{2\pi\sqrt{L_m * C_R}} (HZ)$$

L_M = Inductance of primary winding

C_R = Resonance equivalent parasitic capacitance

If V_{DS} voltage falls to resonant valley level from max plateau value, the QRD comparator will be tripped while FB pin current is close to 10μA.

However, the QR detection will be influenced by propagation delay. If inductance of primary winding is less than 500μH, there is barb in Vds (as shown in Fig. 12).

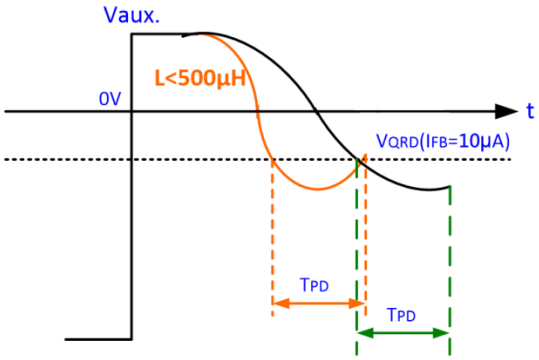


Fig. 12

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD5523M1. Similar to UC3842, the LD5523M1 would without voltage offset to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{-(PWM\ COMPARATOR)} = \frac{RB}{RA + RB} \times V_{COMP}$$

A pull-high resistor is embedded internally and therefore no external one is required.

The LD5523M1 integrates the multi-mode PWM controller, and for enhance the light load efficiency, the comp pin value corresponding to the frequency is as shown in Fig. 13. (V_{FB}<1.25V)

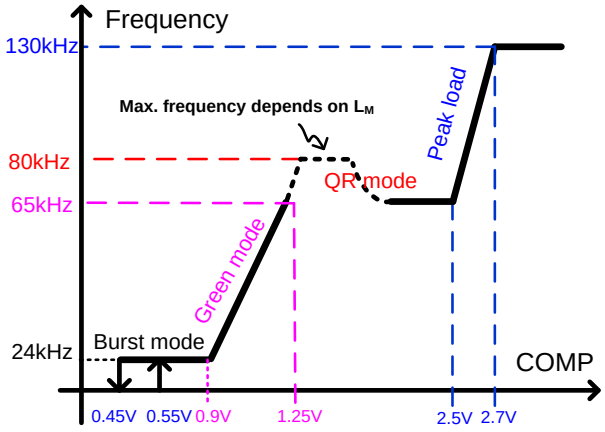


Fig. 13

Current Sensing, Leading Edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD5523M1 detect the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin sets at 0.615V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK\_MAX(Low\ \ line)} = \frac{0.615V}{R_{CS}}$$

A 400ns leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spike is less than 400ns and the negative spike on the CS pin doesn't exceed -0.3V, it could remote the R-C filter (as shown in the Fig. 14).

However, the total pulse width of the turn-on spike is decided by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in Fig. 15) for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

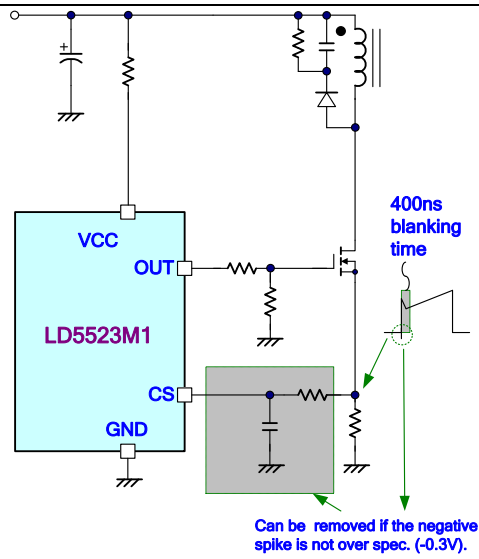


Fig. 14

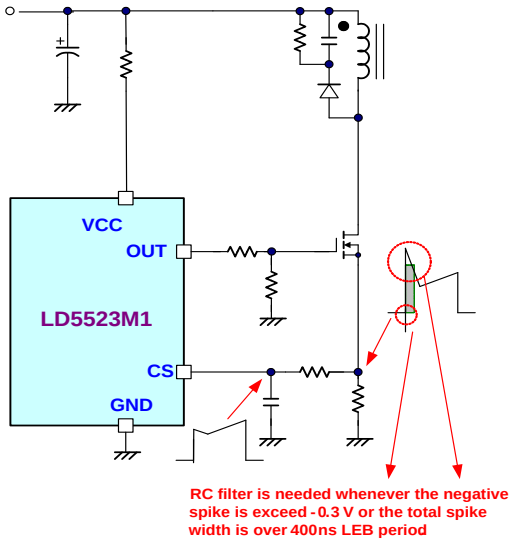


Fig. 15

Output Stage and Maximum Duty

An output stage of a CMOS buffer, with typical 190mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty of LD5523M1 is limited to 81% avoid detecting QR fail.

Over Voltage Protection on VCC Pin (VCC OVP) – Latch

The V_{GS} ratings of the nowadays power MOSFETs are often limited up to max. 31V. To prevent the V_{GS} from the fault condition, LD5523M1 is implemented with an OVP function on VCC. Whenever the VCC voltage is higher than the OVP threshold voltage, the LD5523M1 output gate drive circuit will be shutdown simultaneously to latch off the power MOSFET as Fig. 16.

On the contrast, if the voltage on VCC pin drops below PDR and starts AC-recycling again, it will soon resume to normal operation.

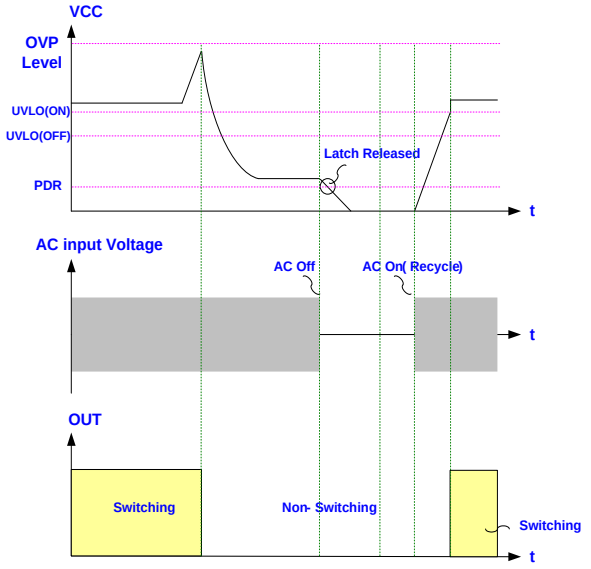


Fig. 16

Over Power Protection (OPP) – Latch

To protect the circuit from damage due to over-load condition and short or open-loop condition, the LD5523M1 is implemented with smart OPP function. It also features Latch function; see Fig. 17 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (V_{COMP}). When the V_{COMP} ramps up to the OPP threshold of 3V and continues over OPP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

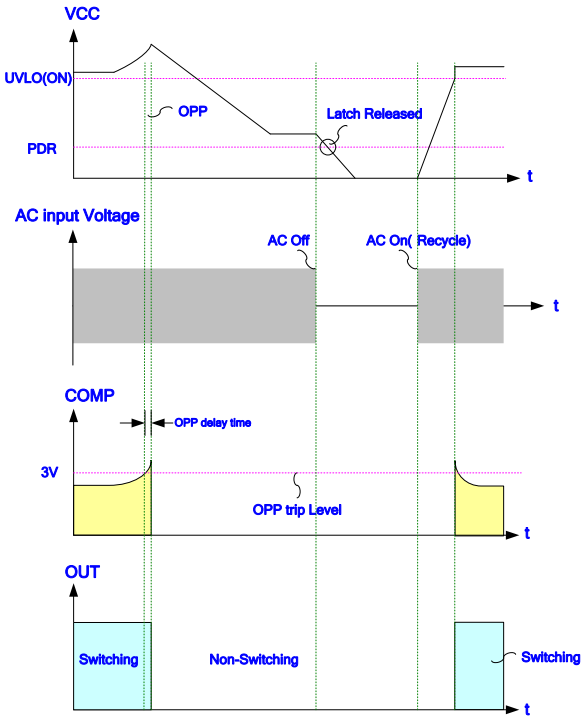


Fig. 17

Over Current Protection (OCP) – Latch

When the switching current is higher than the OCP threshold, the internal counter counts down. When the total accumulated counting time is more than 225ms, the controller triggers the OCP. This protection is latch protection.

Adjustable Over Current Compensation on FB Pin

For compensating the differential input current from high/low line conditions on current sensing resistor, LD5523M1 mirrors compensation current I_{OCP} from I_{FB} to CS pin. The relationship of compensation current I_{OCP} and I_{FB} is expressed by following equation and shown in Fig. 18.

$$I_{OCP} = K \times I_{FB}$$

, where $K = 0.75$

K is the mirror current ratio of FB pin, and the I_{OCP} follows the input voltage. When the V_{COMP} ramps up to the I_{OCP} threshold 0.55V, the compensation current is added gradually. The maximum value of I_{OCP} is generated as V_{COMP} is higher than 1.4V. The corresponding V_{COMP} and I_{OCP} are shown in Fig. 19.

The compensation current IOCP supplies an offset voltage by external resistor ROCP, which is series between the current sensing resistor RS and CS pin. By selecting a proper value of the resistor ROCP in series with the CS pin, the amount of compensation can be adjusted.

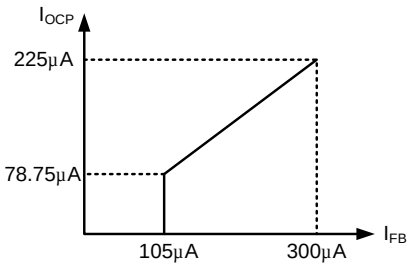


Fig. 18

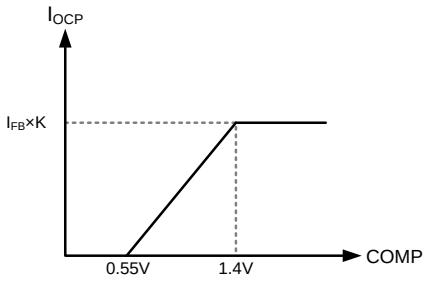


Fig. 19

Over Voltage Protection on FB Pin (FB OVP) – Latch

An output overvoltage protection is implemented in the LD5523M1. The auxiliary winding voltage can be reflected from secondary winding, in which the FB pin voltage is proportional to output voltage during the gate off time. OVP is worked by sensing the auxiliary voltage via the divided resistors R2, refereeing to Fig. 20. The equation of FB OVP is shown as follows.

$$R_2 = \frac{R_1 \cdot V_{FB\_OVP}}{V_a - V_{FB\_OVP}}$$

$$V_a = \frac{N_a}{N_S}(V_O + V_F)$$

,where

V_{DC_BNI} is predicted BNI DC value of input voltage.

V_{DC_BNO} is predicted BNO DC value of input voltage.

I_{BNI} is BNI trip current.

I_{BNO} is BNO trip current.

N_p is turns ration of primary-side winding.

N_a is turns ration of auxiliary winding.

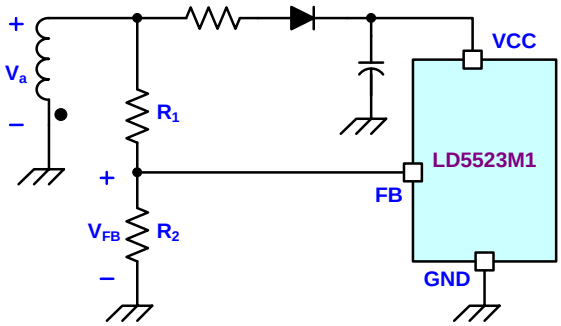


Fig. 20

V_{FB_OVP} is the FB pin OVP trip voltage level. V_a is the auxiliary winding voltage which reflects from the forward voltage V_F of schottky diode and output voltage V_O. N_S is turns ration of secondary-side winding.

If V_{FB} overs the FB OVP trip level, the internal counter starts counting 8 cycles, and then LD5523M1 goes to latch protection mode till VCC pin drops below PDR and starts AC-recycling again.

Over Temperature Protection on CS Pin (CS OTP) – Latch

LD5523M1 is implemented over temperature protection on CS pin which senses voltage to determine NTC status during gate off region. As V_{CS} is greater than 0.25*V_{FB} and continues for 5.4ms, CS_OTP is triggered, than LD5523M1 is in latch mode till the temperature drops to setting work condition, VCC pin drops below PDR and starts AC-recycling again.

Oscillator and Switching Frequency

The LD5523M1 is implemented with frequency swapping function which helps the power supply designers to both optimize EMI performance and lower system cost.

Secondary Diode Short Protection (SDSP) – Latch

The method that the LD5523M1 judges the logic of SDSP is described briefly as follows. When VCS is higher than 1.15V, it will reduce the frequency first, even the Ton < LEB+T_{PD}. When the count is up to 4 times, its gate will be turned-off, shown as Fig. 21.

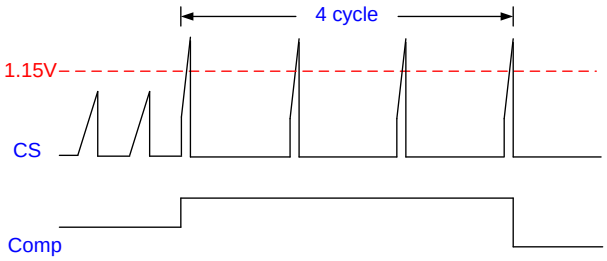


Fig. 21

Green Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property.

Fault Protection

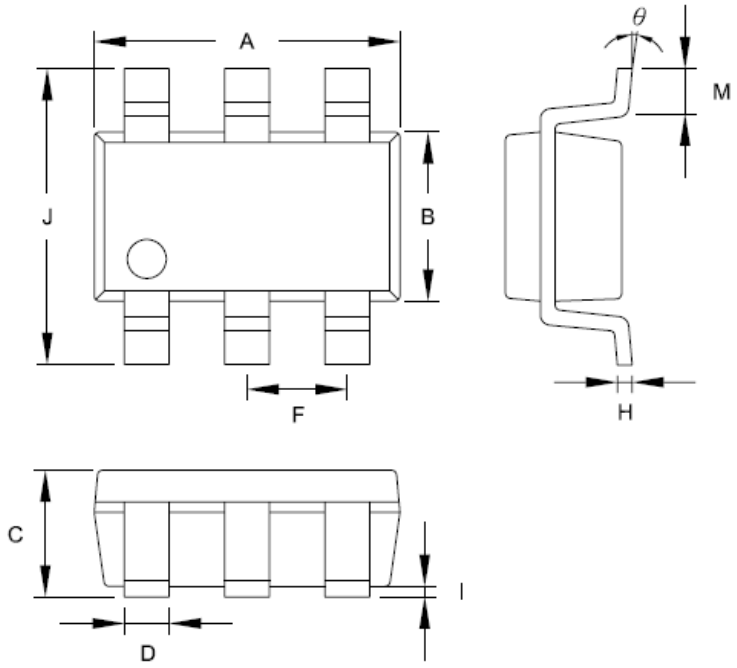
There are several critical protections integrated in the LD5523M1 to prevent from damage to the power supply. Those damages usually come from open or short conditions on the pins of LD5523M1.

In case under such conditions listed below, the gate output will turn off immediately to protect the power circuit.

1. CS pin floating
2. COMP pin floating

Package Information

SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Revision History

REV.	Date	Change Notice
00	04/12/2021	Original Specification

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice.

Customers should verify the datasheets are current and complete before placing order.