Multi-Mode PWM Controller of Flyback with MOSFET Integrated

REV. 00

General Description

The LD5523T is built in a multi-mode PWM controller. The multi-mode PWM controller which consists of Quasi-Resonant (QR) PWM control for light load condition and Continue Conduction Mode (CCM) for heavy load condition. Moreover, the QR controller not only gains the system performance, but also brings the worse EMI capability, while the frequency swapping function of LD5523T can reduce the EMI emission of SMPS and helps the power circuit designers to simply deal with EMI filter and saves several component and developing time.

The LD5523T is implemented in SOT-26 package, and includes the comprehensive protection function, such as Over Load Protection (OLP), Over Voltage Protection (OVP), Output Short Circuit Protection (OSCP) and internal Over Temperature Protection (OTP).

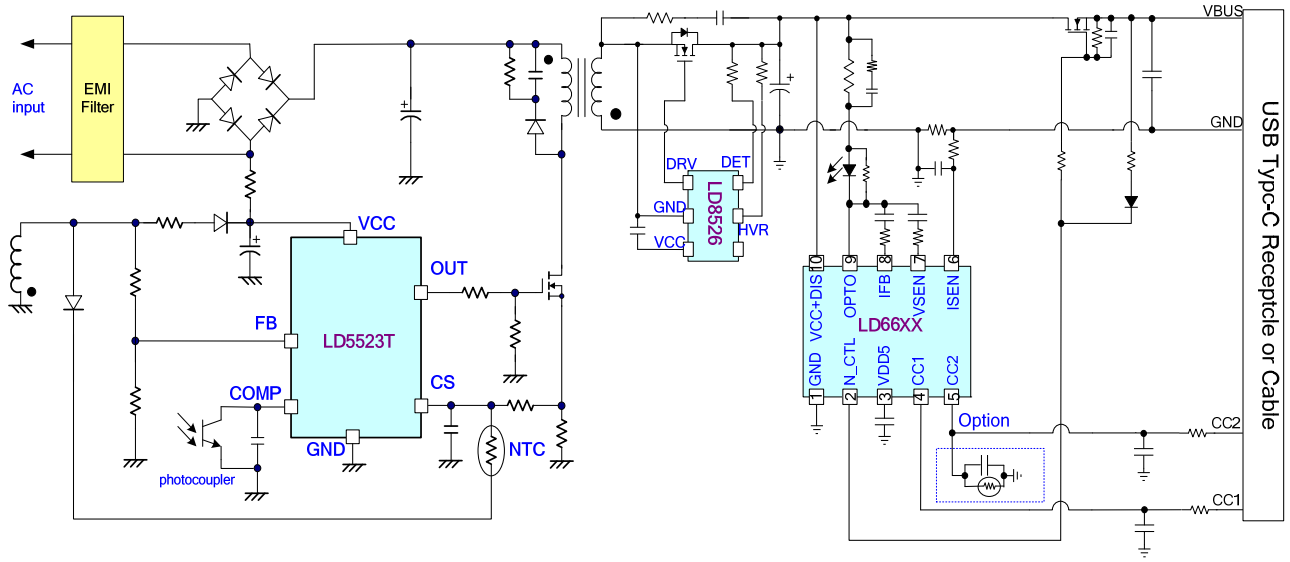
Features

- Secondary-side feedback control with quasi-resonant + CCM operation
- Low Startup Current (<1μA)
- Ultra-low operating current at light load
- Cycle-by-Cycle Current Limit
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- VCC OVP (Over Voltage Protection)
- Adj. OVP (Over Voltage Protection) on FB pin.
- Adj. UVP (Under Voltage Protection) on FB pin.
- OLP (Over Load Protection)
- Internal OTP (Over Temperature Protection)

Applications

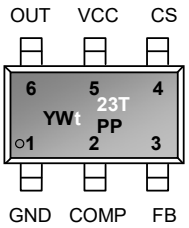
- Switching AC/DC Adaptor
- Open Frame Switching Power Supply

Typical Application



Pin Configuration

SOT-26 (TOP VIEW)



Y : Year code (D: 2004, E: 2005…..)
W : Week code
PP : Production code
t23T : LD5523T

Ordering Information

Part number	Package		TOP MARK	Shipping
LD5523T GL	SOT-26	(Green Package)	YWt/23T/PP	3000 /tape & reel

The LD5523T is RoHs compliant/ green packaged.

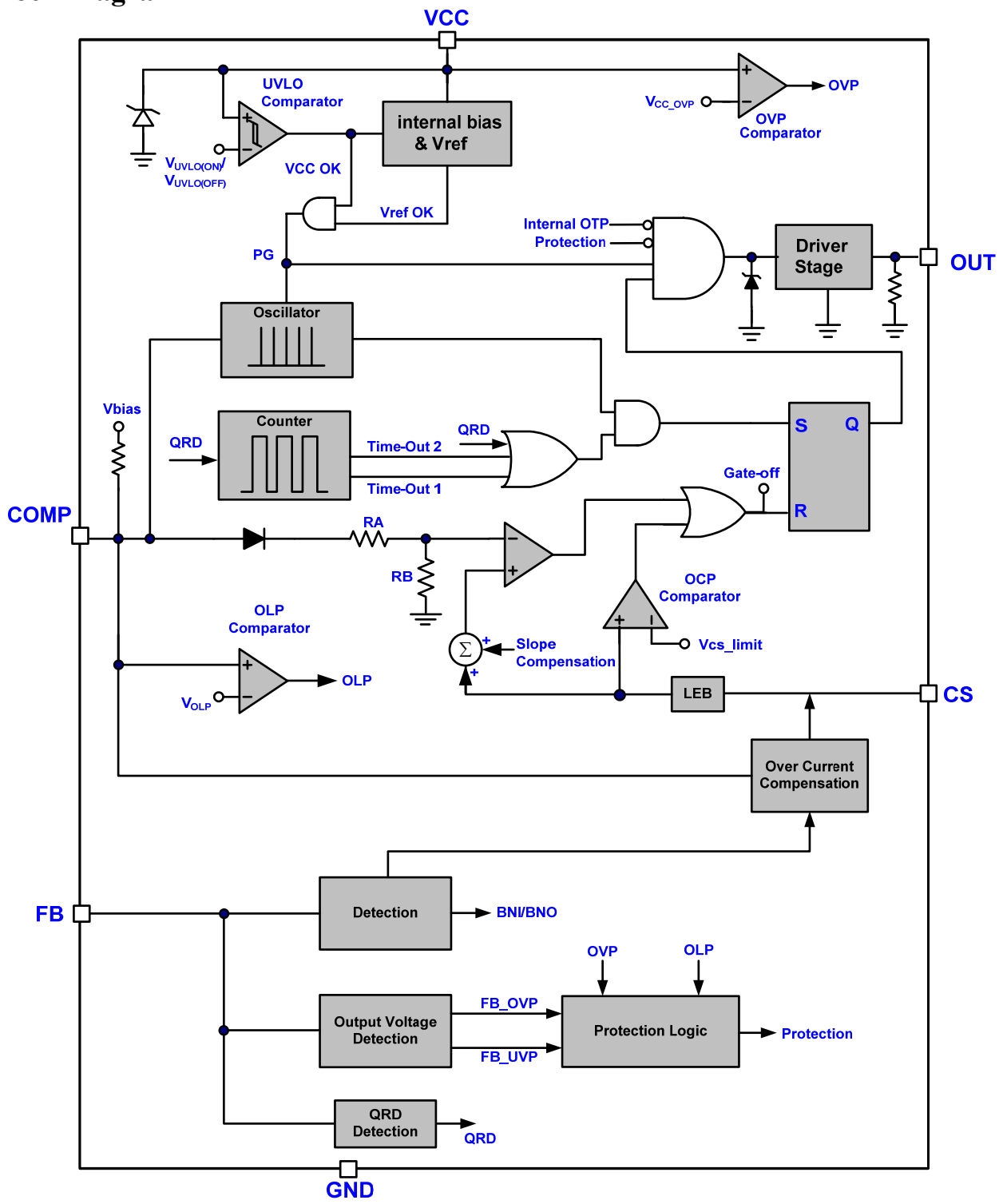
Protection Mode

Product Name	Switching Freq.	VCC_OVP	FB_OVP	OSCP	OLP	FB_UVP	Int. OTP
LD5523T	65kHz	Auto recovery	Auto recovery	Auto recovery	Auto recovery	Auto recovery	Auto recovery

Pin Descriptions

NAME	PIN (SOT-26)	FUNCTION
GND	1	Ground
COMP	2	Output of the error amplifier for voltage compensation
FB	3	Auxiliary voltage sense, brown in/out and Quasi Resonant detection
CS	4	Current sense pin, connect to sense the MOSFET current
VCC	5	Supply voltage pin
OUT	6	Gate drive output to drive the external MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V ~ 30V
COMP	-0.3V ~ 12V
FB, CS	-0.3V ~ 6.5V
OUT	-0.3V ~ VCC+0.3V
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	200°C/W
Package Thermal Resistance (SOT-26, θ_{JC})	115°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	200mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (Except Drain Pin)	2.5 KV
ESD Voltage Protection, Human Body Model (Drain Pin)	1 KV
ESD Voltage Protection, Machine Model (Except Drain Pin)	250 V
ESD Voltage Protection, Machine Model (Drain Pin)	200 V

Note1: The value of θ_{JA} is measured with the device mounted on 1oz one layer FR-4 board, in a still air environment with TA = 25°C. The value in any given application depends on the user's specific board design.

Note2: When COMP/CS/FB pin negative spike voltage < -2V, the time must be < 200ns at every duty cycle which typical value is 15.4μs. (The state of note 2 simply happens when user's system is designed according to the application information.)

Caution:

Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stress above recommended operating conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.0	26.5	V
VCC Capacitor	3.3	10	μF
Start-up resistor Value (AC Side, Half Wave)	400K	2M	Ω
Comp Pin Capacitor (X7R type)	330	4700	pF
CS Pin Capacitor Value	-	30	pF
Current Sense Resistor	0.25	-	Ω

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF ~ 0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible.
2. It's also essential to connect a capacitor to COMP to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current		I_{CC_ST}			1	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V	I_{CC_OP1}		0.295		mA
	V_{COMP}=1.7V,I_{FB}=200μA	I_{CC_OP2}		1.95		mA
	Auto current protection	I_{CC_OPA1}		0.6		mA
UVLO(OFF)		V_{CC_OFF}	5.3	6.3	7.3	V
UVLO(ON)		V_{CC_ON}	15.5	16.5	17.5	V
VCC OVP Level		V_{CC_OVP}	30	31	31.9	V
VCC OVP de-bounce time		T_{VCC_OVP}	6	8	10	Cycle
Voltage Feedback (COMP Pin)						
Short Circuit Current	V_{COMP}=0V	I_{COMP}	0.08	0.116	0.15	mA
Open Loop Voltage	(1)	V_{COMP_OPEN}	3	3.15	3.3	V
Current Sensing (CS Pin)						
Maximum Input Voltage		V_{CS_LIMIT}	0.45	0.5	0.55	V
Leading Edge Blanking Time		T_{LEB}	270	450	630	ns
Internal Slope Compensation	*ton>3μs to D_{MAX}. (Linearly increase) (1)	V_{SLP_L}		165		mV
QRD (Quasi Resonant Detection, FB Pin)						
FB OVP Trip voltage Level	During soft-start	V_{FB_OVP}		1.25		V
FB OVP Trip voltage Level	After soft-start (1)	V_{FB_OVP}	2.65	2.85	3.05	V
FB UVP Trip voltage Level		V_{FB_UVP}		0.85		V
FB UVP 1 De-bounce Time	After start-up +15ms (1)	T_{FB_UVP1}		8		Cycle
FB UVP 2 De-bounce Time	After start-up +15ms (1)	T_{FB_UVP2}		6		Cycle
QRD Trip Level	(1)	I_{QRD}		20		μA
Oscillator for Switching Frequency						
CCM Frequency		F_{CCM}	60	65	70	kHz
Frequency Swapping	(1)	F_{SW_MOD}		±8		%
Green Mode Frequency		F_{SW_GREEN}	21	24	27	kHz
Temp. Stability	(1)	F_{SW_TS}		3	5	%
Voltage Stability	VCC =9V~24V(1)	F_{SW_VS}			1	%
Maximum Duty	(1)	D_{MAX}		81		%

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Soft Start						
Soft Start Time	V_{CS_OFF} from 0.2V to 0.5V(1)	T_{SS}		7		ms
BNO Protection (FB Pin)						
Brown In Trip Level		I_{BNI}	85	95	105	μA
BNO Hysteresis		I_{BNO_HYS}		10		μA
Brown Out De-bounce Time	V_{COMP}=1.7V	T_{DB_BNO}		70		ms
Open Loop Protection						
OLP Trip Level		V_{OLP}	2.65	2.8	2.95	V
OLP delay time	After soft-start	T_{D_OLP}	60	88	116	ms
On Chip OTP (Over Temperature Protection)						
OTP Level	(1,2)	T_{INOTP}		140		°C
OTP Hysteresis	(1,2)	T_{INOTP_HYS}		12		°C

Notes:
1. Guaranteed by design.
2. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.

Typical Performance Characteristics

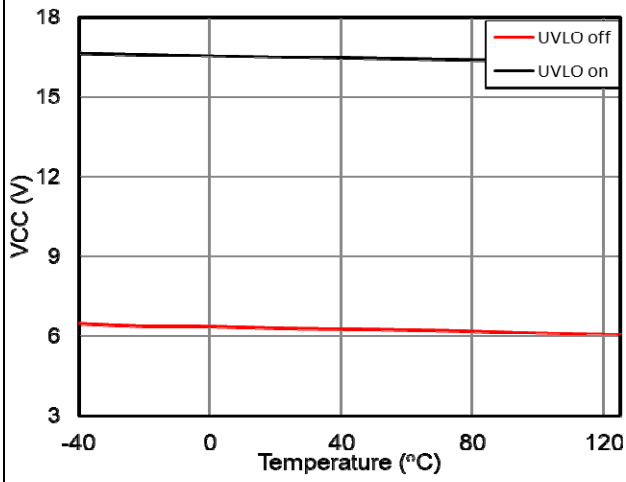


Fig 1. UVLO Level vs. Temperature

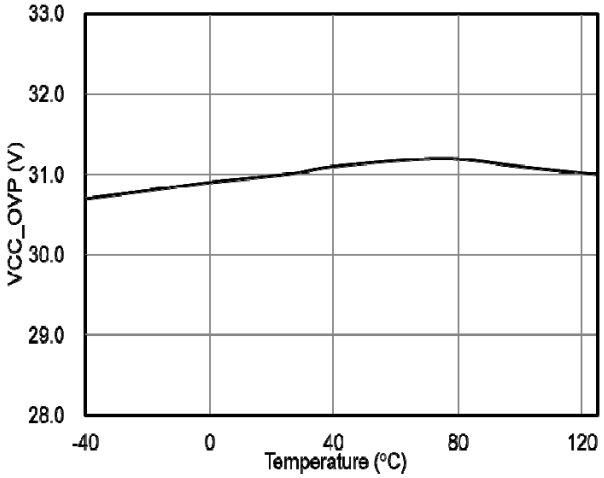


Fig 2. Vcc OVP Level vs. Temperature

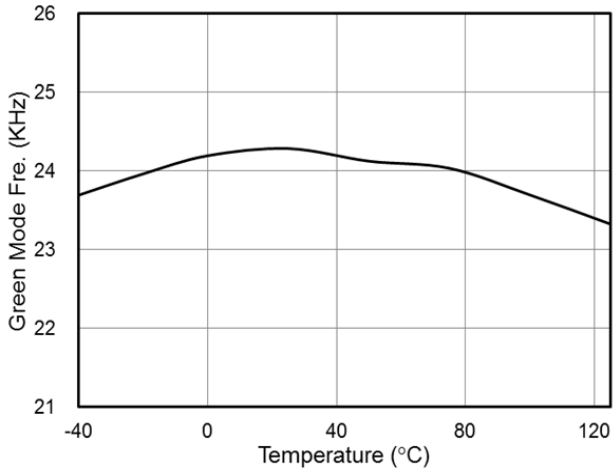


Fig 3. Green Mode Fre. vs. Temperature

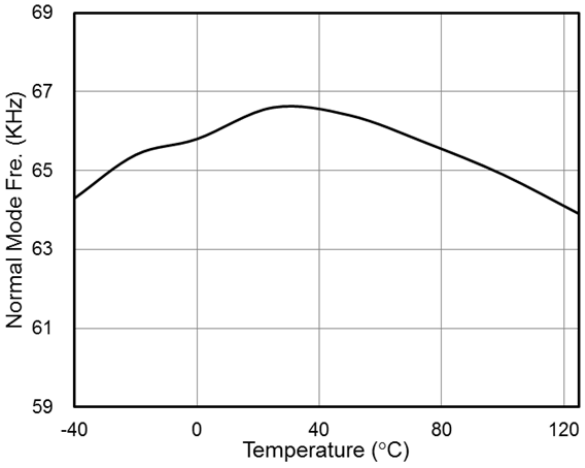


Fig 4. Normal Mode Fre. vs. Temperature

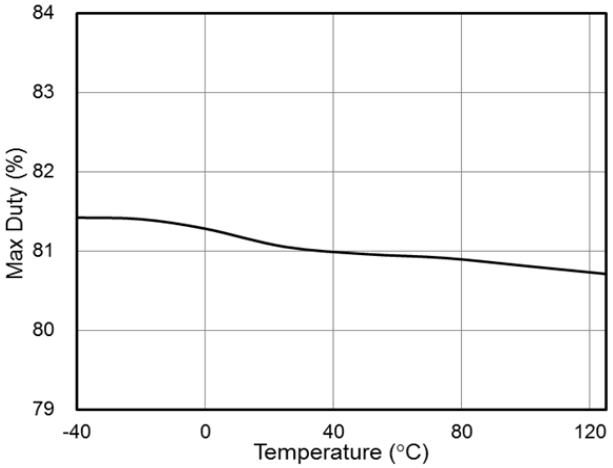


Fig 5. Max Duty vs. Temperature

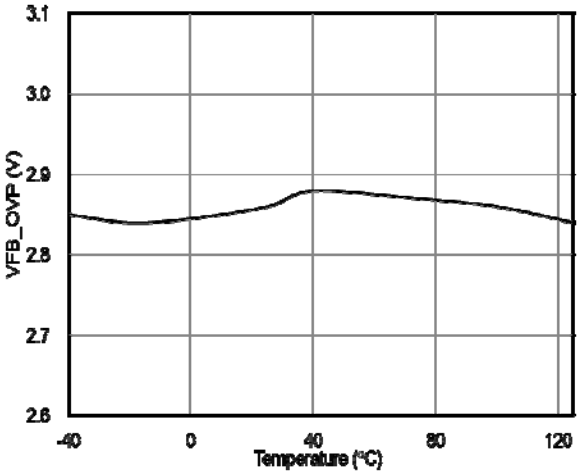


Fig 6. FB OVP Level (After SS) vs. Temperature

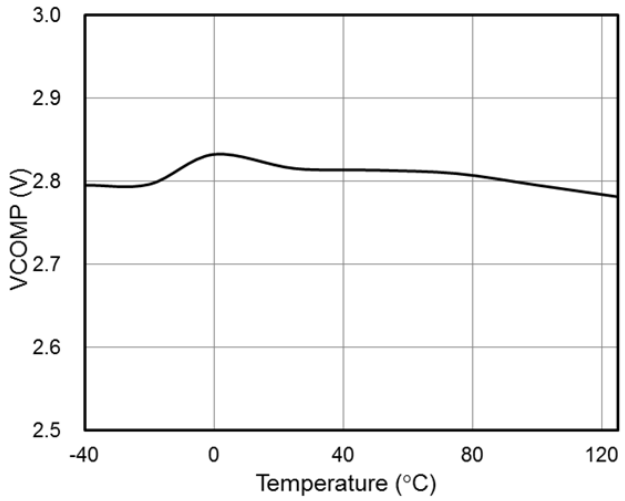


Fig 7. VOLP Level vs. Temperature

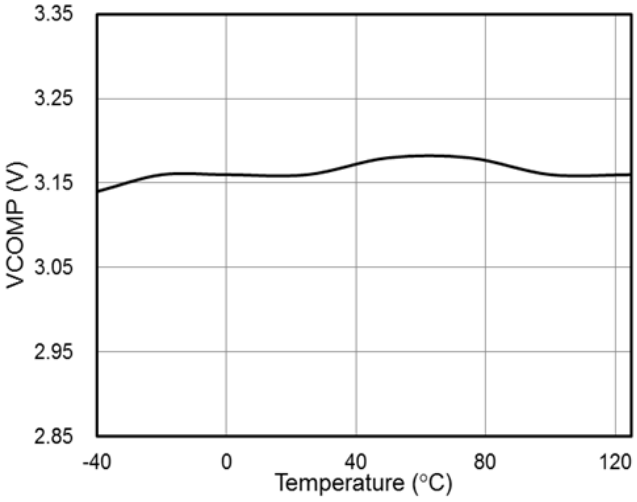


Fig 8. Open Loop Voltage vs. Temperature

Application Information

Operation Overview

The LD5523T is built in a multi-mode PWM controller. The LD5523T operates a constant frequency to achieve the CCM as heavy load. For demanding higher power efficiency and power-saving in light load condition, the LD5523T implements QR function to allow the valley switching and accomplish zero voltage switching (ZVS). Under different load conditions, LD5523T provides the different solutions for achieving higher efficiency and performance.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD5523T. As shown in Fig. 9, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.5V and 6.3V, respectively.

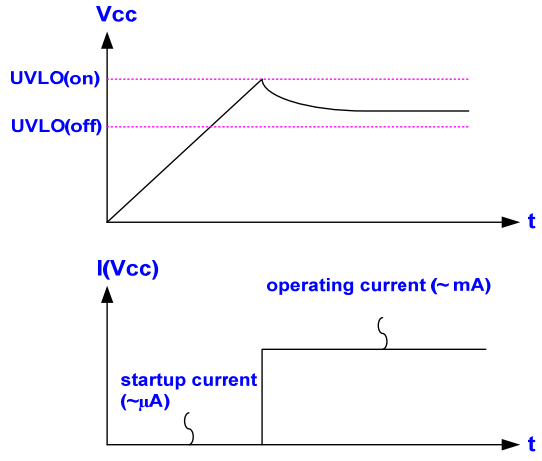


Fig. 9

Startup Current and Startup Circuit

The typical startup circuit to generate the LD5523T VCC is shown in Fig. 10. During the startup transient, the VCC is lower than the UVLO threshold thus LD5523T will not to turn on. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the VCC voltage is high enough to turn on the LD5523T the supply current is provided from the auxiliary winding of the transformer.

Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD5523T is only 1μA. If a higher resistance value of R1 is chosen, it usually takes more time to start up. To select the value of R1 and C1 carefully will optimize the power consumption and startup time.

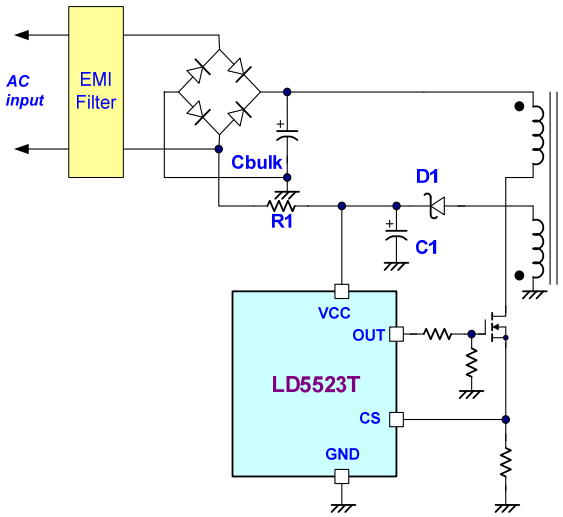


Fig. 10

QR Mode Detection

The transformer will be demagnetized after the main power MOSFET turns off. A quasi resonant signal will be detected from auxiliary winding by FB pin through the external resister.

As soon as the current of the secondary side diode is down to zero during MOSFET-off period, the transformer's core is demagnetized completely. V_{DS} of MOSFET will resonate in discontinuous current mode. The resonance frequency (F_{QR}) will be obtained as below.

$$F_{QR} = \frac{1}{2\pi\sqrt{L_m \times C_R}} (HZ)$$

L_M = Inductance of primary winding
C_R = Resonance equivalent parasitic capacitance
If V_{DS} voltage falls to resonant valley level from max plateau value, the QRD comparator will be tripped while FB pin current is close to 20μA.

However, the QR detection will be influenced by propagation delay. If inductance of primary winding is less than 500μH, there is barb in Vds (as shown in Fig. 11).

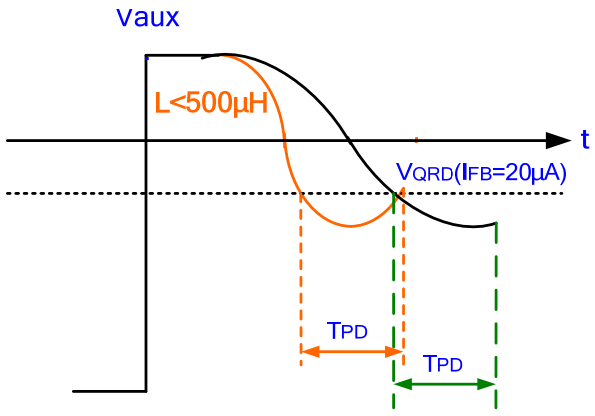


Fig. 11

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD5523T. Similar to UC3842, the LD5523T would without voltage offset to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{R_A}{R_A + R_B} \times V_{COMP}$$

A pull-high resistor is embedded internally and therefore no external one is required.

The LD5523T integrates the multi-mode PWM controller, and for enhance the light load efficiency, the comp pin value corresponding to the frequency is as shown in Fig. 12.

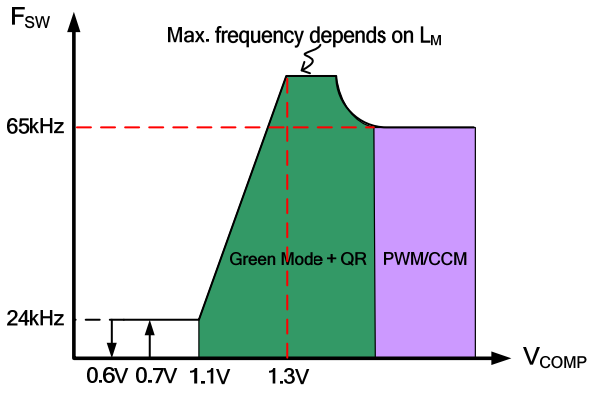


Fig. 12

Current Sensing, Leading Edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD5523T detect the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin sets at 0.5V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.5V}{R_{CS}}$$

A 450ns leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spike is less than 450ns and the negative spike on the CS pin doesn't exceed -0.3V, it could remove the R-C filter (as shown in the Fig. 13).

However, the total pulse width of the turn-on spike is decided by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in Fig. 14) for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

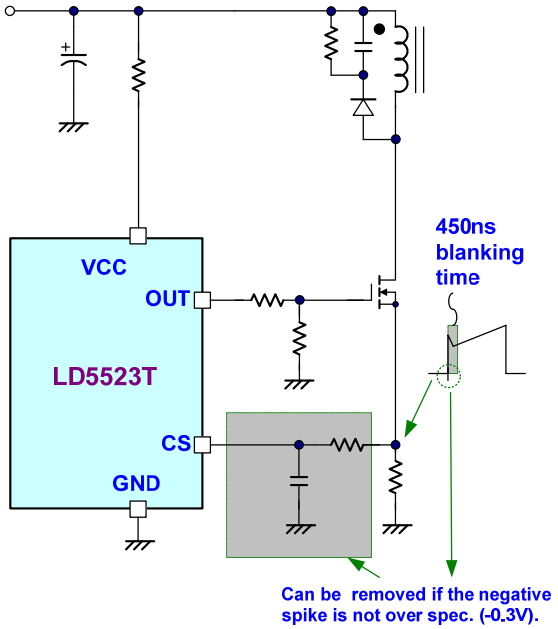


Fig. 13

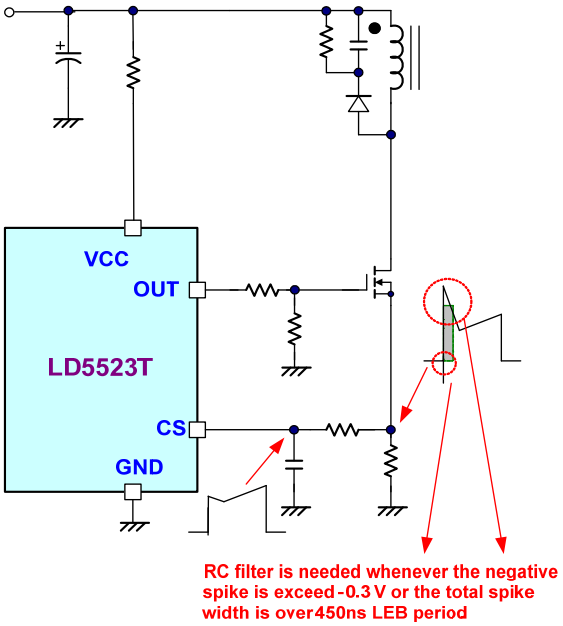


Fig. 14

CCM Switching Frequency Clamp

According to the QR operation principle, the switching frequency is inversely proportional to the output power. Therefore, as the output power increases, the switching frequency can become rather low without limiting. The CCM switching frequency of LD5523T is clamped at 65 kHz internally to provide the optimized operations by considering the EMI performance, thermal treatment, component sizes and transformer design.

Over Voltage Protection on VCC Pin (VCC OVP) – Auto Recovery

LD5523T is implemented with an OVP function on VCC. Whenever the VCC voltage is higher than the OVP threshold voltage, the LD5523T will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(ON).The VCC OVP function in LD5523T is an auto-recovery type protection. The Fig. 15 shows its operation.

On the other hand, if the OVP condition is removed, the VCC level will get back to normal level and the output will automatically return to the normal operation.

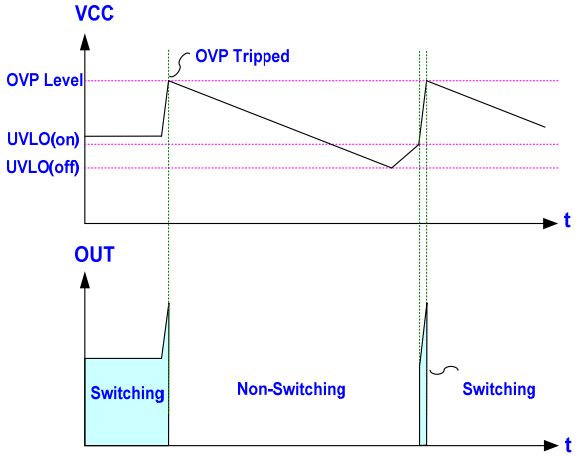


Fig. 15

Over Load Protection (OLP) – Auto Recovery

To protect the circuit from damage due to over-load condition and short or open-loop condition, the LD5523T is implemented with smart OLP function. It also features auto –recovery function, see Fig. 16 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the V_{COMP} ramps up to the OLP threshold of 2.8V and continues over OLP delay time, the protection will be activated and

then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

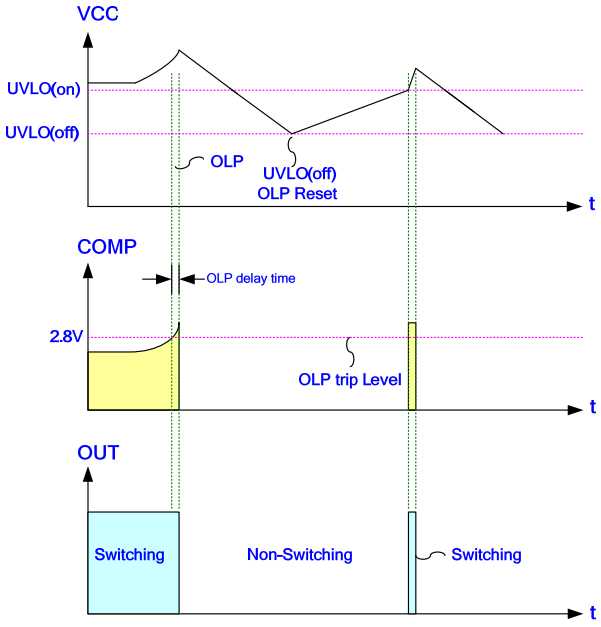


Fig. 16

Over Voltage Protection on FB Pin (FB OVP) – Auto Recovery

An output overvoltage protection is implemented in the LD5523T. The auxiliary winding voltage can be reflected from secondary winding, in which the FB pin voltage is proportional to output voltage during the gate off time. OVP is worked by sensing the auxiliary voltage via the divided resistors R2, refereeing to Fig. 17. The equation of FB OVP is shown as follows.

$$R_2 = \frac{R_1 \cdot V_{FB\_OVP}}{V_a - V_{FB\_OVP}}$$

$$V_a = \frac{N_a}{N_S}(V_O + V_F)$$

V_{FB_OVP} is the FB pin OVP trip voltage level. V_a is the auxiliary winding voltage which reflects from the forward voltage V_F of Schottky diode and output voltage V_O. N_S is turns ration of secondary-side winding.

If V_{FB} overs the FB OVP trip level, the internal counter starts counting 8 cycles, and then LD5523T goes to auto-recovery protection mode till the FB OVP status is defused.

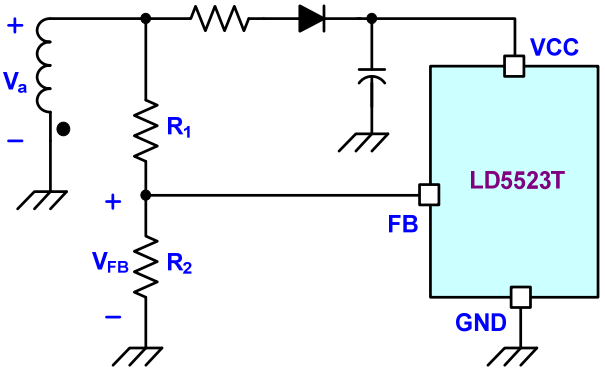


Fig. 17

Under Voltage Protection 1 on FB Pin (FB UVP 1) – Auto Recovery

The FB UVP 1 function can prevent the damage from output short circuit. Once the output is shorted, Vo drop immediately. According to the close loop control, COMP voltage will pull high in the meanwhile. Therefore, as V_{FB} is lower than FB UVP trip level during gate off region and VCOMP pulls higher than 2.8V over 8 cycles, then the FB UVP 1 will be activated to stop the switching of the power MOSFET until the next UVLO(on). The Fig. 18 shows its operation.

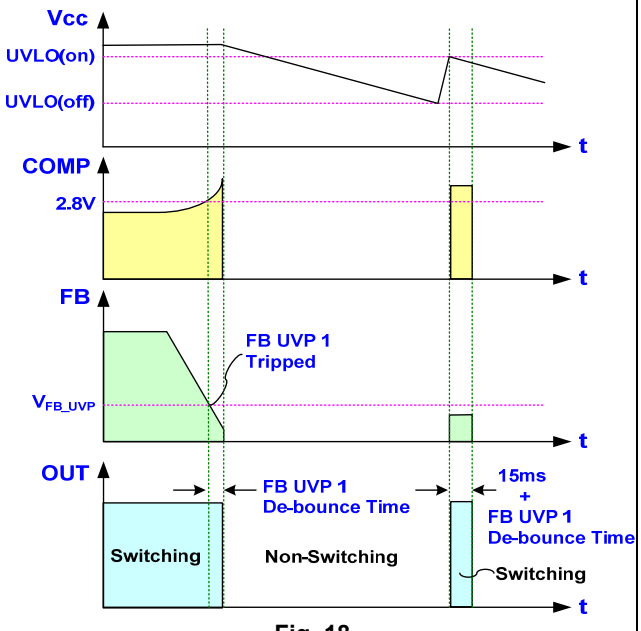


Fig. 18

Under Voltage Protection 2 on FB Pin (FB UVP 2) – Auto Recovery

To protect the circuit from damage due to output under voltage condition, LD5523T is implemented with an UVP function on FB pin. The output voltage is detected by PD controller, if output voltage falls to PD UVP level in abnormal condition, PD controller will control output voltage to drop immediately. The FB pin voltage is proportional to output voltage during the gate off time. Therefore, as VFB is lower than FB UVP trip level during gate off region over 6 cycles, then the FB UVP 2 will be activated to stop the switching of the power MOSFET until the next UVLO(on). The Fig. 19 shows its operation.

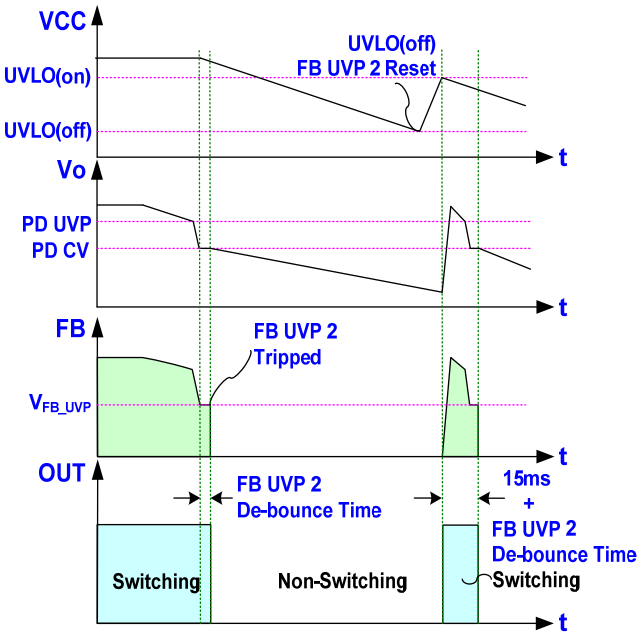


Fig. 19

Output Short Circuit Protection (OSCP) – Auto Recovery

The OSCP function can prevent the damage from output short circuit. Once the output is shorted, Vo and V_{CC} drop immediately. According to the close loop control, COMP voltage will pull high in the meanwhile. The auxiliary winding voltage can be reflected from secondary winding, in which the FB pin voltage is proportional to output voltage during the gate off time. Therefore, VFB also drops during gate off region. At this time, the OSCP protection will be triggered and turn off the gate driving.

Oscillator and Switching Frequency

The LD5523T is implemented with frequency swapping function which helps the power supply designers to both optimize EMI performance and lower system cost.

Green Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property.

Fault Protection

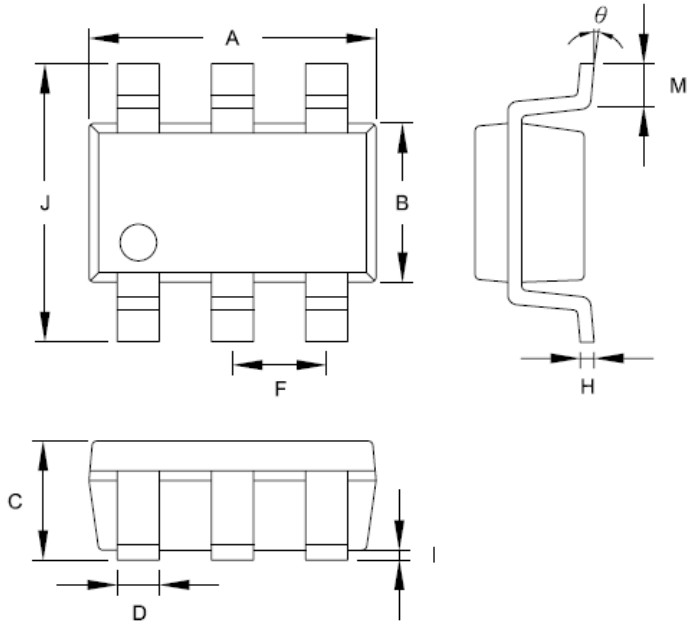
There are several critical protections integrated in the LD5523T to prevent from damage to the power supply. Those damages usually come from open or short conditions on the pins of LD5523T.

In case under such conditions listed below, the gate output will turn off immediately to protect the power circuit.

1. CS pin floating
2. COMP pin floating

Package Information

SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Revision History

REV.	Date	Change Notice
00	04/08/2021	Original Specification.