Multi-Mode PWM Controller of Flyback with Integrated BNI/BNO and Protection

REV. 00

General Description

In order to enhance the efficiency performance, the LD5525 integrates the multi-mode PWM controller, which consists of Quasi-Resonant (QR) PWM control for light load condition and Continue Conduction Mode (CCM) for heavy load condition. Moreover, the QR controller not only gains the system performance, but also brings the worse EMI capability, while the frequency swapping function of LD5525 can reduce the EMI emission of SMPS and helps the power circuit designers to simply deal with EMI filter and saves several component and developing time.

The LD5525 is implemented in SOT-26 package, and includes the comprehensive protection function, such as Over Load Protection (OLP), Over Voltage Protection (OVP), Output Short Circuit Protection (OSCP) and internal Over Temperature Protection (OTP). Furthermore, the programmable Brown-in/out Protection is built-in.

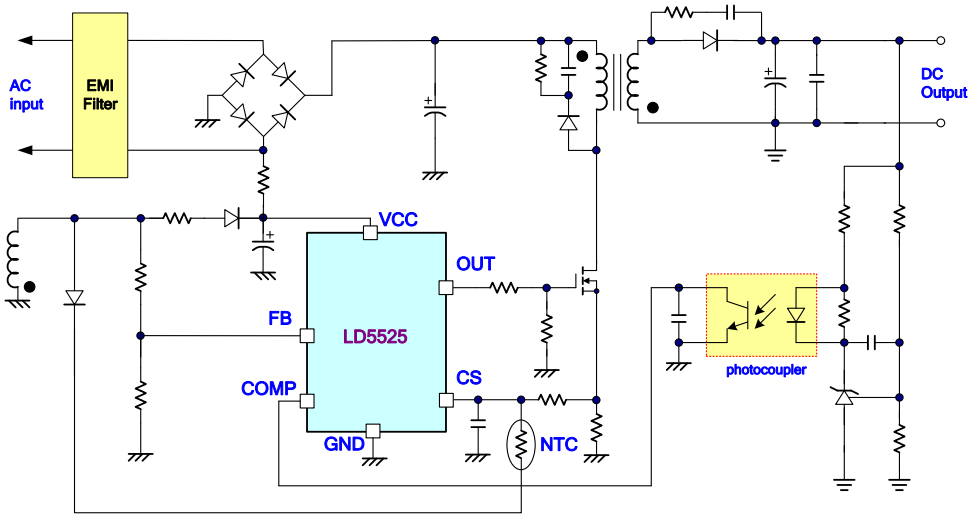
Features

- Secondary-side feedback control with quasi-resonant operation
- Low Startup Current (<3μA)
- 0.5mA Ultra-low operating current at light load
- Current Mode Control with Cycle-by-Cycle Current Limit
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- VCC OVP (Over Voltage Protection)
- Adj. OVP (Over Voltage Protection) on FB pin.
- Adj. UVP (Under Voltage Protection) on FB pin.
- Adjustable Brown in/out on FB pin.
- OLP (Over Load Protection)
- External OTP (Over Temperature Protection) on CS Pin
- Internal OTP (Over Temperature Protection)
- Gate Source/Sink Capability: 250mA/-500mA

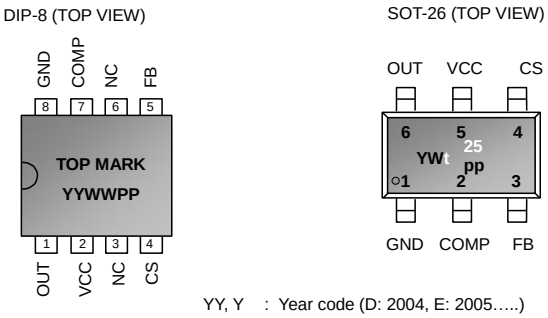
Applications

- Switching AC/DC Adaptor

Typical Application



Pin Configuration



YY, Y : Year code (D: 2004, E: 2005…..)
WW, W : Week code
PP : Production code
T25 : LD5525

Ordering Information

Part number	Package		TOP MARK	Shipping
LD5525 GL	SOT-26	(Green Package)	YWt/25	3000 /tape & reel
LD5525 GN	DIP-8	(Green Package)	LD5525 GN	3600 /tube /Carton

The LD5525 is ROHS compliant/Green Packaged.

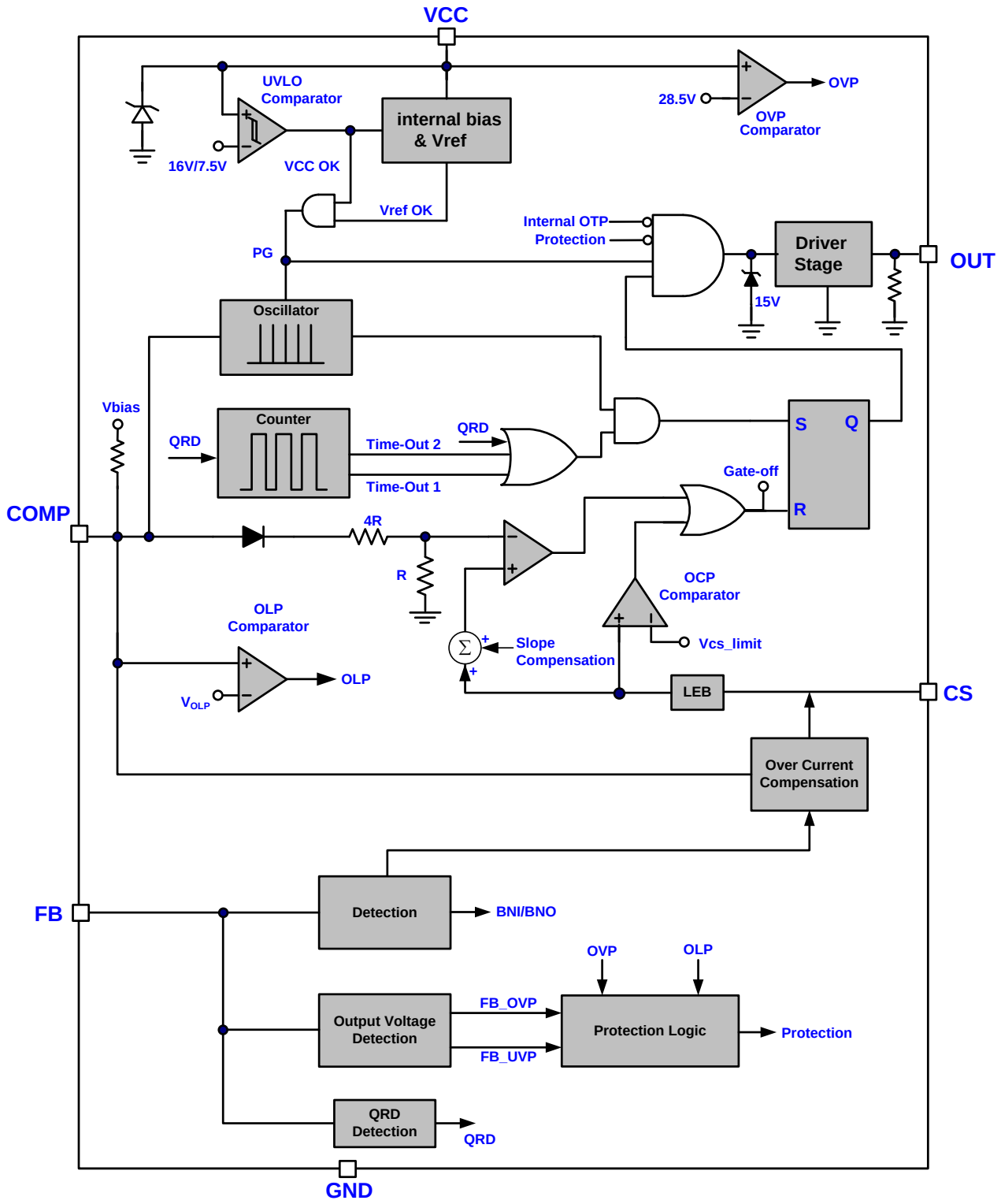
Protection Mode

Switching Freq.	VCC OVP	FB_OVP	FB_UVP	OLP	BNI/BNO	CS_OTP
85kHz/65kHz	Auto recovery	Auto recovery	Auto recovery/80ms	Auto recovery/80ms	Auto recovery	Auto recovery

Pin Descriptions

NAME	PIN (SOT-26)	Pin (DIP-8)	FUNCTION
GND	1	8	Ground
COMP	2	7	Output of the error amplifier for voltage compensation
FB	3	5	Auxiliary voltage sense, brown in/out and Quasi Resonant detection
CS	4	4	Current sense pin, connect to sense the MOSFET current
VCC	5	2	Supply voltage pin
OUT	6	1	Gate drive output to drive the external MOSFET
NC		3	
NC		6	

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC,	-0.3V ~ 30V
OUT	-0.3V ~ VCC
COMP, FB, CS	-0.3V ~ 7V
Operating Ambient Temperature	-20°C ~ 85°C
Operating Junction Temperature	-40°C ~ 125°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	200°C/W
Package Thermal Resistance (DIP-8, θ_{JA})	100°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	200mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	400mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V
Gate Output Current	250mA/-500mA

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Ambient Temperature	-40	85	°C
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.0	26.5	V
VCC Capacitor	3.3	10	μF
Start-up resistor Value (AC Side, Half Wave)	400K	2M	Ω
Comp Pin Capacitor	1	10	nF
CS Pin Capacitor Value	47	470	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF ~ 0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. It's also essential to connect a capacitor to COMP to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current		I_{CC_ST}			3	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V, OUT=1nF	I_{CC_OP1}		0.5		mA
	V_{COMP}=3V, OUT=1nF	I_{CC_OP2}		1.5		mA
	OVP/OLP Tripped/ Auto	I_{CC_OPA1}		0.5		mA
	Brown in / Start-up (Before the first pulse)	I_{CC_OPA3}		0.75		mA
	Brown out / Auto	I_{CC_OPA4}		0.45		mA
UVLO(OFF)		V_{CC_OFF}	7.0	7.5	8.0	V
UVLO(ON)		V_{CC_ON}	15	16	17	V
VCC OVP Level		V_{CC_OVP}	27.5	28.5	29.5	V
VCC OVP de-bounce time		N_{TD_VCCOVP}		8		Cycle
Voltage Feedback (COMP Pin)						
Short Circuit Current	V_{COMP}=0V	I_{COMP}	0.1	0.125	0.15	mA
Open Loop Voltage		V_{COMP_OPEN}	4.9	5.2	5.5	V
Maximum Frequency Mode	(1)	V_{COMP_Fmax}		2.2		V
Green Mode Threshold	(1)	V_G		1.8		V
Burst Mode		V_{ZDC}	1.4	1.5	1.6	V
	Hysteresis	V_{ZDCH}		100		mV
Min. OCP Compensation Current	I_{FB} =I_{BNI} (1)	I_{OCP_MIN}		47.5		uA
Max. OCP Compensation Current	(1)	I_{OCP_MAX}		200		uA
Green mode operation switch		I_{GM}		200		uA
Current Sensing (CS Pin)						
Maximum Input Voltage	I_{FB} <I_{GM}	$V_{CS\_LIMIT\_LL}$	0.49	0.52	0.55	V
	I_{FB} >I_{GM}	$V_{CS\_LIMIT\_HL}$	0.54	0.57	0.60	V
Leading Edge Blanking Time		T_{LEB}	250	350	450	ns
Internal Slope Compensation	*ton>3us to D_{MAX}. (Linearly increase), (1)	V_{SLP_L}		170		mV
Delay to Output		T_{PD}		80		ns

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
QRD (Quasi Resonant Detection, FB Pin)						
OVP Trip voltage Level		V_{FB_OVP}	3.4	3.5	3.6	V
OVP De-bounce Cycle		N_{TFB_OVP}		8		Cycle
UVP Trip voltage Level	(1)	V_{FB_UVP}		1		V
QRD Trip Level	(1)	V_{QRD}		100		mV
QRD Delay Time	(1)	T_{QRD}		100		ns
QR Mode Time Out 1		T_{OUT1}		5		µs
Max Frequency Clamp Time Out 2		T_{OUT2}	100	150	200	µs
BNO Protection (FB Pin)						
Brown In Trip Level		I_{BNI}	85	95	101.5	µA
Brown Out Trip Level		I_{BNO}	79	85	93.5	µA
BNO_hys		I_{BNO_HYS}	6			µA
Brown Out De-bounce Time	V_{COMP}=3V	T_{DB_BNO}		60		ms
OTP (Over Temperature, CS Pin)						
CS OTP Level		V_{CSOTP}		0.5		V
CS OTP de-bounce time		T_{D_CSOTP}		8		Cycle
Oscillator for Switching Frequency						
QR Maximum Frequency	I_{FB} <I_{GM}	$F_{QR\_MAX\_LL}$	121	130	139	kHz
	I_{FB} >I_{GM}	$F_{QR\_MAX\_HL}$	79	85	91	kHz
CCM Frequency	I_{FB} <I_{GM}, (1)	F_{CCM_LL}	79	85	91	kHz
	I_{FB} >I_{GM}, (1)	F_{CCM_HL}	60	65	70	kHz
Frequency Swapping		F_{SW_MOD}		±6		%
Green Mode Frequency		F_{SW_GREEN}		25	27	kHz
Temp. Stability		F_{SW_TS}		3	5	%
Voltage Stability	VCC =9V~24V	F_{SW_VS}			1	%
Maximum ON Time						
Maximum On Time		T_{ON_MAX}		15		µs
Gate Drive Output (OUT Pin)						
Output Low Level	VCC =15V, Io=20mA	V_{OL}			1	V
Output High Level	VCC =15V, Io=20mA	V_{OH}	8		13	V
Rising Time	VCC =15V C_L=1000pF	T_r		200	350	ns
Falling Time	VCC =15V C_L =1000pF	T_f		80	150	ns
Output High Clamp Level	VCC =18V	V_{O_CLAMP}		13.5		V

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Soft Start						
Soft Start Time	V_{CS_OFF} from 0.2V to 0.5V	T_{SS}		5		ms
Open Loop Protection						
OLP Trip Level		V_{OLP}	4.3	4.5	4.7	V
OLP delay time	After soft-start	T_{D_OLP}	72	80	88	ms
On Chip OTP (Over Temperature)						
OTP Level	(1,2)	T_{INOTP}		140		°C
OTP Hysteresis	(1,2)	T_{INOTP_HYS}		30		°C

Notes:
1. Guaranteed by design.
2. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.

Typical Performance Characteristics

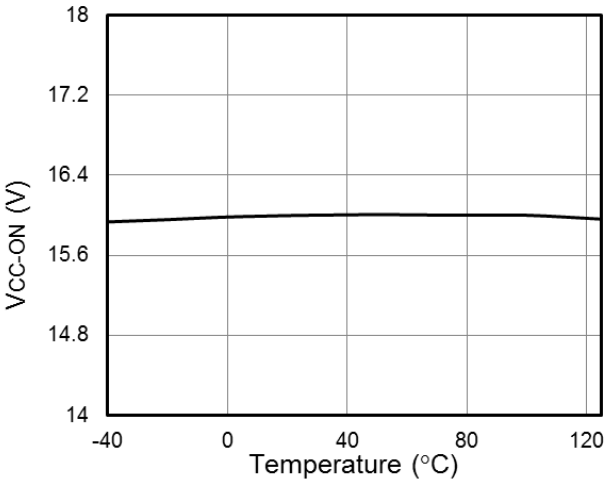


Fig. 1 UVLO on level vs.Temperature

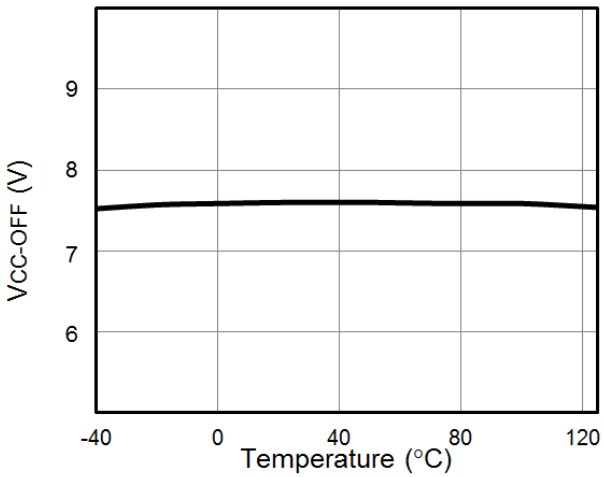


Fig. 2 UVLO off level vs.Temperature

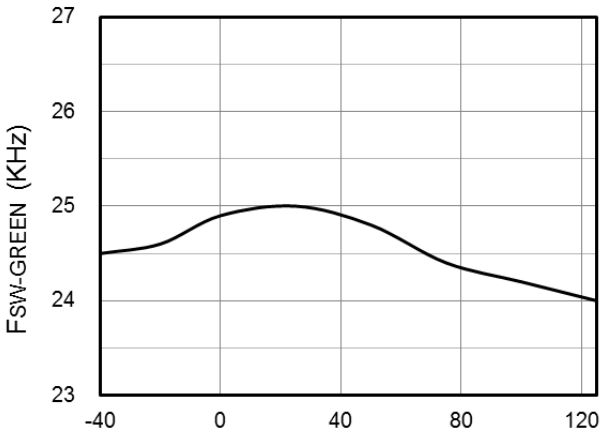


Fig. 3 Green Mode Frequency vs.Temperature

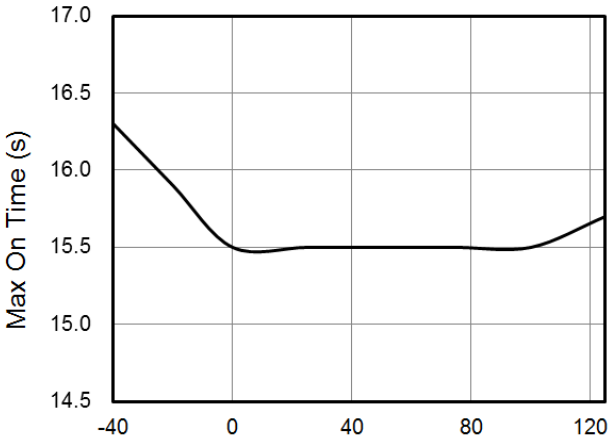


Fig. 4 Max On Time vs.Temperature

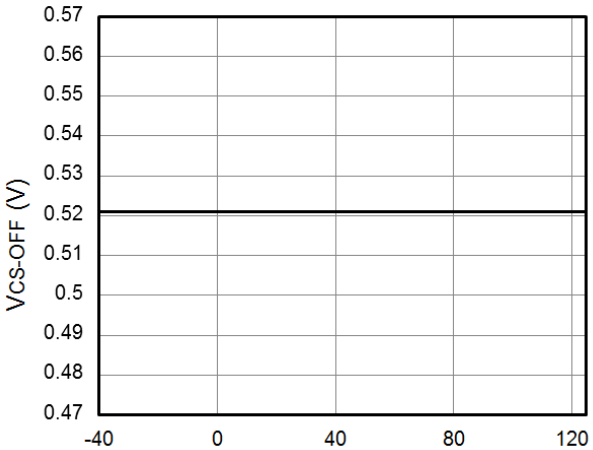


Fig. 5 VCS Limit level vs.Temperature

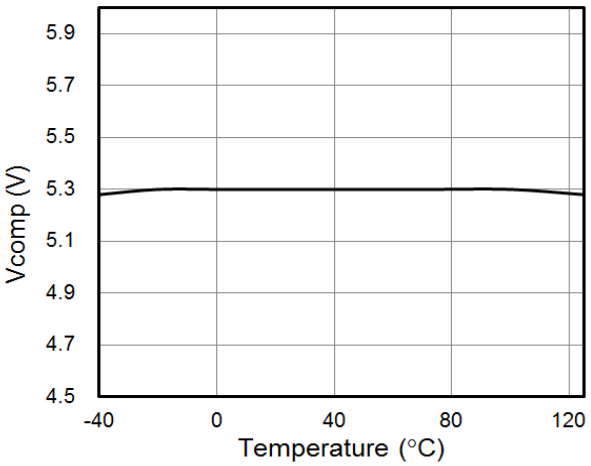


Fig. 6 Open Loop Voltage Level vs.Temperature

Application Information

Operation Overview

The LD5525 is built in the multi-mode PWM controller, in which operates a constant frequency to achieve the CCM as heavy load. For demanding higher power efficiency and power-saving in light load condition, the LD5525 implements QR function to allow the valley switching and accomplish zero voltage switching (ZVS). Under different load conditions, LD5525 provides the different solutions for achieving higher efficiency and performance.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD5525 PWM controllers and further to drive the power MOSFET. As shown in Fig. 7, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.0V and 7.5V, respectively.

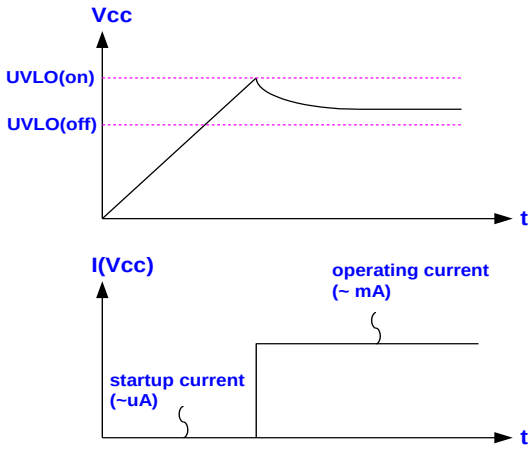


Fig. 7

Startup Current and Startup Circuit

The typical startup circuit to generate the LD5525 VCC is shown in Fig. 8. During the startup transient, the VCC is lower than the UVLO threshold thus there is no gate pulse produced from LD5525 to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the VCC voltage is high enough to turn on the LD5525 and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer.

Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD5525 is only 3μA. If a higher resistance value of R1 is chosen, it usually takes more time to start up. To select the value of R1 and C1 carefully will optimize the power consumption and startup time.

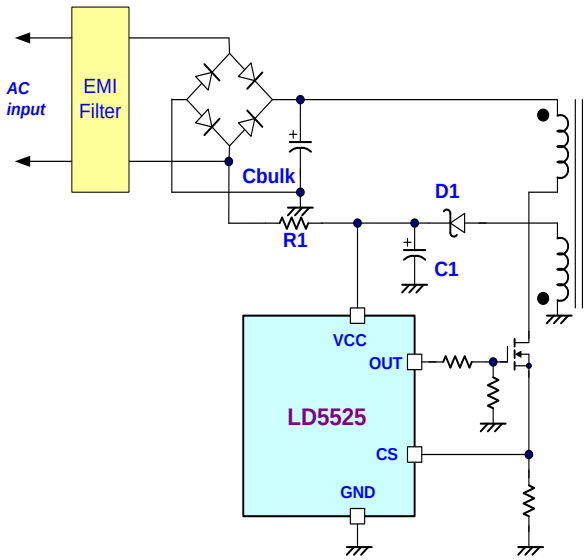


Fig. 8

Q-R Mode Detection

The transformer will be demagnetized after the main power MOSFET turns off. A quasi resonant signal will be detected from auxiliary winding by FB pin through the external resister.

As soon as the current of the secondary side diode is down to zero during MOSFET-off period, the transformer's core is demagnetized completely. V_{DS} of MOSFET will

resonate in discontinuous current mode. The resonance frequency (F_{QR}) will be obtained as below.

$$F_{QR} = \frac{1}{2\pi\sqrt{L_m * C_R}} (HZ)$$

L_M = Inductance of primary winding

C_R = Resonance equivalent parasitic capacitance

If V_{DS} voltage falls to resonant valley level from max plateau value, the QRD comparator will be tripped while FB pin voltage is close to 100mV.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD5525. Similar to UC3842, the LD5525 would without voltage offset to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{RB}{RA+RB} \times V_{COMP}$$

A pull-high resistor is embedded internally and therefore no external one is required.

Current Sensing, Leading Edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD5525 detect the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin sets at 0.57V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK\,(MAX)} = \frac{0.57V}{R_{CS}}$$

A 350nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spike is less than 350nS and the negative spike on the CS pin doesn't exceed -0.3V, it could remote the R-C filter (as shown in the figure 9).

However, the total pulse width of the turn-on spike is decided by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in figure 10) for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

Output Stage and Maximum ON Time

An output stage of a CMOS buffer, with typical 250mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum on time of LD5525 is limited to 15us to limit the minimum frequency of the system.

Maximum Switching Frequency Clamp

According to the QR operation principle, the switching frequency is inversely proportional to the output power. Therefore, as the output power decreases, the switching frequency can become rather high without limiting. The maximum switching frequency of LD5525 is clamped at 65 kHz internally to provide the optimized operations by considering the EMI performance, thermal treatment, component sizes and transformer design.

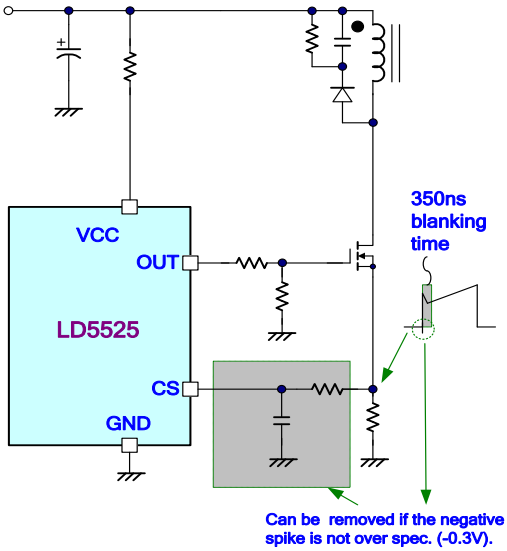


Fig. 9

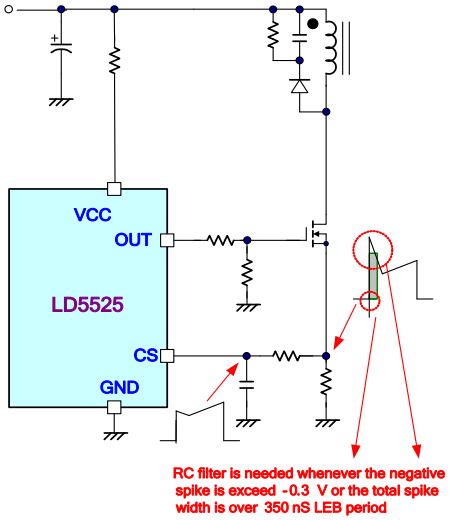


Fig. 10

Over Voltage Protection on VCC pin (VCC OVP) – Auto Recovery

The V_{GS} ratings of the nowadays power MOSFETs are often limited up to max. 28.5V. To prevent the V_{GS} from the fault condition, LD5525 is implemented with an OVP function on VCC. Whenever the VCC voltage is higher than the OVP threshold voltage, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(ON).

The VCC OVP function in LD5525 is an auto-recovery type protection. The Fig. 11 shows its operation.

On the other hand, if the OVP condition is removed, the VCC level will get back to normal level and the output will automatically return to the normal operation.

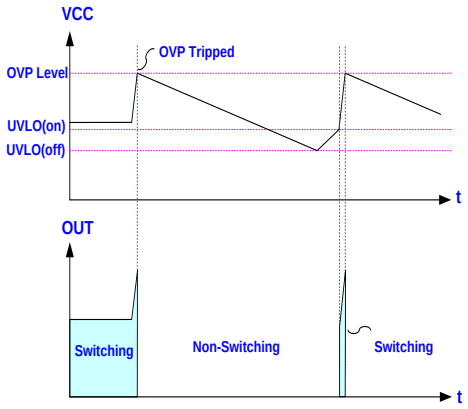


Fig.11

Over Load Protection (OLP) – Auto Recovery

To protect the circuit from damage due to over-load condition and short or open-loop condition, the LD5525 is implemented with smart OLP function. It also features auto –recovery function, see Fig. 12 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the V_{COMP} ramps up to the OLP threshold of 4.5V and continues over OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

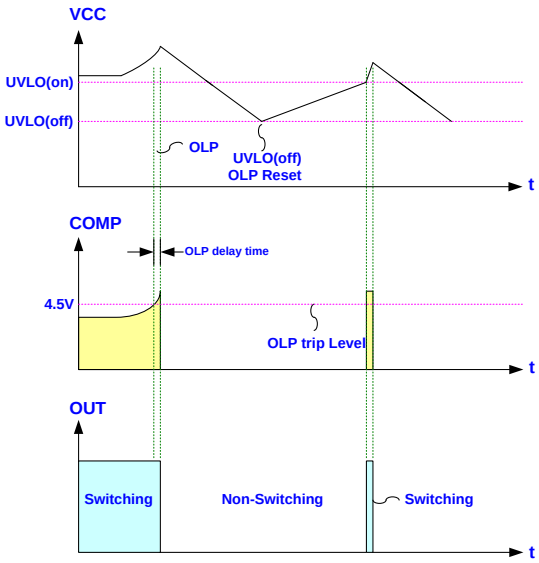


Fig. 12

Adjustable Over Current Compensation on FB Pin

For compensating the differential input current from high/low line conditions on current sensing resistor, LD5525 mirrors a compensation current I_{OCP} from I_{FB} to CS pin. The relationship of compensation current I_{OCP} and I_{FB} is expressed by following equation and shown in Fig. 13.

$$I_{OCP} = K \times I_{FB}$$

, where $K = 0.5$

K is the mirror current ratio of FB pin, and the I_{OCP} follows to the input voltage.

The compensation current I_{OCP} supplies an offset voltage by external resistor R_{OCP}, which is series between the current sensing resistor R_S and CS pin. By selecting a proper value of the resistor R_{OCP} in series with the CS pin, the amount of compensation can be adjusted.

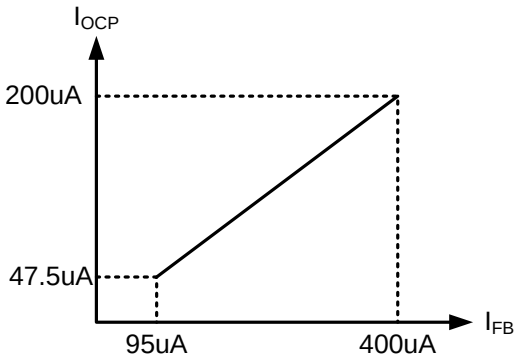


Fig. 13

Brown-In/ Brown-Out Protection (BNI/BNO) – Auto Recovery

The LD5525 integrate the brown in, brownout protection and valley detection into FB pin. The auxiliary voltage reflects a proportional bulk voltage during the on time. Fix the internal current at the BNI and BNO, the BNI level could be set by modulating the FB divided resistors and auxiliary voltage, as shown in Fig. 14. For preventing the abnormal condition of line voltage to causing damage, BNO function is implemented, while turns off the gate signal after de-bounce time 60ms as BNO occurring, as shown in Fig. 15. The relationship of input voltage and BNI/BNO is expressed in following equation.

$$V_{DC\_BNI} = \frac{N_P}{N_a} \cdot I_{BNI} \cdot R_1$$

$$V_{DC\_BNO} = \frac{N_P}{N_a} \cdot I_{BNO} \cdot R_1$$

,where

V_{DC_BNI} is predicted BNI DC value of input voltage

V_{DC_BNO} is predicted BNO DC value of input voltage

I_{BNI} is BNI trip current.

I_{BNO} is BNO trip current.

N_p is turns ration of primary-side winding

N_a is turns ration of auxiliary winding

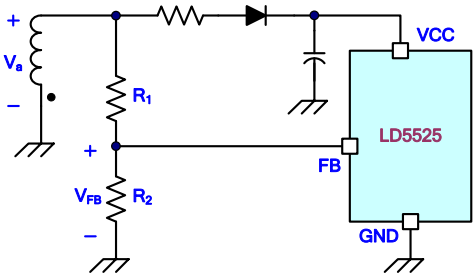


Fig. 14

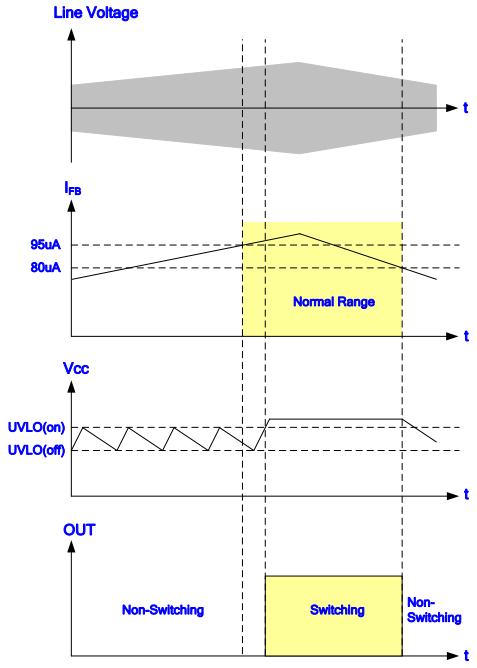


Fig. 15

Over Voltage Protection on FB pin (FB OVP) – Auto Recovery

An output overvoltage protection is implemented in the LD5525. The auxiliary winding voltage can be reflected from secondary winding, in which the FB pin voltage is proportional to output voltage during the gate off time. OVP is worked by sensing the auxiliary voltage via the divided resistors R2, refereeing to Fig. 14. The equation of FB OVP is shown as follows.

$$R_2 = \frac{R_1 \cdot V_{FB\_OVP}}{V_a - V_{FB\_OVP}}$$

$$V_a = \frac{N_a}{N_S}(V_O + V_F)$$

V_{FB_OVP} is the FB pin OVP trip voltage level. V_a is the auxiliary winding voltage which reflects from the forward voltage V_F of Schottky diode and output voltage V_O. N_S is turns ration of secondary-side winding.

If V_{FB} overs the FB OVP trip level, the internal counter starts counting 8 cycles, and then LD5525 goes to auto-recovery protection mode till the FB OVP status is defused

Under Voltage Protection on FB pin (FB UVP) – Auto Recovery

In order to prevent output short situation, LD5525 is implemented by FB_UVP. When the output load is shorted to ground, the voltage suddenly decreases to zero, which always reflects to auxiliary winding during the gate off region. Therefore, as V_{FB} is lower than 1V during gate off region, and then the FB_UVP is triggered.

Over Temperature Protection on CS pin (CS OTP)- Auto Recovery

LD5525 is implemented over temperature protection on CS pin which senses voltage to determine NTC status during gate off region. As VCS is greater than 0.5V and continues for 8 cycles, CS_OTP is triggered, than LD5525 is in auto recovery mode till the temperature drops to setting work condition.

Oscillator and Switching Frequency

The LD5525 is implemented with Frequency Swapping function which helps the power supply designers to both optimize EMI performance and lower system cost.

Green Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property.

Fault Protection

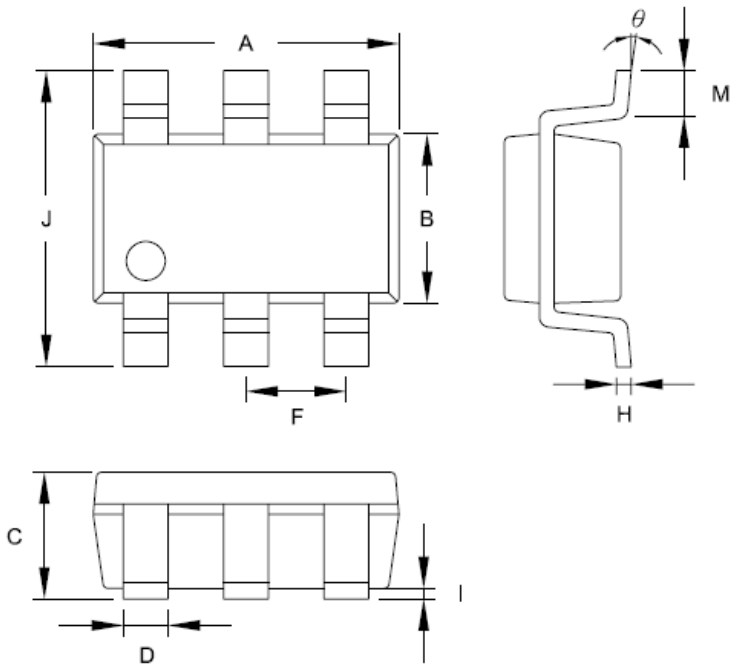
There are several critical protections integrated in the LD5525 to prevent from damage to the power supply. Those damages usually come from open or short conditions on the pins of LD5525.

In case under such conditions listed below, the gate output will turn off immediately to protect the power circuit.

1. CS pin floating
2. COMP pin floating

Package Information

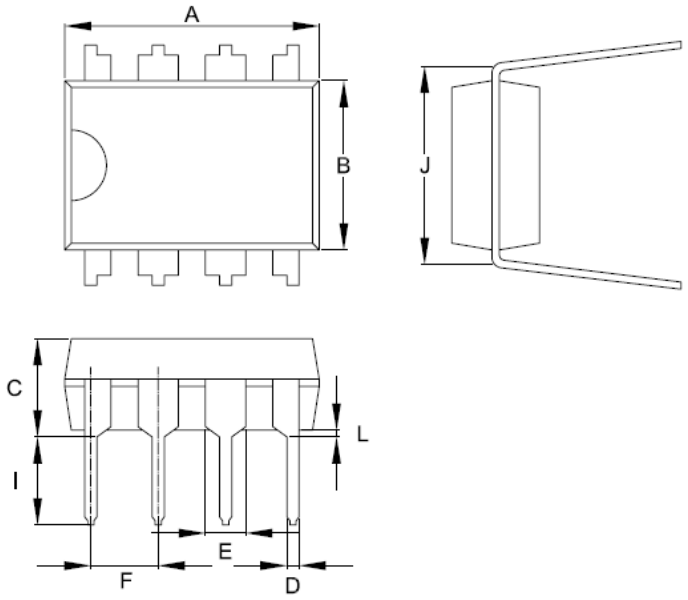
SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	06/30/2015	Original Specification.