Green-Mode PWM Controller with Frequency Swapping and Integrated Protections

REV:01

General Description

The LD5533 is built with several functions, protection and EMI-improved solution in a tiny package. It takes less components counts or circuit space, especially ideal for those total solutions of low cost.

The implemented functions include low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. It also features more protections like OPP (Over Power Protection), OCP (Over Current Protection), OSCP (Output Short Circuit Protection) and OVP (Over Voltage Protection) to prevent circuit damage occurred under abnormal conditions.

Furthermore, the Frequency Swapping function is to reduce the noise level and thus helps the power circuit designers to easily deal with the EMI filter design by spending minimum amount of component cost and developing time.

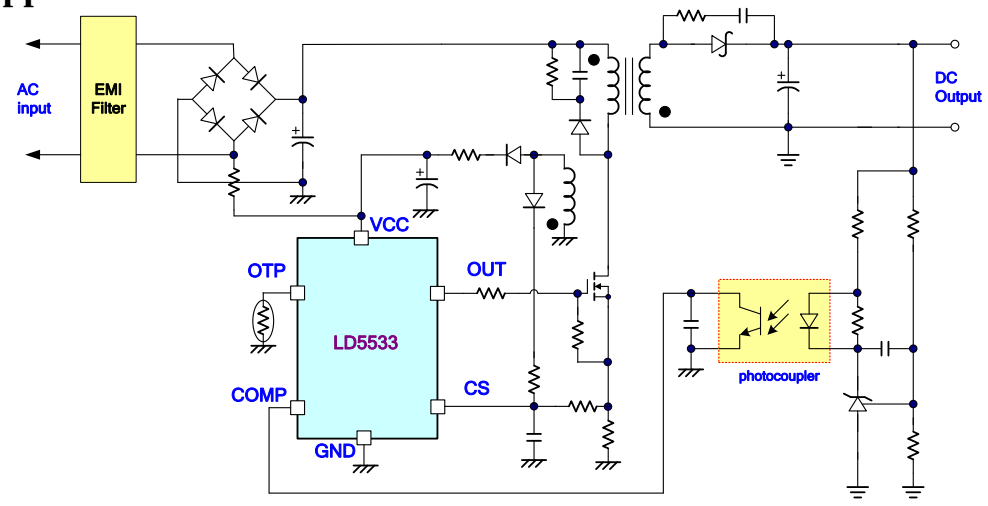
Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (<12μA)
- Current Mode Control
- Green Mode Control
- UVLO (Under Voltage Lockout)
- Variable Frequency Technology around 130KHz
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Frequency Swapping
- Internal Slope Compensation
- OVP (Over Voltage Protection) on Vcc Pin
- OTP (Over Temperature Protection) through a NTC
- OPP (Over Power Protection)
- OCP (Over Current Protection)
- OSCP (Short circuit protection)
- 300/-500mA Driving Capability

Applications

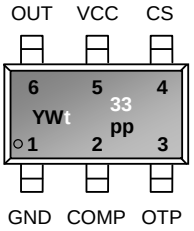
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

Typical Application



Pin Configuration

SOT-26 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005…..)
WW, W : Week code
PP : Production code
t33 : LD5533

Ordering Information

Part number	Package	Top Mark	Shipping
LD5533 GL	SOT-26	YWt/33	3000 /tape & reel

The LD5533 is ROHS compliant/ Green packaged

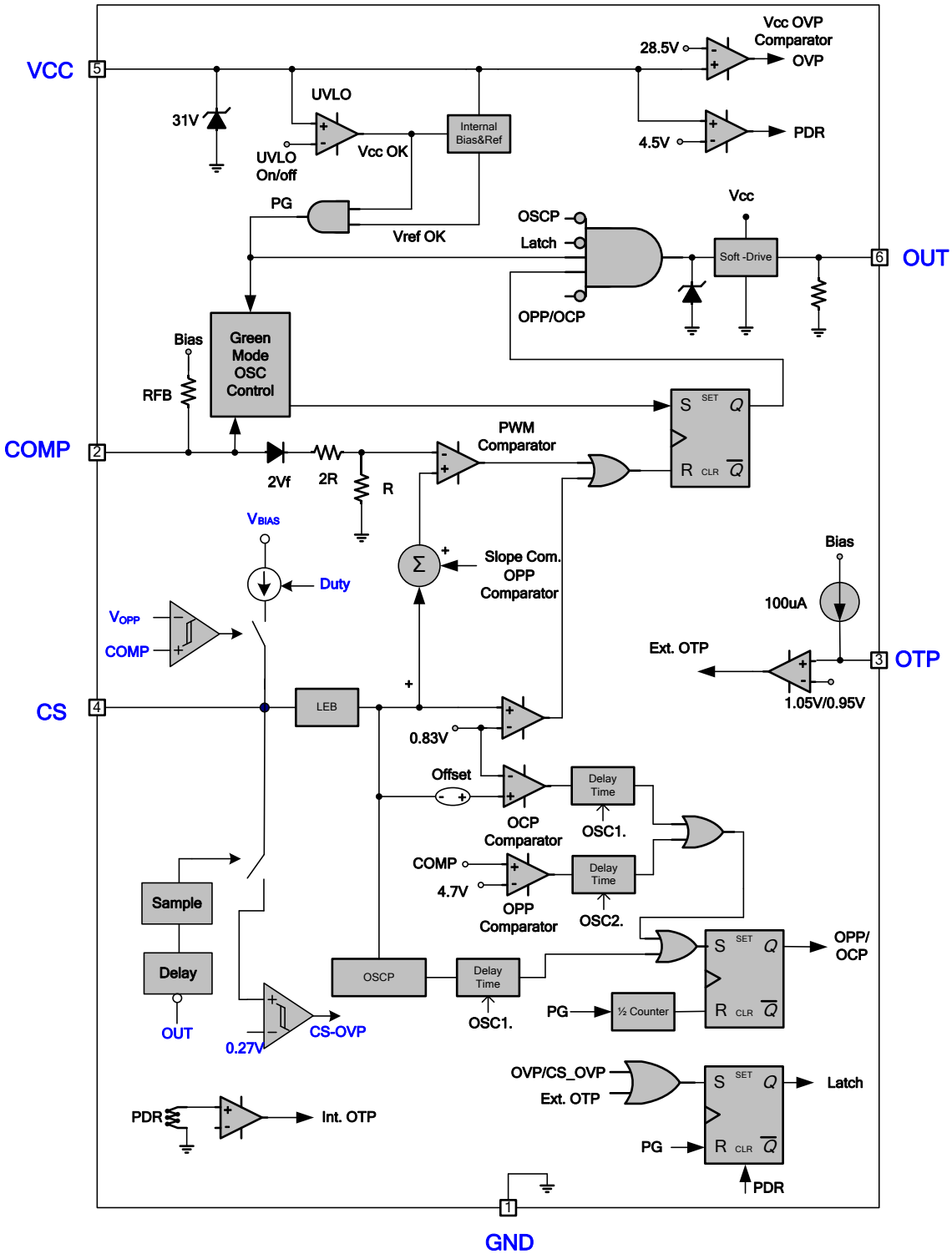
Protection Mode

Switching Freq.	VCC OVP	OPP	OCP	OSCP	Int. OTP	OTP Pin	CS Pin OVP
130KHz	Latch	Auto-Restart	Auto-Restart	Auto-Restart	Auto-Restart	Latch	Latch

Pin Descriptions

PIN	NAME	FUNCTION
1	GND	Ground
2	COMP	Voltage feedback pin (same as the COMP pin in UC384X). Connect a photo-coupler to close the control loop and achieve the regulation.
3	OTP	Pull this pin below 0.95V to shut off the controller into Latch mode until the AC power resumes. Connecting this pin to ground with NTC will achieve OTP protection. Let this pin float or connect a 100kΩ resistor to disable the Latch protection.
4	CS	Current sense pin, connect it to sense the MOSFET current. This pin is also connected to an auxiliary winding of the PWM transformer through a resistor and a diode for output over-voltage protection.
5	VCC	Supply voltage pin
6	OUT	Gate drive output to drive the external MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V ~30V
COMP, OTP, CS	-0.3V ~10V
OUT	-0.3V ~Vcc+0.3V
Maximum Junction Temperature	150°C
Operating Ambient Temperature	-40°C to 85°C
Operating Junction Temperature	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance @85°C (SOT-26, θ_{JA})	200°C/W
Power Dissipation (SOT-26)	200mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Ambient Temperature	-40	85	°C
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.5	26.5	V
VCC Capacitor	3.3	10	μF
Start-up resistor Value (AC Side, Half Wave)	400K	1.8M	Ω
Comp Pin Capacitor	1	10	nF
CS Pin Capacitor Value	47	390	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	Symbol	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)						
Startup Current	VCC < UVLO (ON)	I_{STUP}			12	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V	I_{VCC_0V}		0.7	0.75	mA
	V_{COMP}=3V	I_{VCC_3V}		2	2.3	mA
Holding Current	V_{CC}=7.5V (latched)	$I_{HD\_7.5V}$	-5%	430	+5%	μA
	V_{CC} =5V (latched)	I_{HD_5V}	-8%	40	+8%	μA
	Auto mode.	I_{HD_auto}		530		μA
Holding Voltage	ICC=200μA	$V_{HD\_200\mu A}$	5.5	6.5	7.5	V
	ICC=100μA	$V_{HD\_100\mu A}$				
UVLO (off)		$V_{UVLO(OFF)}$	8.1	8.6	9.1	V
UVLO (on)		$V_{UVLO(ON)}$	15	16	17	V
OVP Level		V_{OVP}	27.5	28.5	29.5	V
OVP pin de-bounce time		T_{DE_OVP}		8		cycle
Latch-Off Release Voltage		V_{LCH_OFF}	4	4.5	5	V
Voltage Feedback (Comp Pin)						
Short Circuit Current	V_{COMP}=0V	I_{COMP_0V}	0.1	0.125		mA
Open Loop Voltage	COMP pin open	I_{COMP_OP}	5.1	5.3		V
Peak Mode Threshold VCOMP		V_{COMP_PK}		4.4		V
Peak Mode Down Threshold	(Fig 1.)	V_{COMP_DN}		4.2		V
Green Mode Threshold VCOMP		V_{COMP_GN}		2.8		V
Green Mode Down Threshold VCOMP, FSW_DN		$V_{COMP\_GN\_DN}$		2.3		V
Zero Duty Threshold VCOMP		V_{ZD}		1.7		V
Zero Duty Hysteresis		V_{ZD_H}		100		mV
IOPP Threshold VCOMP	Duty≤20%	V_{IOPP}		4		V
Current Sensing (CS Pin)						
Limit Voltage, V_{CS_OFF}	Duty≥50%	V_{CS_OFF}	-4%	0.83	+4%	V
OCP Voltage for Low line, V_{CS}	(Fig 2.)	V_{CS}	-4%	0.68	+4%	V
OCP Voltage for High line, V_{CS_OFFSET}		V_{CS_OFFSET}		0.06		V
OPP Compensation Current	Duty≥50%	I_{OPP_50}	0		5	μA
	Duty≤20%	I_{OPP_20}		575		μA
Leading Edge Blanking Time		t_{LEB}		250	300	ns
Internal Slope Compensation	0% to D_{MAX}. (Linearly increase) , note 1	V_{SLOPE}		300		mV

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	Symbol	MIN	TYP	MAX	UNITS
Input impedance	note 1	Z_{IN}	1			MΩ
Delay to Output	note 1	T_D	50		100	ns
OVP CS pin						
OVP Trip Current Level		V_{CS_OVP}	-8%	0.27	+8%	V
De-bounce Cycle		T_{DE_OVP}		8		Cycle
Oscillator for Switching Frequency						
Frequency, FREQ	Normal mode	F_{SW}	62	65	68	kHz
	Peak mode	F_{SW_PK}	123	130	137	kHz
Green Mode Frequency, FREQG	Green mode	F_{SW_GM}	20	23	26	kHz
Swapping Frequency		F_{SWAP}		±6		%
Temp. Stability	(-20°C ~85°C), note 1	T_{STAB}	0	5		%
Voltage Stability	(VCC=11V-25V) , note 1	V_{STAB}	0	1		%

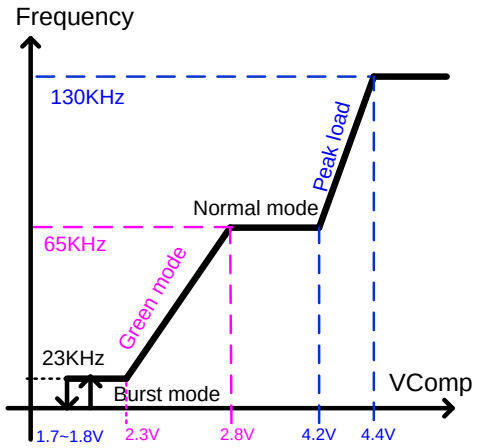


Fig 1. V_{COMP} vs. PWM Frequency

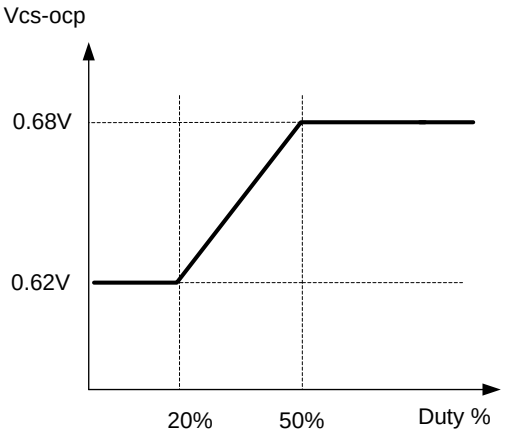


Fig 2. Duty vs. OCP level

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	Symbol	MIN	TYP	MAX	UNITS
Gate Drive Output (OUT Pin)						
Output Low Level	VCC=15V, Io=20mA	V_{O_L}			1	V
Output High Level	VCC=15V, Io=20mA	V_{O_H}	8		15	V
Output High Clamp Level	V_{CC}=20V	V_{O_HC}	13	15	17	V
Rising Time	Load Capacitance= 1000pF	T_R	--	150	250	ns
Falling Time	Load Capacitance= 1000pF	T_F		50	100	ns
Source capability	Load Capacitance= 33nF, note 1	I_{O_SOURCE}		300		mA
Sink capability	Load Capacitance= 33nF, note 1	I_{O_SINK}		500		mA
Max. Duty		D_{MAX}		85		%
OPP (Over Power Protection)						
OPP Trip Level		V_{COMP_OPP}	4.5	4.7	4.9	V
OPP Delay Time	Excluding soft start time	T_{D_OPP}		20		ms
OCP (Over Current Protection)						
OCP Delay Time		T_{D_OCP}	100	110	120	ms
OSCP (Output Short Circuit Protection)						
OSCP Trip Level		V_{OSCP}		CS Limit		V
OSCP Delay Time	Excluding soft start time.	T_{D_OSCP}		8		Cycle
OTP Pin Auto-Restart Protection						
OTP Pin Source Current	(VCC=11V-25V)	I_{OTP}	92	100	108	μA
Turn-On Trip Level		V_{OTP_ON}	1.00	1.05	1.10	V
Turn-Off Trip Level		V_{OTP_OFF}	0.9	0.95	1.0	V
OTP LATCH pin de-bounce time		T_{D_OTP}		250		μs
On Chip OTP (Over Temperature)						
OTP Level	Note 2	T_{OTP}		140		°C
OTP Hysteresis	Note 2	T_{H_OTP}		30		°C
Soft Start Duration						
Soft Start Duration	Note 1	T_{SS}		7		ms

Notes:

1. : guaranteed by design

2. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.

Typical Performance Characteristics

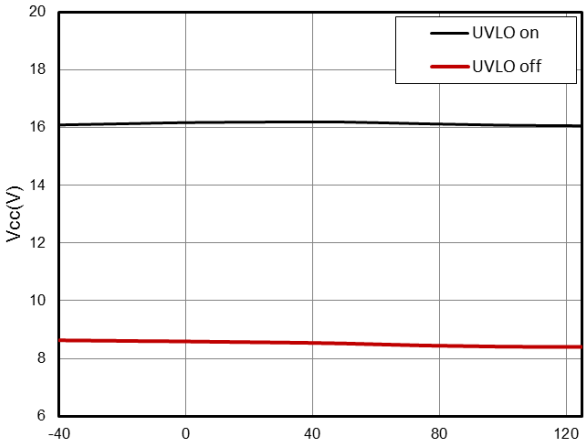


Fig. 3 UVLO level vs.Temperature

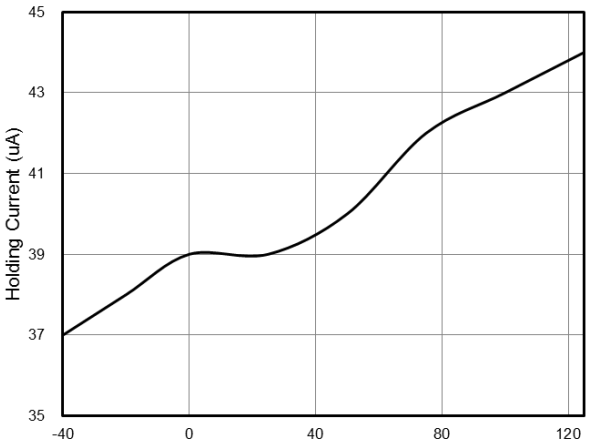


Fig. 4 Holding Current vs.Temperature

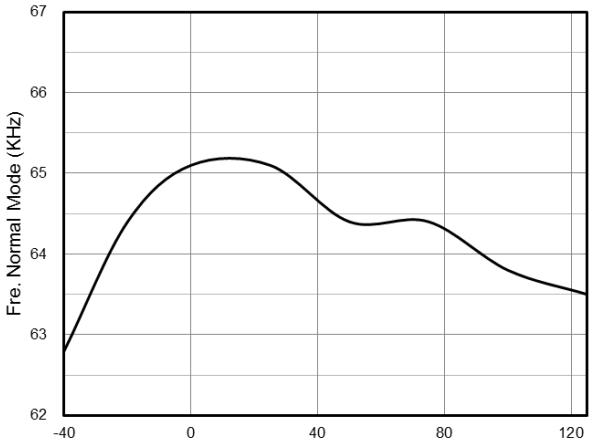


Fig. 5 Fre. Normal Mode vs.Temperature

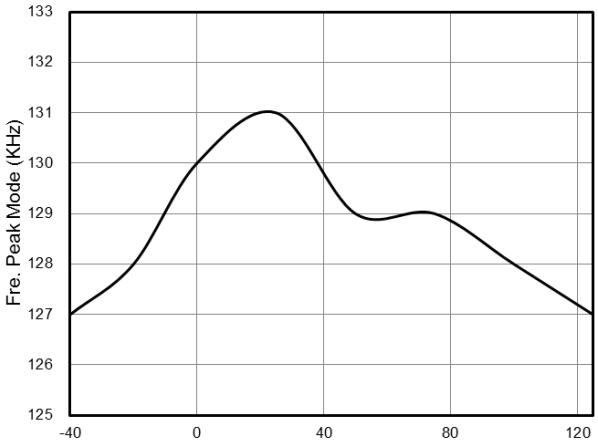


Fig. 6 Fre. Peak Mode vs.Temperature

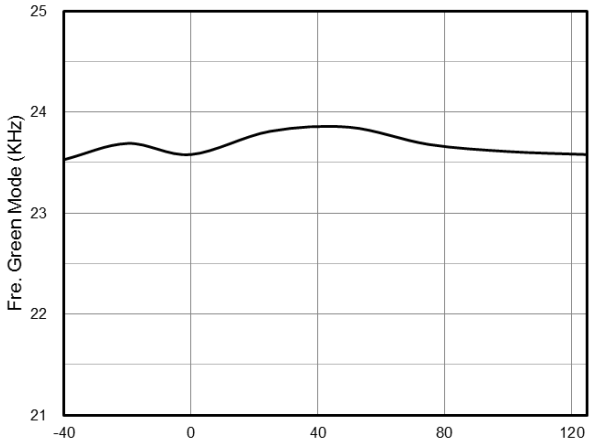


Fig. 7 Fre. Green Mode vs.Temperature

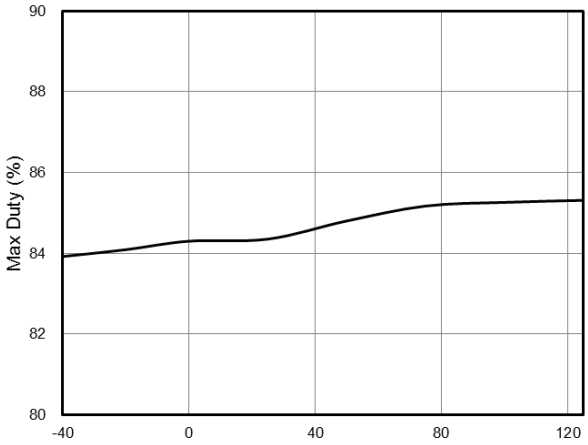


Fig. 8 Max Duty vs.Temperature

Typical Performance Characteristics

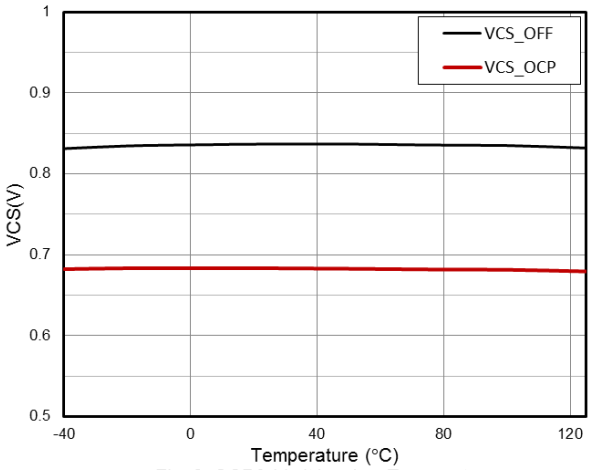


Fig. 9 OCP& Limit level vs.Temperature

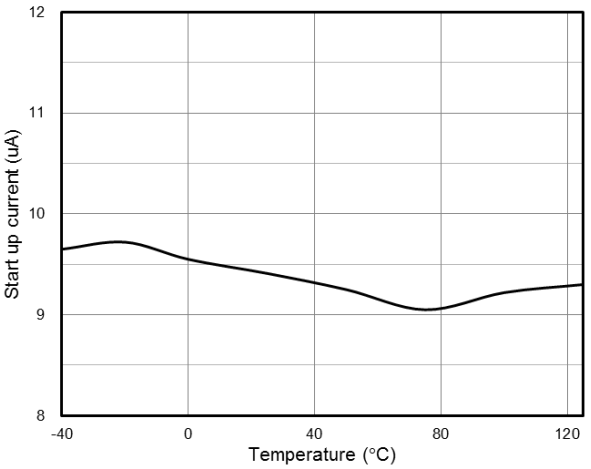


Fig. 10 Start up current vs.Temperature

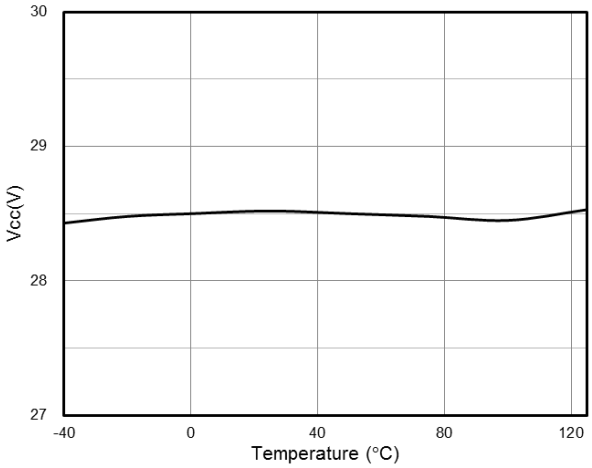


Fig. 11 Vcc OVP Level vs.Temperature

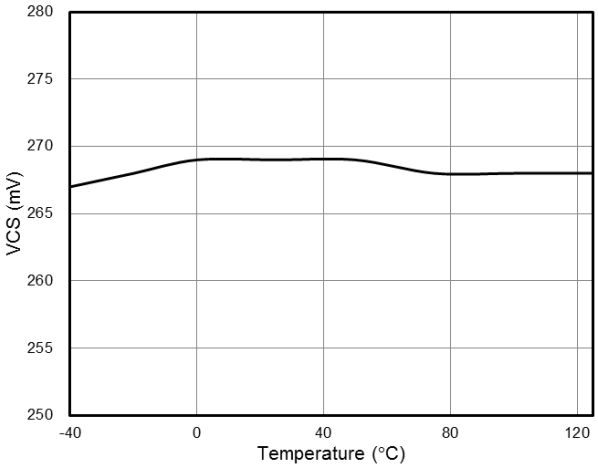


Fig. 12 VCS OVP Level vs.Temperature

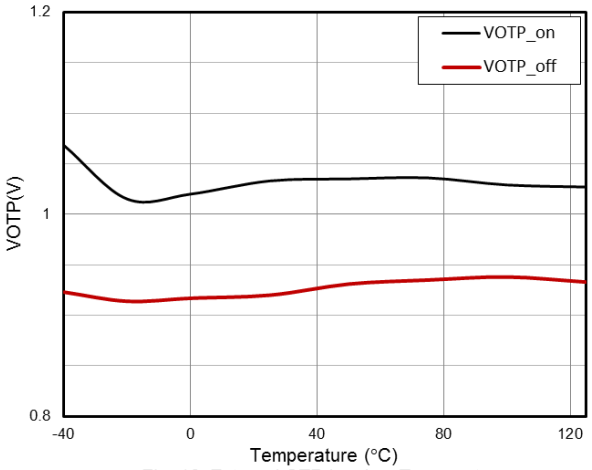


Fig. 13 External OTP level vs.Temperature

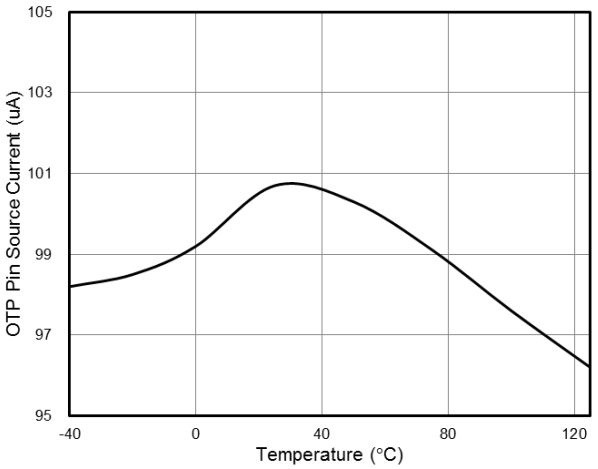


Fig. 14 OTP Pin Source Current vs.Temperature

Application Information

Operation Overview

The LD5533 meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrates more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD5533 PWM controller and further to drive the power MOSFET. As shown in Fig. 15, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.0V and 7.5V, respectively.

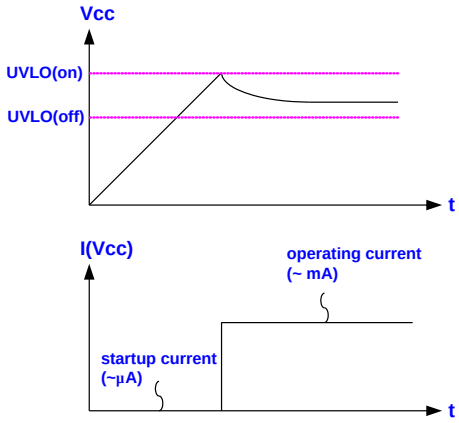


Fig. 15

Startup Current and Startup Circuit

The typical startup circuit to generate V_{CC} of the LD5533 is shown in Fig. 16. During the startup transient, the V_{CC} is below UVLO threshold. Before it has sufficient voltage to develop OUT pulse to drive the power MOSFET, R1 will provide the startup current to charge the capacitor C1. Once V_{CC} obtain enough voltage to turn on the LD5533 and further to deliver the gate drive signal, it will enable the auxiliary winding of the transformer to provide supply current. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current for LD5533 is only 12μA.

If a higher resistance value of the R1 is chosen, it will usually spend more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

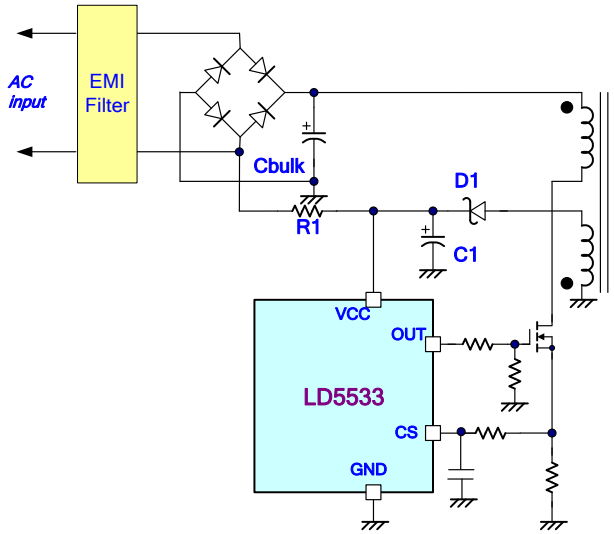


Fig. 16

Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 17, the LD5533 detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.83V. From above, the MOSFET peak current is concluded as below.

$$I_{PEAK(MAX)} = \frac{0.83V}{R_S}$$

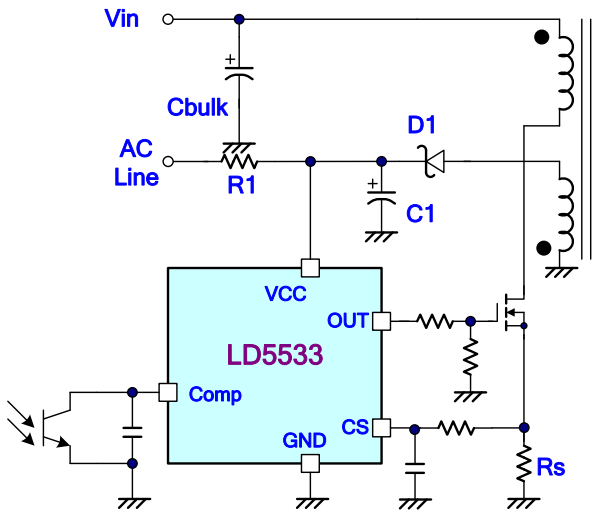


Fig. 17

A 250nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent false-triggering from the current spike. In those low power applications, if the total pulse width of the turn-on spikes is less than 150nS and the negative spike on the CS pin below -0.3V, the R-C filter is free to eliminate. (As shown in Fig. 18).

However, the total pulse width of the turn-on spike is subject to output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in Fig. 19) for large power application to avoid the CS pin being damaged by the negative turn-on spike.

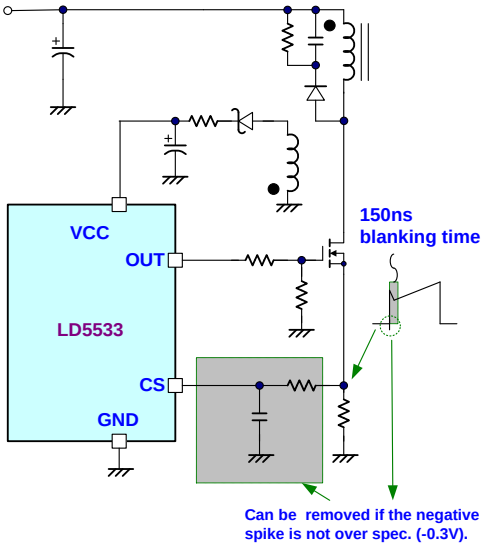


Fig. 18

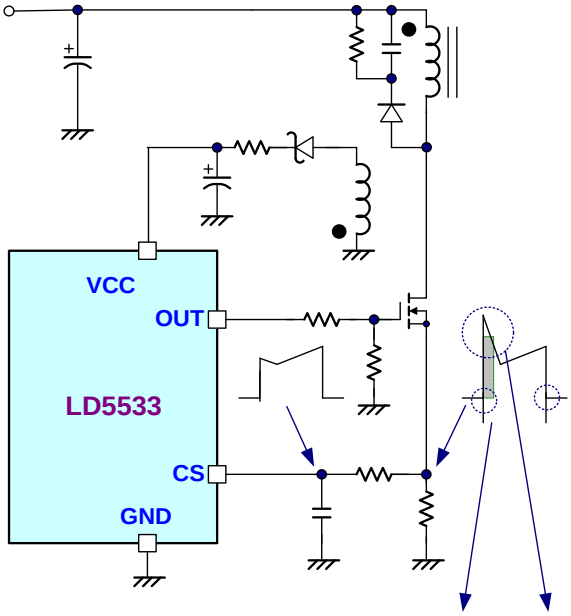


Fig. 19

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD5533 is limited to 85% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD5533. Similar to UC3842, the LD5533 would carry 2 diode voltage offset at the stage to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{RB}{RA + RB} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally and therefore no external one is required.

Internal Slope Compensation

In the conventional applications, the problem of the stability is a critical issue for current mode controlling,

when it operates over 50% duty-cycle. As UC384X, It takes slope compensation from the ramp signal of the RT/CT pin injected through a coupling capacitor. It therefore requires no extra design for the LD5533 since it has integrated it already.

On/Off Control

To pull COMP below 1.6V can disable the gate output pin of the LD5533. The off-mode can be released when the pull-low signal is removed.

Over Power Protection (OPP) - Auto Recovery

To protect the circuit from damage in over-power short or open-loop condition, the LD5533 is implemented with smart OPP function. It also features auto recovery function, see Fig. 20 for the waveform. In case of fault condition, the feedback system will force the voltage loop enter toward saturation and then pull the voltage high on COMP pin (VCOMP). When the V_{COMP} ramps up to the OPP threshold of 4.7V and continues over OPP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

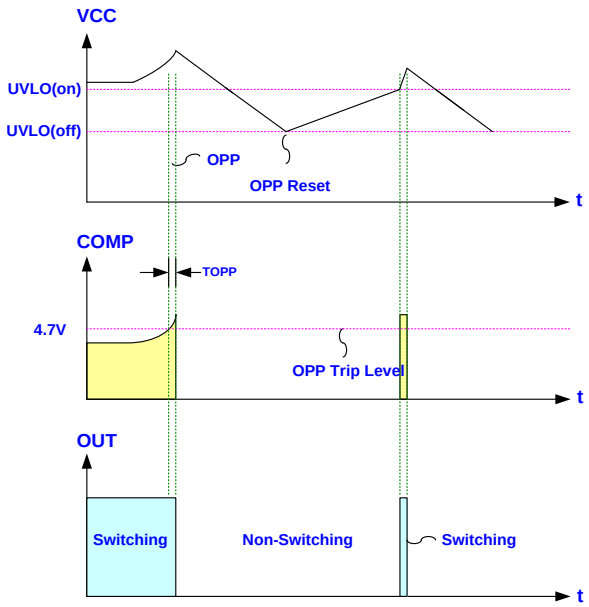


Fig. 20

Over Current Protection (OCP) - Auto Recovery

When the switching current is higher than the OCP threshold, the internal counter counts up. When the total accumulated counting time is more than 110ms, the controller triggers the OCP. This protection is auto recovery function.

OSCP (Output Short Circuit Protection) - Auto Recovery

Even when the output shorts to GND, there's no way to turn off the signal unless the following four conditions are met.

1. The CS is higher than limit voltage.
2. The comp voltage is higher than 4.7V
3. This duration is greater than 8 cycles.
4. Turn on time is lower than 1μs.

The out signal could not be charged either, if it fails to meet the three conditions.

Once the protection is triggered, switching is terminated and the MOSFET remains off.

OVP (Over Voltage Protection) on Vcc – Latch Mode

The Vcc OVP function of LD5533 is in latch mode. As soon as the voltage of the Vcc pin rises above OVP threshold, the output gate drive circuit will be shut down simultaneously to latch off the power MOSFET. On the contrast, if the voltage on Vcc pin drops below OVP threshold and starts AC-recycling again, it will soon resume to normal operation. Fig. 21 shows its operation.

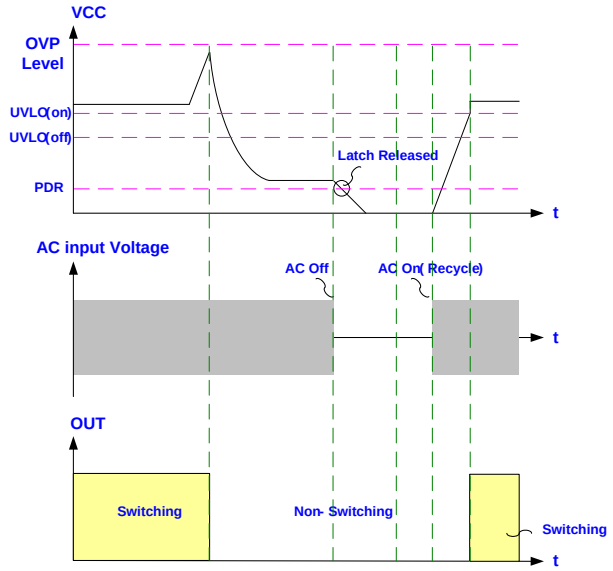


Fig. 21

OTP Pin --- Latched Mode Protection

To protect the power circuit from damage due to system failure, over temperature protection (OTP) is required. The OTP circuit is implemented to sense whether there's a hot-spot over power circuit like power MOSFET or output rectifier. It can be easily achieved by connecting a NTC with OTP pin of LD5533. As the device temperature or ambient temperature rises, the resistance of NTC decreases. So, the voltage across the OTP pin could be written as below.

$$V_{OTP} = 100\mu A \cdot R_{NTC}$$

If the V_{OTP} is below the defined voltage threshold (0.95V in typical), the LD5533 will terminate the gate output and latch off the power supply. There are 2 conditions required to restart it successfully. First, cool down the circuit so that NTC resistance will increase and raise V_{OTP} up above 1.05V. Then, remove the AC power cord and restart AC power-on recycling.

Adjustable Over Power Compensation (CS Pin)

In general, the power converter can deliver more current with high input voltage than low input voltage. To compensate this, an offset voltage is added to the CS signal by an internal current source (I_{OPP}) and an external resistor (R_{OPP}) in series between the sense resistor (Rs) and the CS pin, as shown in Fig. 22. Different values of resistors in series with the CS pin may adjust the amount of compensation. The value of I_{OPP} depends on the duty cycle of OUT pin. The equation of I_{OPP} is decreased as:

$$I_{OPP} = \begin{cases} (0.5 - Duty) \cdot 1915\mu A & (0.2 < Duty < 0.5) \\ 0\mu A & (Duty \geq 0.5) \\ 575\mu A & (Duty \leq 0.2) \end{cases}$$

In light load, this offset is in same level of magnitude as the current sense signal, it shall be canceled. Therefore the compensation current will be fully added once the COMP voltage is above 3.05V, as shown in Fig. 23.

R_{OCP}:470Ω~1.4kΩ; C_{OCP}:82pF~390pF

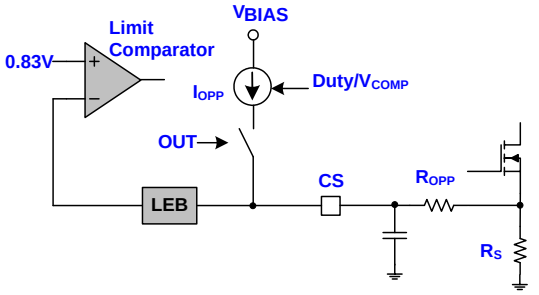


Fig. 22

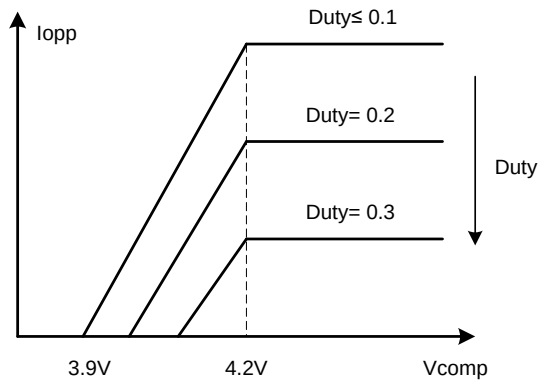


Fig. 23

Output Over Voltage Protection – Latch Mode

An output overvoltage protection is implemented in the LD5533 to sense the auxiliary voltage via the divided resistors as shown in Fig. 24. The auxiliary winding voltage is reflected to the secondary winding and therefore the flat voltage on the CS pin is in proportion to the output voltage. LD5533 can sample this flat voltage level after a delay time to perform output over voltage protection. This delay time is used to ignore the voltage ringing from leakage inductance of PWM transformer. The sampling voltage level is compared with internal threshold voltage 0.27V. If the sampling voltage exceeds the OVP trip level, an internal counter starts counting the subsequent OVP events. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. However, when typically 8 cycles of subsequent OVP events are detected, the OVP circuit switches the power MOSFET off. As the protection is latched, the converter only restarts after the internal latch is reset.

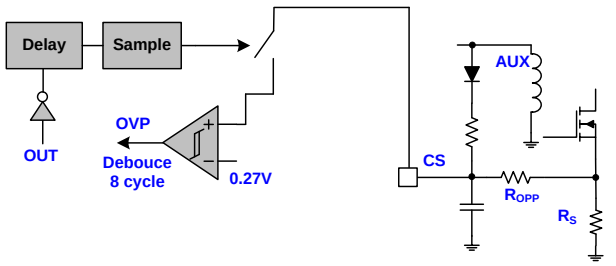


Fig. 24

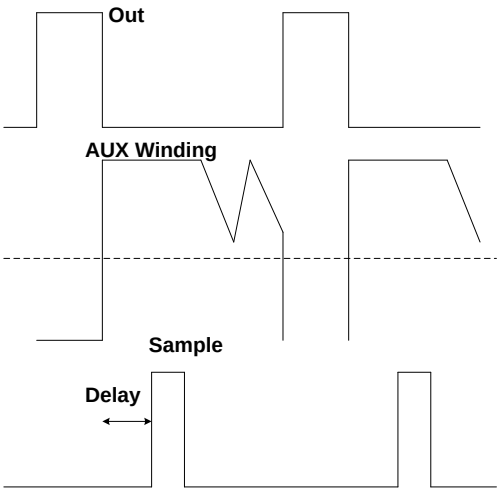


Fig. 25

Oscillator and Switching Frequency

The LD5533 is implemented with Frequency Swapping function which helps the power supply designers optimize EMI performance and reduce system cost. The switching frequency substantially centers at 130KHz, and swap between a range of ±6%.

Green-Mode Operation

By using the green-mode control, the switching frequency can be reduced in light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property.

Fault Protection

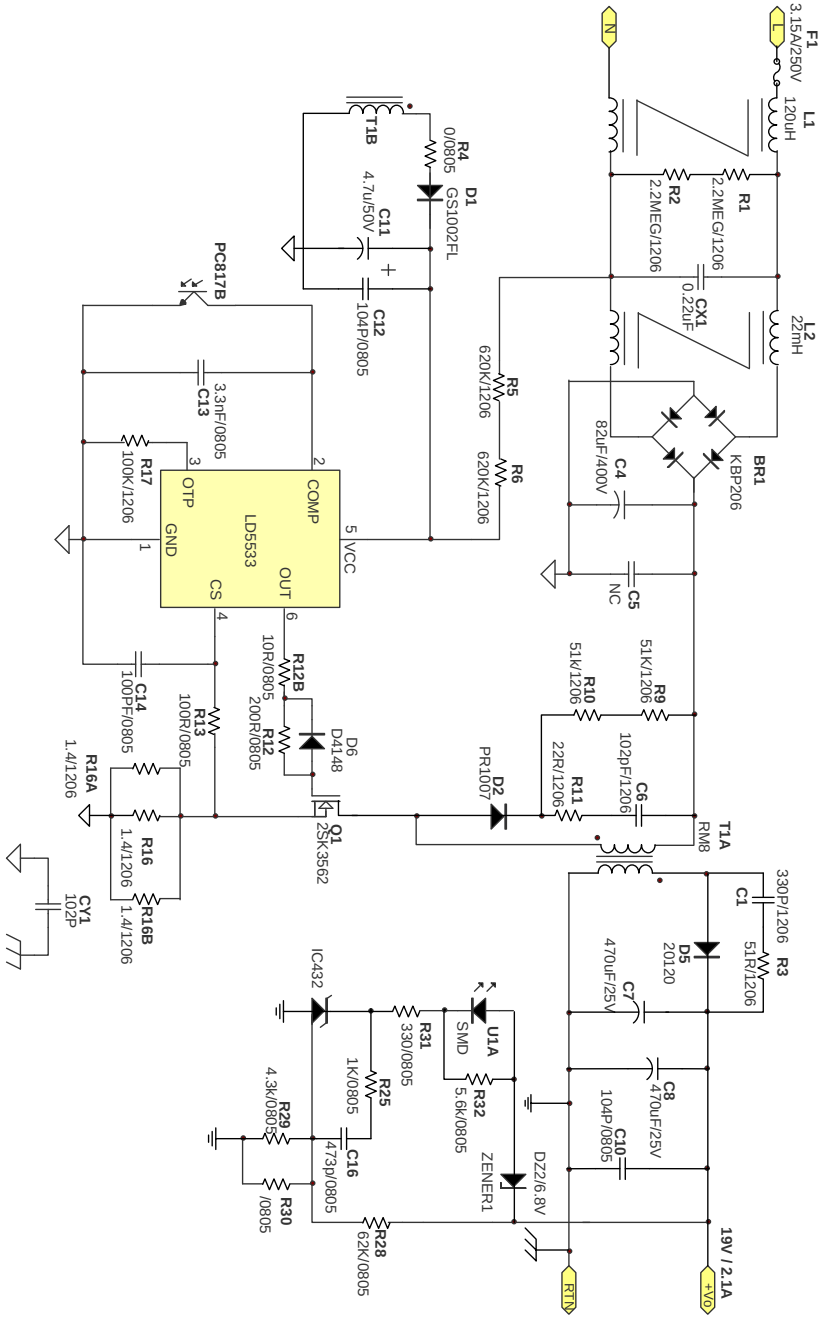
There are several critical protections integrated in the LD5533 to prevent from damage to the power supply.

Those damages usually came from open or short conditions on LD5533.

In case under the conditions listed below, the gate output will turn off immediately to protect the power circuit.

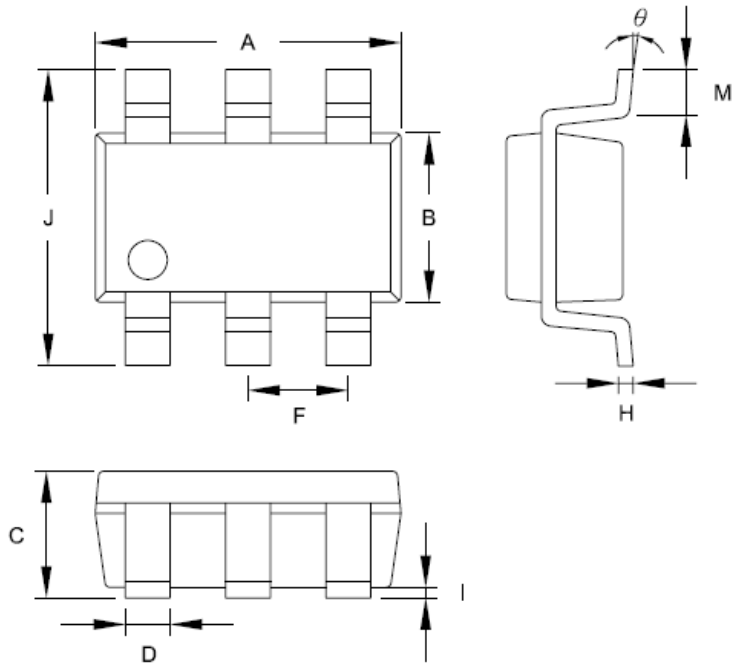
1. CS pin floating
2. COMP pin floating

Reference Application Circuit --- 40W (19V/2.1A) Adapter



Package Information

SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Revision History

Rev.	Date	Change Notice
00	02/18/2014	Original Specification
01	11/14/2016	Revise the top marking from YWP to YWt