Green-Mode PWM Controller with Frequency Swapping and Integrated Protections

REV. 00

General Description

The LD5537H1 is built-in with several functions, protection and EMI-improved solution in a tiny package. It takes less components counts or circuit space, especially ideal for those total solutions of low cost.

The implemented functions include low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. It also features more protections like OLP (Over Load Protection)、OVP (Over Voltage Protection) and AC BNI / BNO to prevent circuit damage occurred under abnormal conditions.

Furthermore, the frequency swapping function is to reduce the noise level and thus helps the power circuit designers to easily deal with the EMI filter design by spending minimum amount of component cost and developing time.

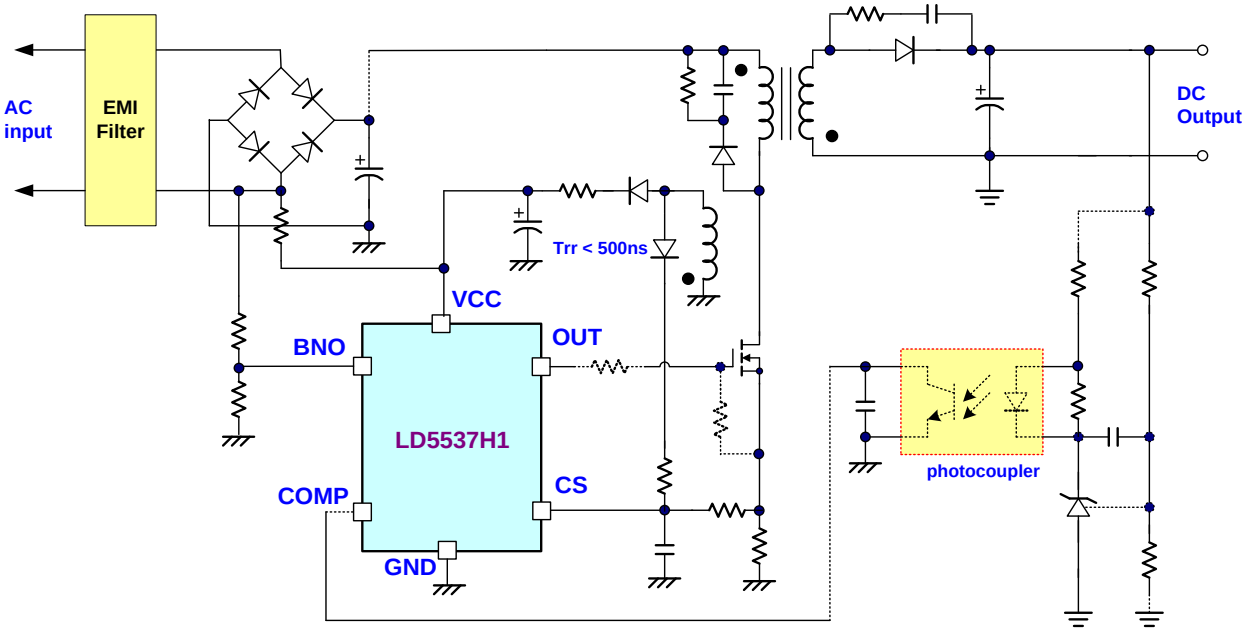
Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (<3μA)
- Multi-Mode PWM controller
- Current Mode Control
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Frequency Swapping, Slop Compensation
- OVP (Over Voltage Protection) on VCC and CS Pin
- Adjustment input AC BNI / BNO
- OLP (Over Load Protection)
- OSCP (Output Short Circuit Protection)
- 250mA/-500mA Driving Capability

Applications

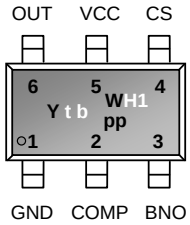
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

Typical Application



Pin Configuration

SOT-26 (TOP VIEW)



Y : Year code (D: 2004, E: 2005…..)
W : Week code
PP : Production code
tbH1 : LD5537H1

Ordering Information

Part number	Package	Top Mark	Shipping
LD5537H1 GL	SOT-26	Yt b/ WH1	3000 / tape & reel

The LD5537H1 is ROHS compliant / green packaged.

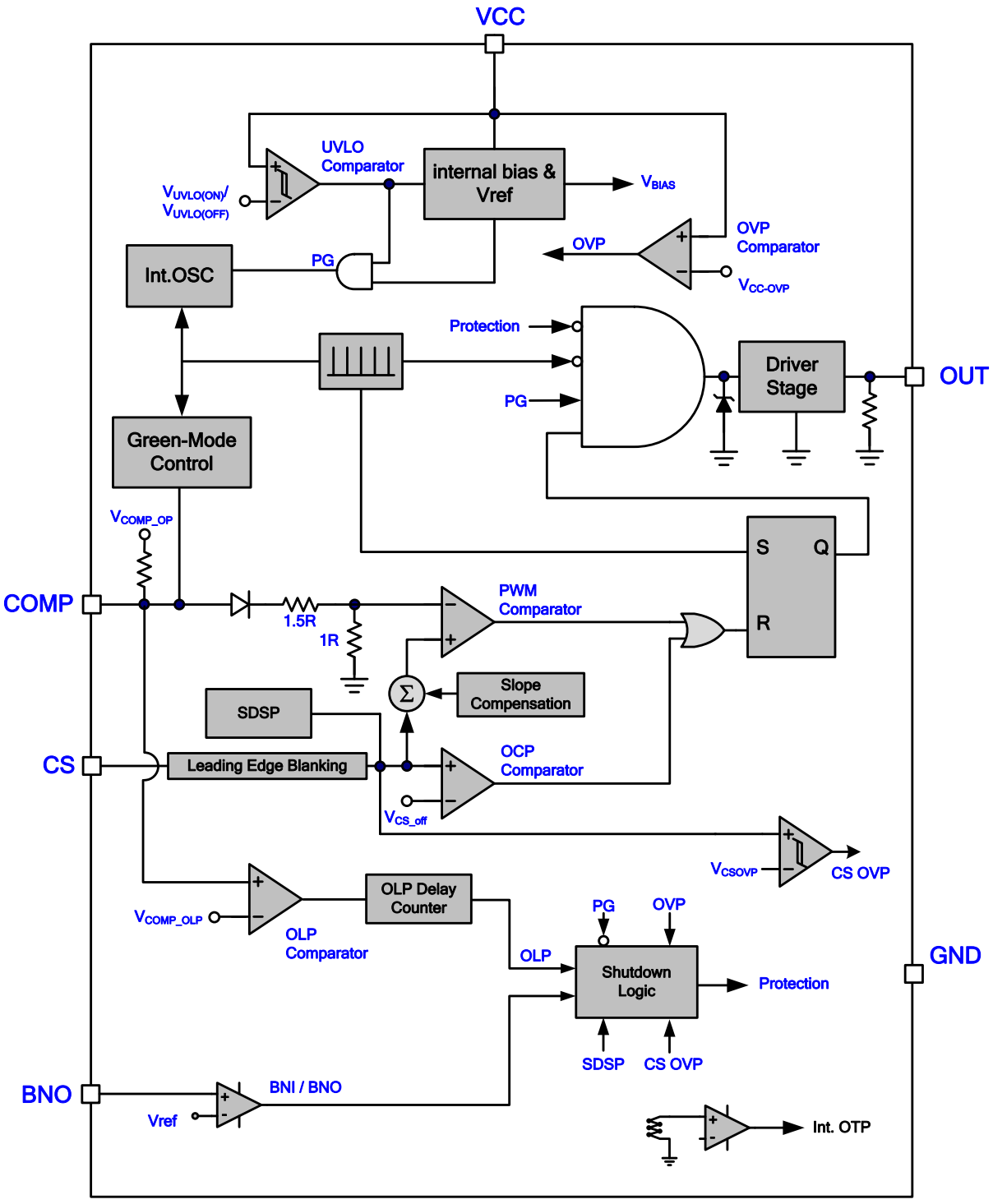
Protection Mode

Product Name	Switching Freq.	OLP	VCC OVP	CS OVP	OSCP	SDSP	BNO Pin	Int. OTP
LD5537H1	65kHz	Latch	Latch	Latch	Latch	Latch	Auto recovery	Auto recovery

Pin Descriptions

SOT-26	NAME	FUNCTION
1	GND	Ground
2	COMP	Voltage feedback pin (same as the COMP pin in UC384X). Connect a photo-coupler to close the control loop and achieve the regulation.
3	BNO	Brownout Protection Pin. Connect a resistor divider between this pin and bridge rectifier of AC input to set the brownout level. If the voltage is less than threshold voltage, the PWM output will be disabled.
4	CS	Current sense pin, connect it to sense the MOSFET current.
5	VCC	Supply voltage pin
6	OUT	Gate drive output to drive the external MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V ~ 30V
COMP, CS, BNO	-0.3V ~ 6V
OUT	-0.3V ~ VCC+0.3V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	200°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	200mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stress above recommended operating conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.5	26.5	V
VCC Capacitor	3.3	10	μF
Start-up resistor Value (AC Side, Half Wave)	540K	2.2M	Ω
COMP Pin Capacitor	1	10	nF
CS Pin Capacitor Value	47	390	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF ~ 0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible.
2. It's also essential to connect a capacitor to COMP to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current	VCC < UVLO(ON)	I_{CC_ST}			3	μA
Operating Current (with 1nF load on OUT Pin)	V_{COMP}=0V, OUT=1nF	I_{CC_OP1}		0.285		mA
	V_{COMP}=1.7V, OUT=1nF	I_{CC_OP2}		2.9		mA
	Auto current protection	I_{CC_OPA1}		0.6		mA
	Latch current protection	I_{CC_OPA2}		0.8		mA
UVLO(OFF)	OUT OFF	VCC_{OFF}	6.5	7.5	8.5	V
UVLO(ON)		VCC_{ON}	15	16	17	V
VCC OVP Level		VCC_{OVP}	27	28	29	V
VCC OVP de-bounce time		T_{VCC_OVP}		8		Cycle
Latch-Off Release Voltage		V_{PDR}	4.1	4.8	5.5	V
Voltage Feedback (Comp Pin)						
Short Circuit Current	V_{COMP}=0V	I_{COMP}		0.116		mA
Open Loop Voltage		V_{COMP_OPEN}		3.15		V
Zero Duty Threshold V_{COMP}		V_{ZDC}		0.5		V
Zero Duty Hysteresis		V_{ZDCH}		100		mV
Current Sensing (CS pin)						
Maximum Input Voltage (V_{CS_OFF})		V_{CS_LIMIT}		0.815		V
Maximum Input Voltage (V_{CS_MIN})	For High Line	V_{CS_MIN}		0.645		V
Leading Edge Blanking Time		T_{LEB}		200		ns
Internal Slope Compensation	0% to D_{MAX}. (Linearly increase) *	V_{SLP_L}		330		mV
Input impedance	*	Z_{CS}	1			MΩ
Delay to Output	*	T_{PD}		100		ns
Gate Drive Output (OUT Pin)						
Output Low Level	VCC =15V, Io=20mA(1)	V_{OL}			1	V
Output High Level	VCC =15V, Io=20mA	V_{OH}	9		14	V
Rising Time	VCC =15V C_L=1000pF	T_r		200		ns
Falling Time	VCC =15V C_L =1000pF	T_f		30		ns
Output High Clamp Level	VCC =18V	V_{O_CLAMP}		11.5		V

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency						
CCM Frequency		F_{CCM}		65		kHz
Frequency Swapping	*	F_{SW_MOD}		±8		%
Green Mode Frequency		F_{SW_GREEN}		24		kHz
Temp. Stability	*	F_{SW_TS}		3	5	%
Voltage Stability	VCC =9V~24V *	F_{SW_VS}			1	%
Maximum Duty	*	D_{MAX}		81		%
Soft Start						
Soft Start Time	V_{CS_OFF} from 0.2V to 0.5V *	T_{SS}		7		ms
OLP (Over Load Protection)						
OLP Trip Level		V_{OLP}	2.65	2.8	2.95	V
OLP delay time	After soft-start	T_{D_OLP}		88		ms
Over Voltage Protection (CS Pin)						
CS OVP Trip Current Level		V_{CSOVP}	0.29	0.31	0.33	V
CS OVP De-bounce Cycle	*	T_{D_CSOVP}		8		Cycle
BNO Pin Auto Protection (BNO Pin)						
Brownout Turn-On Trip Level		V_{BNI}	1	1.05	1.1	V
Brownout Turn-Off Trip Level		V_{BNO}	0.9	0.95	1	V
BNO Pin De-bounce Time		T_{BNO}		75		ms
Internal OTP Protection						
OTP Level	*	T_{UP_OTP}		140		℃
OTP Hysteresis	*	T_{INOTP_HYS}		12		℃
SDSP (Secondary Diode Short Protection)						
SDSP CS Pin Level	Secondary diode short	V_{CS_SDSP}		1.2		V
De-bounce Cycle	*	T_{D_SDSP}		4		Cycle

*: Guaranteed by design.

Typical Performance Characteristic

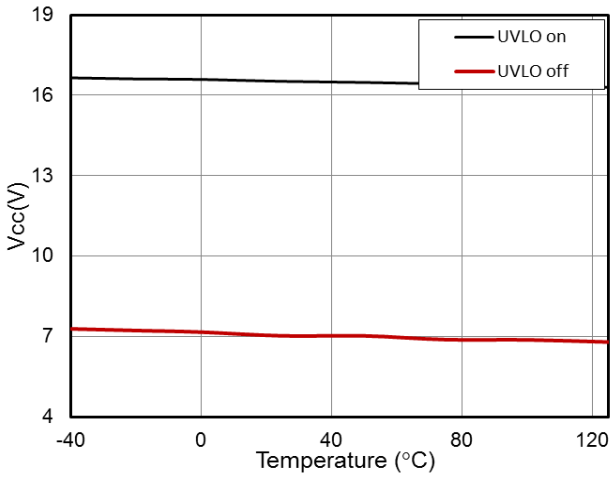


Fig. 1 UVLO Level vs.Temperature

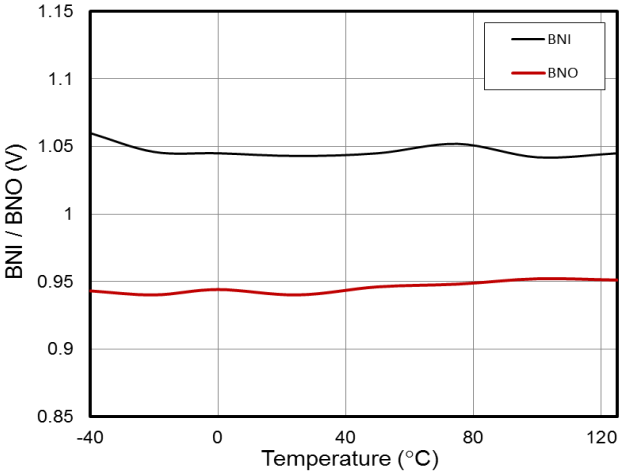


Fig. 2 BNI / BNO vs.Temperature

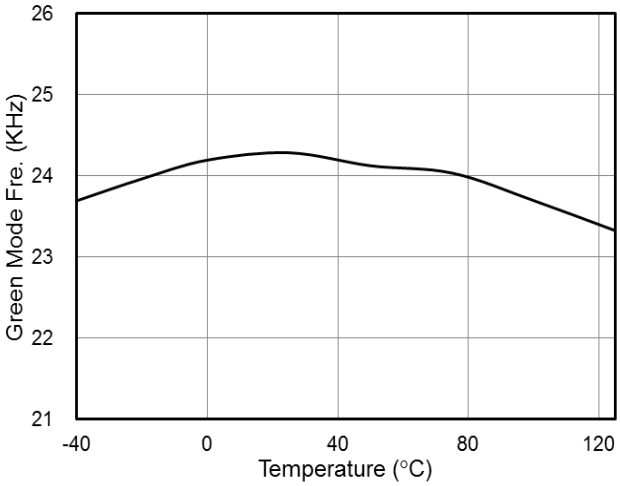


Fig. 3 Green Mode Fre. vs.Temperature

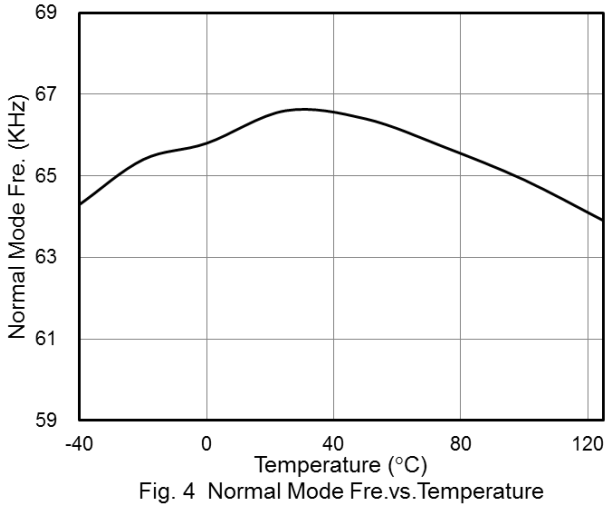


Fig. 4 Normal Mode Fre.vs.Temperature

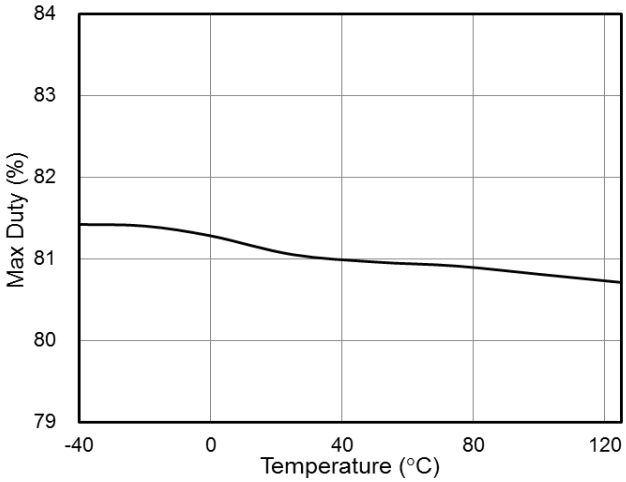


Fig. 5 Max Duty vs.Temperature

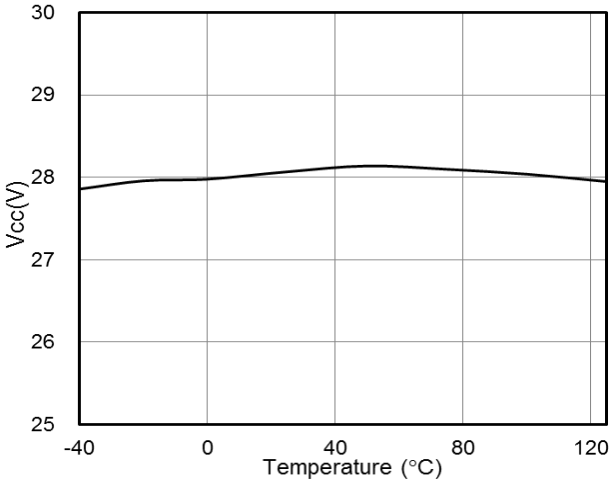


Fig. 6 Vcc OVP Level vs.Temperature

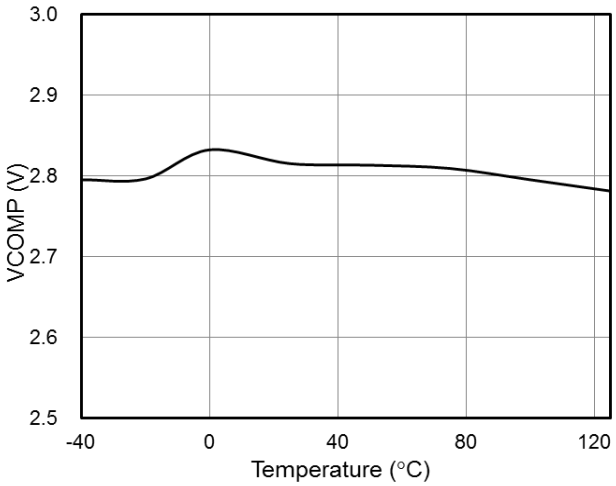


Fig. 7 VOLP vs.Temperature

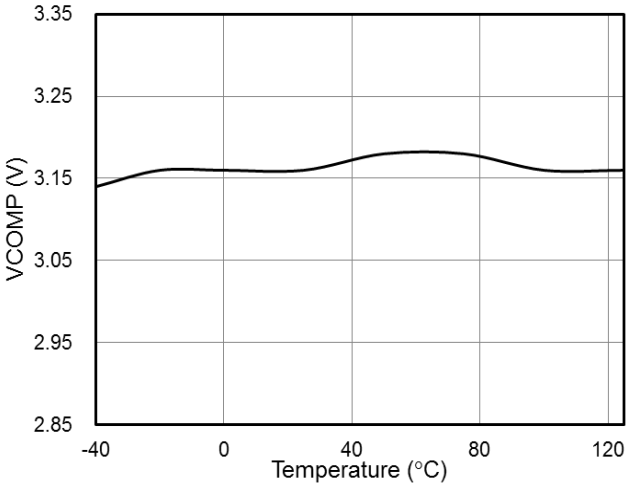


Fig. 8 Open Loop Voltage vs.Temperature

Application Information

Operation Overview

The LD5537H1 meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrates more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD5537H1 PWM controller and further to drive the power MOSFET. As shown in Fig. 9, a hysteresis is built in to prevent the shutdown from the voltage dip during startup.

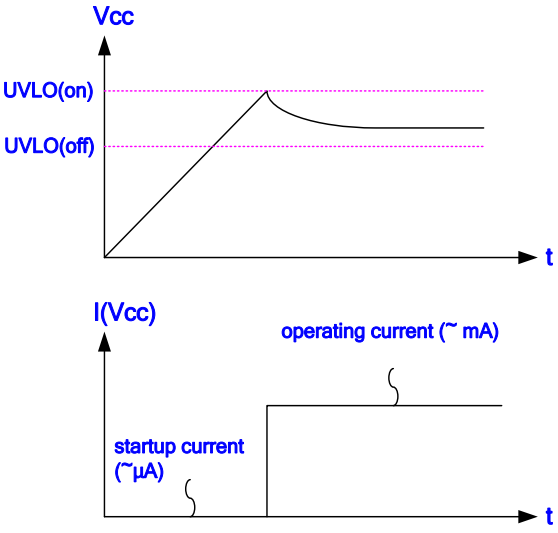


Fig. 9

Startup Current and Startup Circuit

The typical startup circuit to generate VCC of the LD5537H1 is shown in Fig. 10. During the startup transient, the VCC is below UVLO threshold. Before it has sufficient voltage to develop OUT pulse to drive the power MOSFET, R1 will provide the startup current to charge the capacitor C1. Once VCC obtain enough voltage to turn on the LD5537H1 and further to deliver the gate drive signal, it will enable the auxiliary winding of the transformer to provide supply current. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current for LD5537H1 is only 3μA.

If a higher resistance value of the R1 is chosen, it will usually take more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

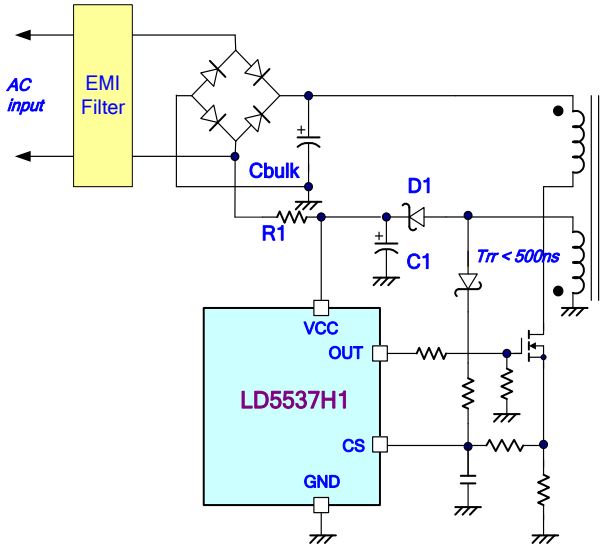


Fig. 10

Current Sensing and Leading-Edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD5537H1 detect the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit.

In general, the power converter will provide more current when input voltage alters to high due to the signal propagation delay. This can be compensated through LD5537H1. It's controlled by varying the current limit with the duty cycles in corresponding to V_{CS_OFF}. As shown in

Fig. 11, V_{CS_OFF} (corresponding to current limit) is in direct proportion to duty ratio in a certain segment and is fixed at high or low if duty ratio is respectively over or below threshold values. As a result, the current limit will be lowered at high-line inputs. This compensation control mechanism is developed with patents pending by Leadtrend Technology.

The maximum voltage threshold of the current sensing pin is set at 0.815V for low-line input. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.815}{R_{CS}}$$

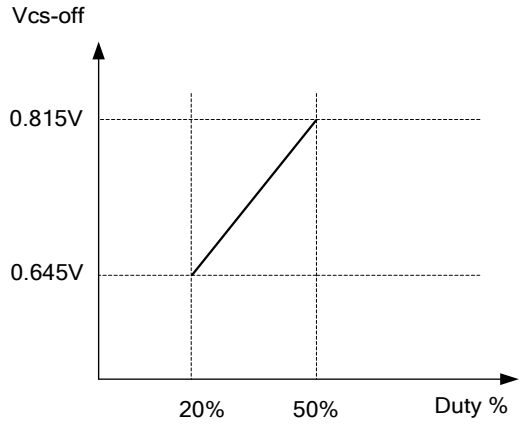


Fig. 11

A 200ns leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spike is less than 200ns and the negative spike on the CS pin doesn't exceed -0.3V, it could remote the R-C filter (as shown in the Fig. 12).

However, the total pulse width of the turn-on spike is decided by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in Fig. 13) for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

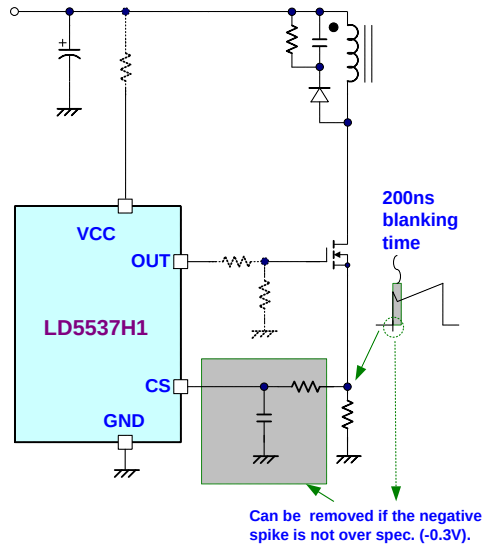


Fig. 12

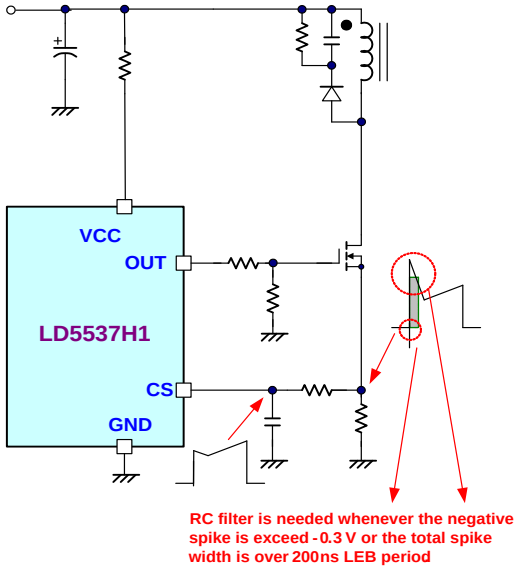


Fig. 13

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 250/-500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD5537H1 is limited to 81% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD5537H1. Similar to UC3842, the LD5537H1 would carry a diode voltage offset at the stage to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{-(PWM\ COMPARATOR)} = \frac{RB}{RA+RB} \times V_{COMP}$$

A pull-high resistor is embedded internally and can be eliminated externally.

Oscillator and Switching Frequency

The LD5537H1 is implemented with frequency swapping function which helps the power supply designers to both optimize EMI performance and lower system cost. The switching frequency substantially centers at 65kHz, and swap between a range of ±8kHz.

Green-Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property. Fig. 14 shows the characteristics of the switching frequency vs. the COMP pin voltage (V_{COMP}).

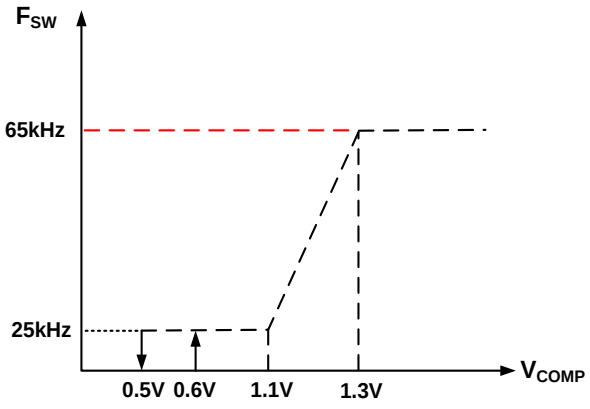


Fig. 14

On/Off Control

The LD5537H1 can be turned off by pulling COMP pin lower than 0.5V. The gate output pin of the LD5537H1 will be disabled immediately under such condition. The off-mode can be released when the pull-low signal is removed.

Internal Slope Compensation

In the conventional applications, the problem of the stability is a critical issue for current mode controlling, when it operates over 50% duty-cycle. As UC384X, It takes slope compensation from injecting the ramp signal of the RT/CT pin through a coupling capacitor. It therefore requires no extra design for the LD5537H1 since it has integrated it already.

Output Short Circuit Protection (OSCP) – Latch

The OSCP function can prevent the damage from output short circuit. Once the output is shorted, Vout and VCC drop immediately, which always reflects the auxiliary winding during the gate off region. According to the close loop control, COMP voltage will pull high in the meanwhile. If the V_{COMP} pulls higher than 2.8V over 15ms and VCC drops below 9.6V. At this time, the OSCP protection will be triggered and turn off the gate driving.

Over Load Protection (OLP) – Latch

To protect the circuit from damage in over-load condition and short or open-loop condition, the LD5537H1 is implemented with smart OLP function. LD5537H1 also features latch function; see Fig. 15 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (V_{COMP}). When the V_{COMP} ramps up to the OLP threshold of 2.8V and continues over OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

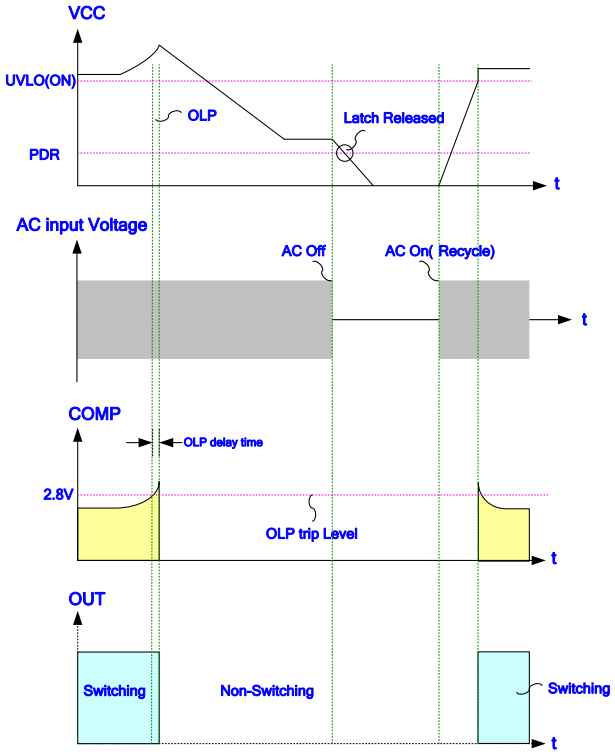


Fig. 15

Over Voltage Protection (OVP) on VCC Pin – Latch

The V_{GS} ratings of the nowadays power MOSFETs are often limited up to max. 29V. To prevent the V_{GS} from the fault condition, LD5537H1 is implemented with an OVP function on VCC. Whenever the VCC voltage is higher than the OVP threshold voltage, the LD5537H1 output gate drive circuit will be shutdown simultaneously to latch off the power MOSFET as Fig. 16.

On the contrast, if the voltage on VCC pin drops below PDR and starts AC-recycling again, it will soon resume to normal operation.

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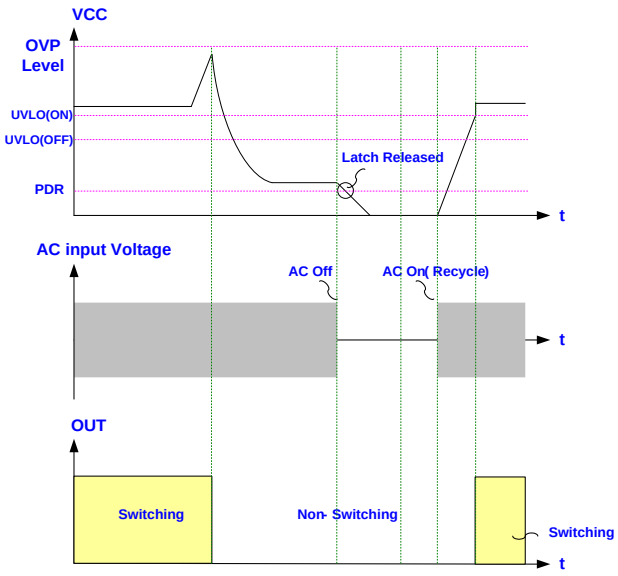


Fig. 16

Output Over Voltage Protection (CS OVP) on CS Pin – Latch

An output overvoltage protection is implemented in the LD5537H1, as shown in Fig. 17 and 18. It senses the auxiliary voltage via the divided resistors. The auxiliary winding voltage is reflected from secondary winding and therefore the flat voltage on the CS/OVP pin is proportional to the output voltage. LD5537H1 can sample this flat voltage level after a delay time to perform output over voltage protection. This delay time is used to ignore the voltage ringing from leakage inductance of PWM transformer. The sampling voltage level is compared with internal threshold voltage 0.31V. If the sampling voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP events. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. However, when typically 8 cycles of subsequent OVP events are detected, the OVP circuit switches the power MOSFET off.

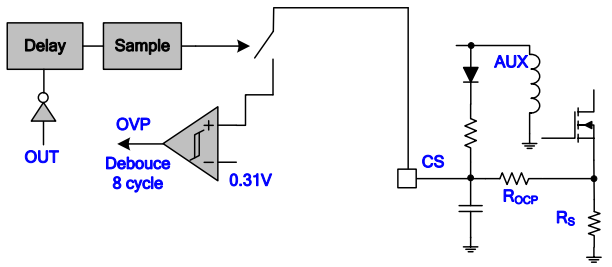


Fig. 17

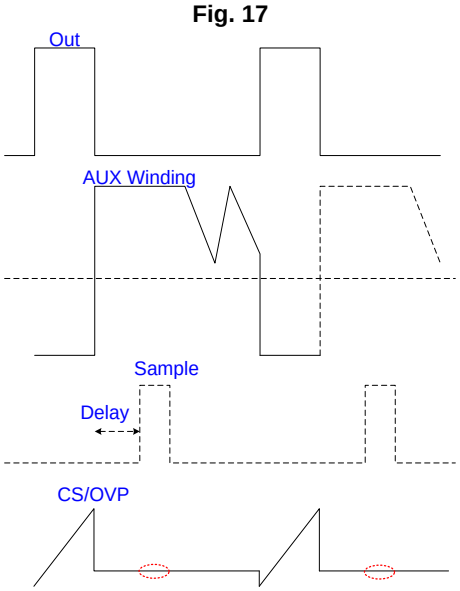


Fig. 18

Brown-out Protection (BNO)

The LD5537H1 is programmable to set the brownout protection point though BNO pin. The voltage across the BNO pin is proportional to bridge rectifier of AC input. A brownout comparator is implemented to detect the abnormal line condition. As soon as the condition is detected, it will shut down the controller to prevent the damage. Fig. 19 shows the operation. When VBNO falls below 0.95V, the gate output will remain off even VCC has already achieved UVLO(ON). It therefore makes VCC hiccup between UVLO(ON) and UVLO(OFF). Unless the line voltage is enough to pull VBNO larger than 1.05V, the gate output will not start switching even when the next UVLO(ON) is tripped. A hysteresis is implemented to prevent the false trigger during turn-on and turn-off. LD5537H1 can floating this pin If haven't need BNO function.

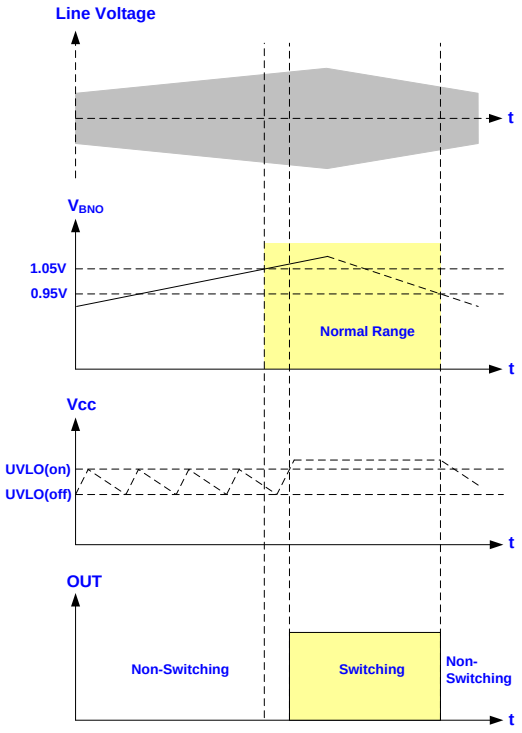


Fig. 19

Secondary Diode Short Protection (SDSP) – Latch

The method that the LD5537H1 judges the logic of SDSP is described briefly as follows. When VCS is higher than 1.2V, it will reduce the frequency first, even the Ton < LEB+T_{PD}. When the count is up to 4 times, its gate will be turned-off, shown as Fig. 20.

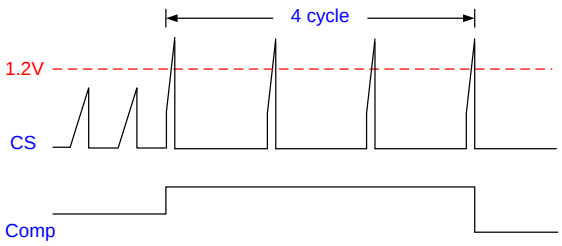


Fig. 20

Fault Protection

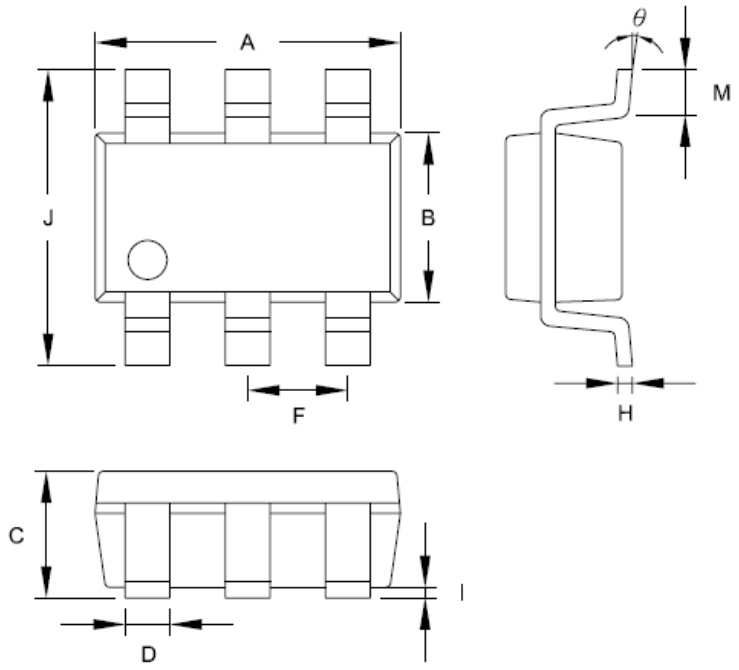
There are several critical protections integrated in the LD5537H1 to prevent from damage to the power supply. Those damages usually come from open or short conditions on the pins of LD5537H1.

In case under such conditions listed below, the gate output will turn off immediately to protect the power circuit.

1. CS pin floating
2. COMP pin floating

Package Information

SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Revision History

REV.	Date	Change Notice
00	01/03/2019	Original Specification