Green-Mode PWM Controller with Frequency Swapping and Integrated Protections

REV. 01

General Description

The LD5538 is built-in with several functions, protection and EMI-improved solution in a tiny package. It takes less components counts or circuit space, especially ideal for those total solutions of low cost.

The implemented functions include low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. It also features more protections like OPP (Over Power Protection), OCP (Over Current Protection), OSCP (Output Short Circuit Protection) and OVP (Over Voltage Protection) to prevent circuit damage occurred under abnormal conditions.

Furthermore, the Frequency Swapping function is to reduce the noise level and thus helps the power circuit designers to easily deal with the EMI filter design by spending minimum amount of component cost and developing time.

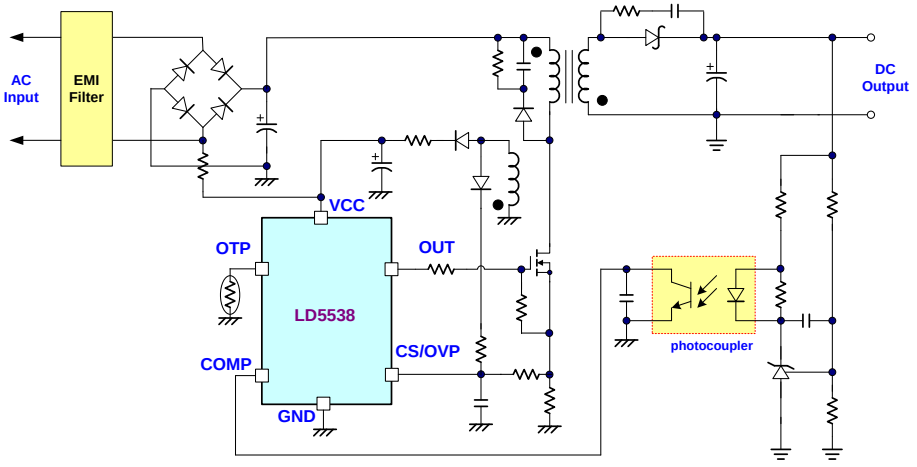
Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (<1.5μA)
- Current Mode Control
- Green Mode Control
- UVLO (Under Voltage Lockout)
- Variable Frequency Technology around 130KHz
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Frequency Swapping
- Internal Slope Compensation
- OVP (Over Voltage Protection) on VCC Pin
- OTP (Over Temperature Protection) through a NTC
- OPP (Over Power Protection)
- OCP (Over Current Protection)
- OSCP (Short Circuit Protection)
- SDSP (Secondary Diode Short Protection)
- 300mA/-500mA Driving Capability

Applications

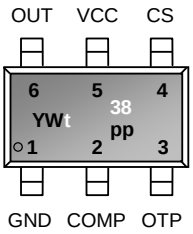
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

Typical Application



Pin Configuration

SOT-26 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005…..)
WW, W : Week code
PP : Production code
t38 : LD5538

Ordering Information

Part number	Package	Top Mark	Shipping
LD5538 GL	SOT-26	YWt/38	3000 /tape & reel

The LD5538 is ROHS compliant/Green Packaged.

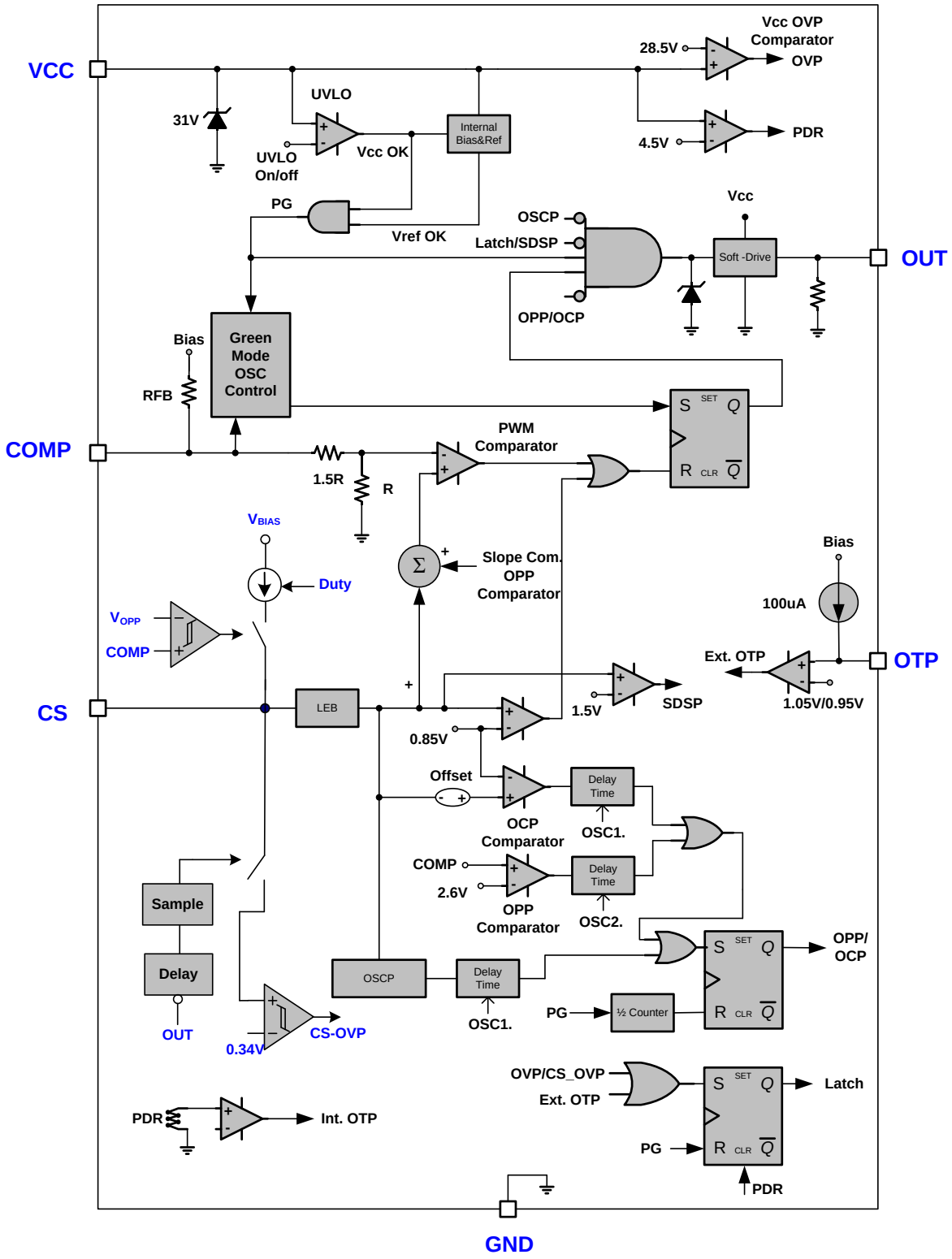
Protection Mode

Switching Freq.	VCC OVP	OPP	OCP	OSCP	Int. OTP	OTP Pin	CS Pin OVP
65k/130KHz	Latch	Auto-Restart	Auto-Restart	Auto-Restart	Auto-Restart	Latch	Latch

Pin Descriptions

SOT-26	NAME	FUNCTION
1	GND	Ground
2	COMP	Voltage feedback pin (same as the COMP pin in UC384X). Connect a photo-coupler to close the control loop and achieve the regulation.
3	OTP	Pull this pin below 0.95V to shut down the controller into latch mode until the AC resumes power-on. Connecting this pin to ground with NTC will achieve OTP protection. Let this pin float or connect a 100kΩ resistor to disable the latch protection.
4	CS	Current sense pin, connect it to sense the MOSFET current.
5	VCC	Supply voltage pin
6	OUT	Gate drive output to drive the external MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V ~ 30V
COMP, OTP, CS	-0.3V ~ 7V
OUT	-0.3V ~ VCC+0.3V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	200°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	200mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.5	26.5	V
VCC Capacitor	3.3	10	μF
Start-up resistor Value (AC Side, Half Wave)	400K	1.8M	Ω
COMP Pin Capacitor	1	10	nF
CS Pin Capacitor Value	47	390	pF
CS OVP Diode Junction Capacitor		8	pF

Note:

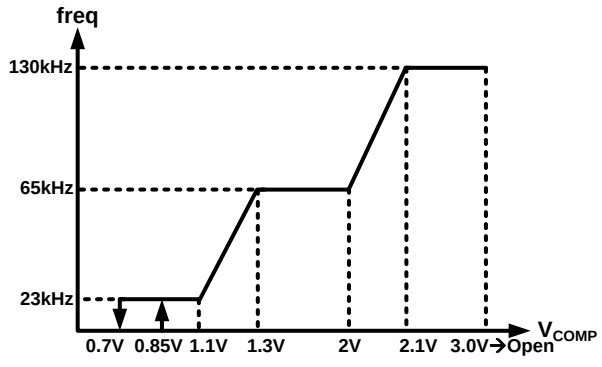
1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF ~ 0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. It's also essential to connect a capacitor to COMP to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

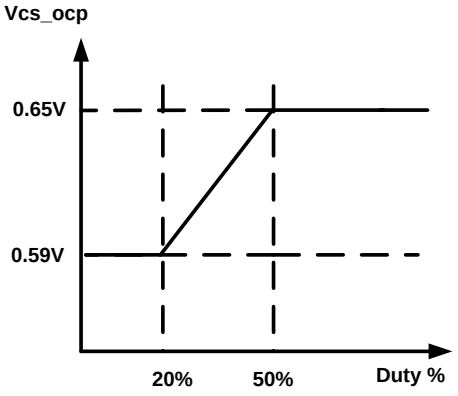
(For typical T_J = +25°C, for min/max values T_J = -40°C ~ +125°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current	VCC < UVLO(ON)	I_{STUP}	0.5	1	1.5	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V	I_{VCC_0V}	0.2	0.25	0.3	mA
	V_{COMP}=2V	I_{VCC_2V}	1.70	1.95	2.1	mA
Holding Current	VCC=15V(latched)	I_{HD_15V}		850		μA
	VCC=10V(latched)	I_{HD_10V}		410		μA
	VCC=5V(latched)	I_{HD_5V}		40		μA
	Auto mode.	I_{HD_AUTO}		620		μA
UVLO(OFF)		$V_{UVLO(OFF)}$	6.5	7.5	8.5	V
UVLO(ON)		$V_{UVLO(ON)}$	14.5	16	17.5	V
OVP Level		V_{OVP}		28.5		V
OVP pin de-bounce time		T_{DE_OVP}		8		cycle
Latch-Off Release Voltage		V_{LCH_OFF}		4.5		V
Voltage Feedback (COMP Pin)						
Short Circuit Current	V_{COMP}=0V	I_{COMP_0V}		0.125		mA
Open Loop Voltage	COMP pin open	I_{COMP_OP}		3		V
Peak Mode Threshold VCOMP		V_{COMP_PK}		2.1		V
Peak Mode Down Threshold		V_{COMP_DN}		2.0		V
Green Mode Threshold VCOMP		V_{COMP_GN}		1.3		V
Green Mode Down Threshold VCOMP, FSW_DN		$V_{COMP\_GN\_DN}$		1.1		V
Zero Duty Threshold VCOMP		V_{ZD}		0.7		V
Zero Duty Hysteresis		V_{ZD_H}		150		mV
IOPP Threshold VCOMP	Duty≦20%	V_{IOPP}		1.9		V
OTP Pin Latch Protection						
OTP Pin Source Current	(VCC=11V-25V)	I_{OTP}	92	100	108	μA
Turn-On Trip Level		V_{OTP_ON}		1.05		V
Turn-Off Trip Level		V_{OTP_OFF}		0.95		V
OTP LATCH pin de-bounce time	Enable Low to High	$T_{D\_OTP\_ON}$	150	250	350	μs
	Enable High to Low	$T_{D\_OTP\_OFF}$	350	450	550	μs

PARAMETER	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS
Current Sensing (CS Pin)							
Limit Voltage, V_{CS_OFF}	Vsetting>0.34V		$V_{CS\_OFF\_H}$	0.8	0.85	0.9	V
	Vsetting<0.34V		$V_{CS\_OFF\_L}$	0.75	0.80	0.85	V
OCP Voltage for Low line, V_{CS}	Duty≦50%	T_J = +25°C	V_{CS_L}	0.61	0.65	0.689	V
OCP Voltage for High line, V_{CS}	Duty≦20%	T_J = +25°C	V_{CS_H}	0.554	0.59	0.625	V
OPP Compensation Current	Duty≧50%		I_{OPP_50}	0		5	μA
	Duty≦20%	Vsetting>0.34V	$I_{OPP\_20\_H}$		210		μA
	Duty≦20%	Vsetting<0.34V	$I_{OPP\_20\_L}$		550		μA
Leading Edge Blanking Time			T_{LEB}		220		ns
Internal Slope Compensation	0% to D_{MAX}. (Linearly increase)		V_{SLOPE}		300		mV
Input impedance			Z_{IN}	1			MΩ
Delay to Output			T_D	50		100	ns
OVP CS pin							
OVP Trip Current Level			V_{CS_OVP}	0.313	0.34	0.367	V
De-bounce Cycle			T_{DE_OVP}		8		Cycle
Sample Delay Time	(1)		T_{CS_D}	1.87	2.2	2.53	μs
Oscillator for Switching Frequency							
Frequency, FREQ	Normal mode	T_J = +25°C	F_{SW}	60	65	70	kHz
	Peak mode	T_J = +25°C	F_{SW_PK}	120	130	140	kHz
Green Mode Frequency, FREQG	Green mode		F_{SW_GRN}	20	23	26	kHz
Trembling Frequency			F_{TREMB}		±6		%
Voltage Stability	(VCC=11V-25V)		V_{STAB}	0		1	%



V_{COMP} vs. PWM Frequency



Duty vs. OCP level

Electrical Characteristics

(For typical T_A = +25°C, for min/max values T_A = -40°C ~ +125°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Gate Drive Output (OUT Pin)						
Output Low Level	VCC=15V, I_O=20mA	V_{O_L}			1	V
Output High Level	VCC=15V, I_O=20mA	V_{O_H}	8		15	V
Output High Clamp Level	VCC=20V	V_{O_HC}	11	12	13	V
Rising Time	Load Capacitance=1000pF	T_r	-	150	250	ns
Falling Time	Load Capacitance=1000pF	T_f		50	100	ns
Source capability(1)	Load Capacitance=33nF	I_{O_SOURCE}		300		mA
Sink capability(1)	Load Capacitance=33nF	I_{O_SINK}		500		mA
Max. Duty		D_{MAX}		85		%
OPP (Over Power Protection)						
OPP Trip Level		V_{COMP_OPP}		2.6		V
OPP Delay Time	Exclude soft start time	T_{D_OPP}		23		ms
OCP (Over Current Protection)						
OCP Delay Time		T_{D_OCP}		110		ms
OSCP (Output Short Circuit Protection)						
OSCP Trip Level	Vsetting>0.34V	$V_{CS\_OFF\_H}$	0.8	0.85	0.9	V
	Vsetting<0.34V	$V_{CS\_OFF\_L}$	0.75	0.80	0.85	V
De-bounce Cycle		T_{D_OSCP}		8		Cycle
SDSP (Secondary Diode Short Protection)						
SDSP CS Pin Level	Secondary diode short	V_{CS_SDSP}	1.4	1.5	1.6	V
De-bounce Cycle		T_{D_SDSP}		8		Cycle
On Chip OTP (Over Temperature)						
OTP Level(1,2)		T_{OTP}		140		°C
OTP Hysteresis(1,2)		T_{H_OTP}		30		°C
Soft Start Duration						
Soft Start Duration		T_{SS}		7		ms

Notes:

1. Guaranteed by design.
2. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.

Typical Performance Characteristics

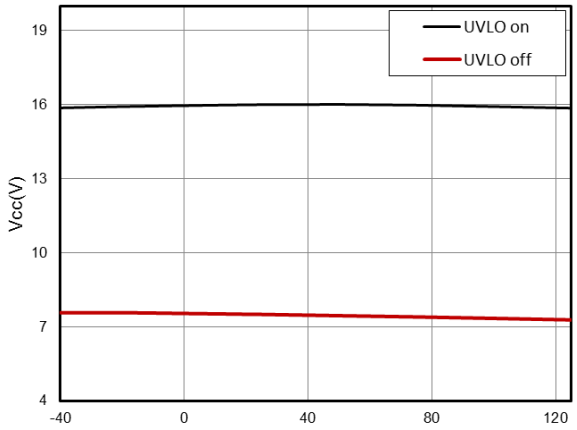


Fig. 1 UVLO level vs.Temperature

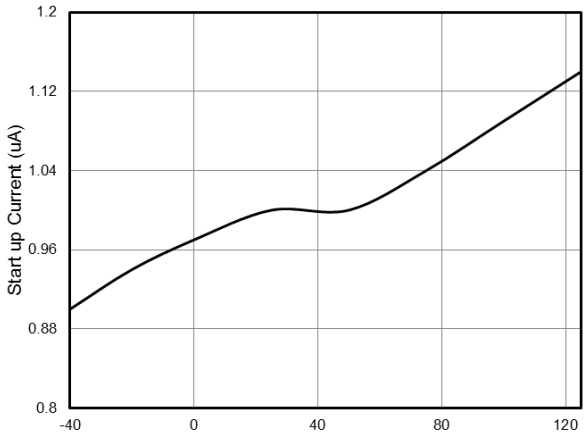


Fig. 2 Start up Current vs.Temperature

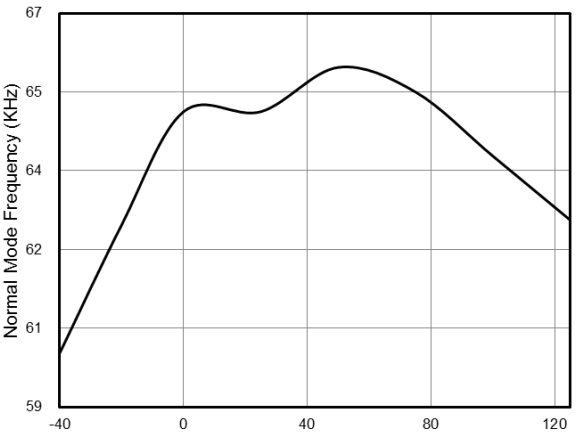


Fig. 3 Normal Mode Frequency vs.Temperature

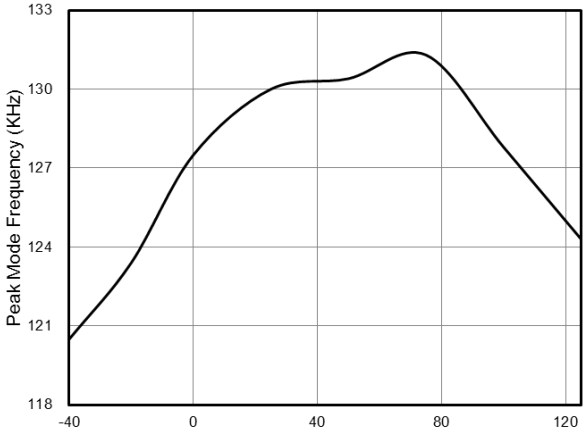


Fig. 4 Peak Mode Frequency vs.Temperature

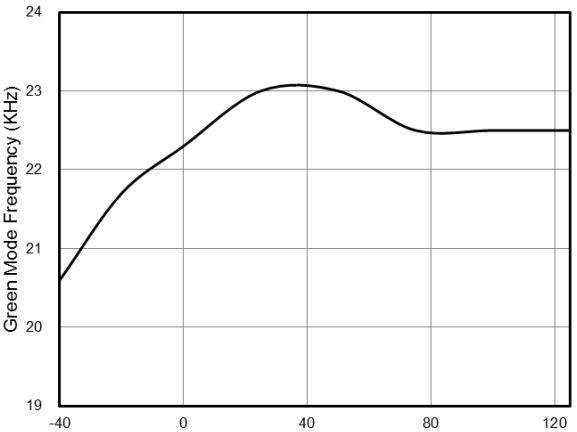


Fig. 5 Green Mode Frequency vs.Temperature

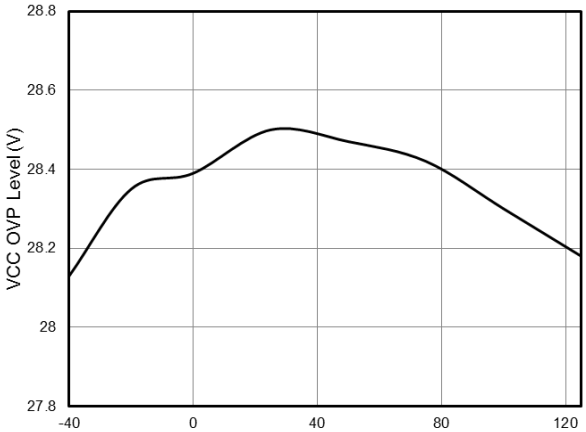


Fig. 6 VCC OVP Level vs.Temperature

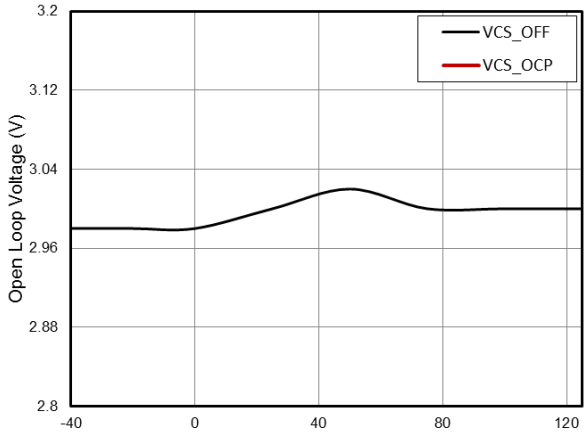


Fig. 7 Open Loop Voltage vs.Temperature

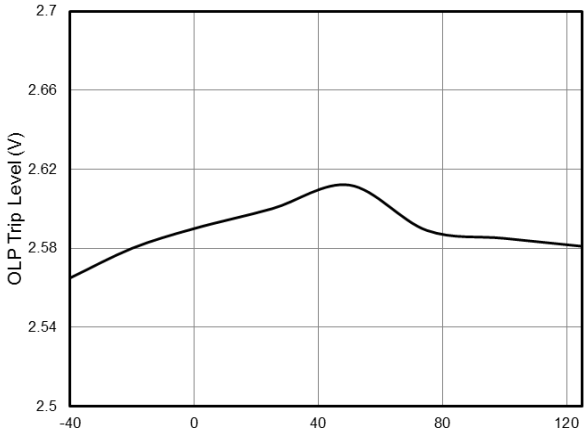


Fig. 8 OLP Trip Level vs.Temperature

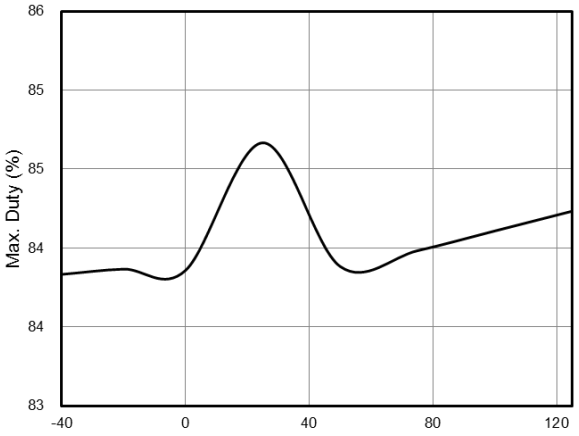


Fig. 9 Max. Duty vs.Temperature

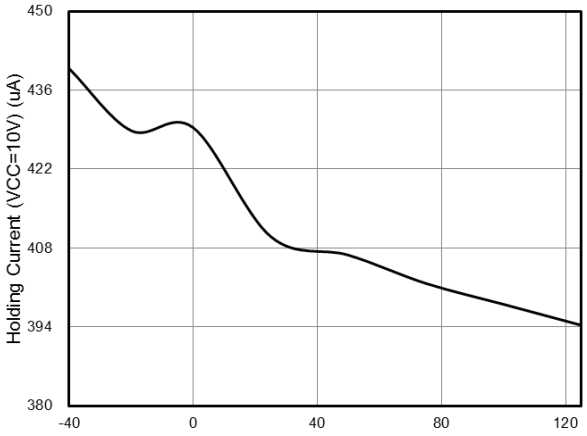


Fig. 10 Holding Current (VCC=10V) vs.Temperature

Application Information

Operation Overview

The LD5538 meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD5538 PWM controller and further to drive the power MOSFET. As shown in Fig. 11, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.0V and 7.5V, respectively.

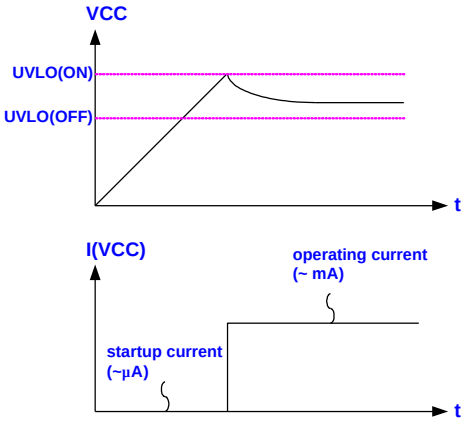


Fig. 11

Startup Current and Startup Circuit

The typical startup circuit to generate V_{CC} of the LD5538 is shown in Fig. 12. During the startup transient, the V_{CC} is below UVLO threshold. Before it has sufficient voltage to develop OUT pulse to drive the power MOSFET, R1 will provide the startup current to charge the capacitor C1. Once V_{CC} obtain enough voltage to turn on the LD5538 and further to deliver the gate drive signal, it will enable the auxiliary winding of the transformer to provide supply current. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current for LD5538 is only 1.5μA.

If a higher resistance value of the R1 is chosen, it will usually take more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

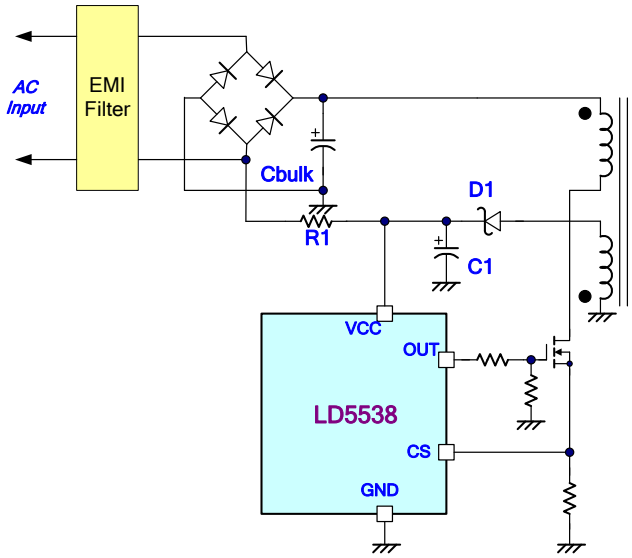


Fig. 12

Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 13, the LD5538 detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

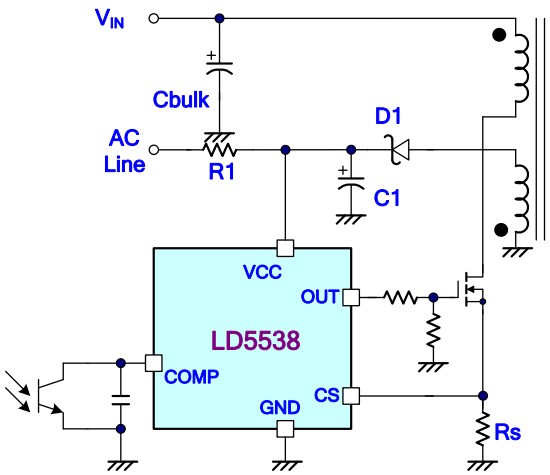


Fig. 13

A 220nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spikes is less than 220nS and the negative spike on the CS pin below -0.3V, the R-C filter is free to eliminate. (As shown in Fig.14).

However, the total pulse width of the turn-on spike is determined according to output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in Fig. 15) for larger power application to avoid the CS pin being damaged by the negative turn-on spike.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 300/-500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD5538 is limited to 85% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD5538. Similar to UC3842, the LD5538 would carry a diode voltage offset at the stage to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{(PWM_{COMPARATOR})} = \frac{RB}{RA+RB} \times V_{COMP}$$

A pull-high resistor is embedded internally and can be eliminated externally.

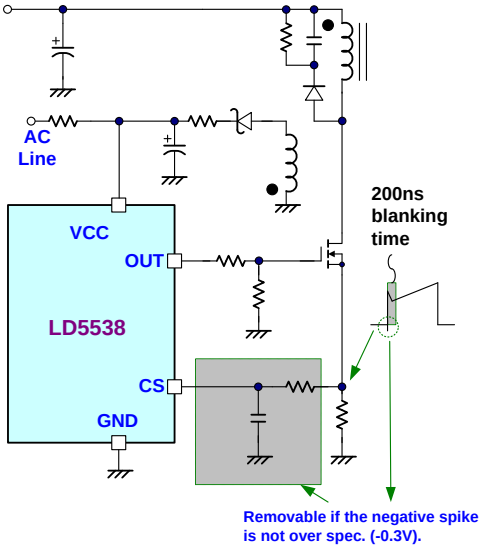


Fig. 14

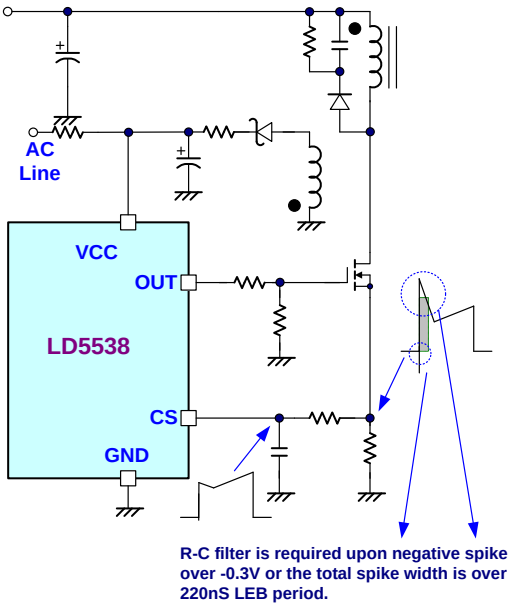


Fig. 15

Internal Slope Compensation

In the conventional applications, the problem of the stability is a critical issue for current mode controlling, when it operates over 50% duty-cycle. As UC384X, It takes slope compensation from injecting the ramp signal of the RT/CT pin through a coupling capacitor. It therefore requires no extra design for the LD5538 since it has integrated it already.

On/Off Control

The LD5538 can be turned off by pulling COMP pin lower than 0.7V. The gate output pin of the LD5538 will be disabled immediately under such condition. The off-mode can be released when the pull-low signal is removed.

Over Power Protection (OPP) - Auto Restart Mode

To protect the circuit from damage due to over-power condition and short or open-loop condition, the LD5538 is implemented with smart OPP function. It also features auto recovery function; see Fig. 16 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the VCOMP ramps up to the OPP threshold of 2.6V and continues over OPP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

Over Current Protection (OCP) - Auto Restart Mode

When the switching current is higher than the OCP threshold, the internal counter counts down. When the total accumulated counting time is more than 110ms, the controller triggers the OCP. This protection is auto-recovery.

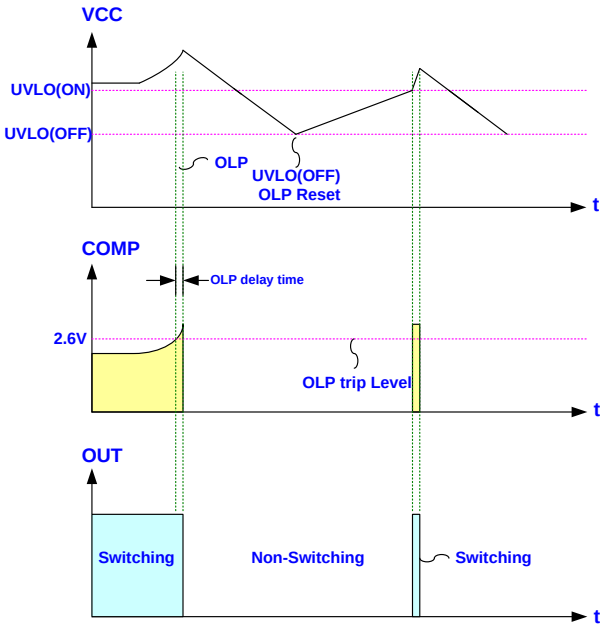


Fig. 16

OSCP (Output Short Circuit Protection) - Auto Restart Mode

Even when the output shorts to GND, there's no way to turn off the signal unless the following four conditions are met.

1. The CS is higher than limit voltage.
2. The COMP voltage is higher than 2.6V
3. This duration is greater than 8 cycles.
4. Turn on time is lower than 1μs.

The out signal could not be charged either, if it fails to meet the four conditions.

Once the protection is triggered, switching is terminated and the MOSFET remains off.

OVP (Over Voltage Protection) on VCC – Latch Mode

The VCC OVP function of LD5538 is in latch mode. As soon as the voltage of the VCC pin rises above OVP threshold, the output gate drive circuit will be shut down

simultaneously to latch off the power MOSFET. On the contrast, if the voltage on VCC pin drops below OVP threshold and starts AC-recycling again, it will soon resume to normal operation. Fig. 17 shows its operation

Otherwise, when the OVP condition is removed, the VCC level will be resumed and the output will automatically return to the normal operation.

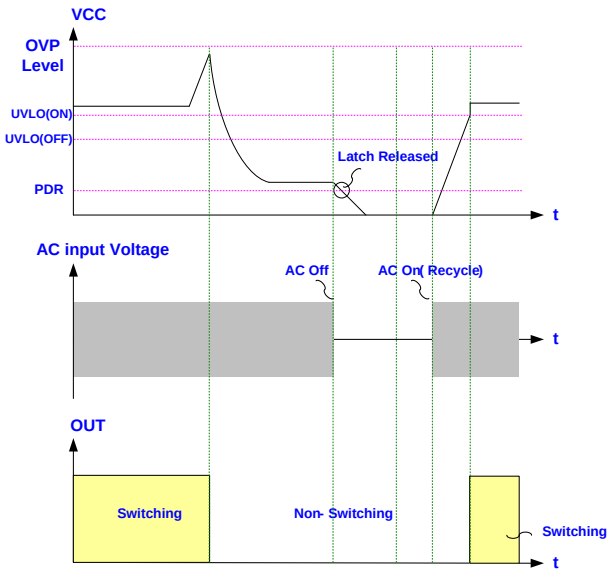


Fig. 17

OTP Pin - Latch Mode

To protect the power circuit from damage due to system failure, over temperature protection (OTP) is required. The OTP circuit is implemented to sense a hot-spot of power circuit like power MOSFET or output rectifier. It can be easily achieved by connecting a NTC with OTP pin of LD5538. As the device temperature or ambient temperature rises, the resistance of NTC decreases. So, the voltage on the OTP pin could be written as below.

$$V_{OTP} = 100\mu A \cdot R_{NTC}$$

When the V_{OTP} is lower than the defined voltage threshold (typ. 0.95V), LD5538 will shut down the gate output and latch off the power supply. There are 2 conditions required to restart it successfully. First, cool down the circuit so that NTC resistance will increase and raise V_{OTP} up above 1.05V. Then, remove the AC power cord and restart AC power-on recycling.

Adjustable Over Power Compensation (CS/OVP Pin)

In general, the power converter can deliver more current at high input voltage than the low input voltage. To compensate this, an offset voltage is added to the CS signal by an internal current source (I_{OCP}) and an external resistor (R_{OPP}) in series between the sense resistor (Rs) and the CS/OVP pin, as shown in Fig. 18. By choosing the value of the resistor in series with the CS pin, the amount of compensation can be adjusted. The value of I_{OPP} depends on the duty cycle of OUT pin. The equation of I_{OPP} is decreased as:

$$I_{OPP} = \begin{cases} (0.5 - Duty) \cdot 1.83mA & (0.2 < Duty < 0.5) \\ 0uA & (Duty \geq 0.5) \\ 550uA & (Duty \leq 0.2) \end{cases}$$

Since in light load conditions this offset is in the same order of magnitude as the current sense signal, it must be removed. Therefore the compensation current is only added when the COMP voltage is higher than 1.9V, as shown in Fig. 19.

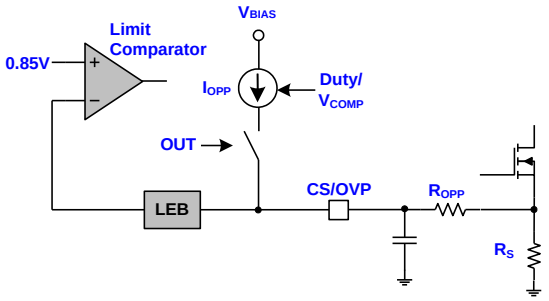


Fig.18

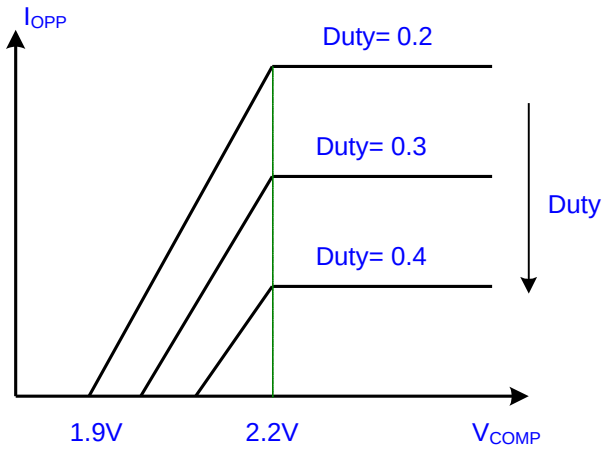


Fig. 19

Output Over Voltage Protection (CS/OVP Pin) - Latch Mode

An output overvoltage protection is implemented in the LD5538, as shown in Fig. 20. This works for the LD5538 by sensing the auxiliary voltage via the divided resistors. The auxiliary winding voltage is reflected from secondary winding and therefore the flat voltage on the CS/OVP pin is proportional to the output voltage. LD5538 can sample this flat voltage level after a delay time to perform output over voltage protection. This delay time is used to ignore the voltage ringing from leakage inductance of PWM transformer. The sampling voltage level is compared with internal threshold voltage 0.34V. If the sampling voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP events. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. However, when typically 8 cycles of subsequent OVP events are detected, the OVP circuit switches the power MOSFET off. As the protection is latched, the converter only restarts after the internal latch is reset.

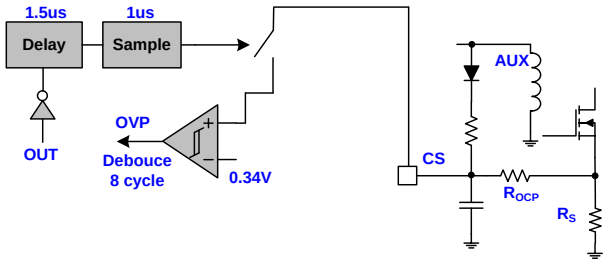


Fig. 20

Oscillator and Switching Frequency

The LD5538 is implemented with Frequency Swapping function which helps the power supply designers to both optimize EMI performance and lower system cost. The switching frequency substantially centers at 65KHz, and swap between a range of ±6%.

Green-Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property.

Fault Protection

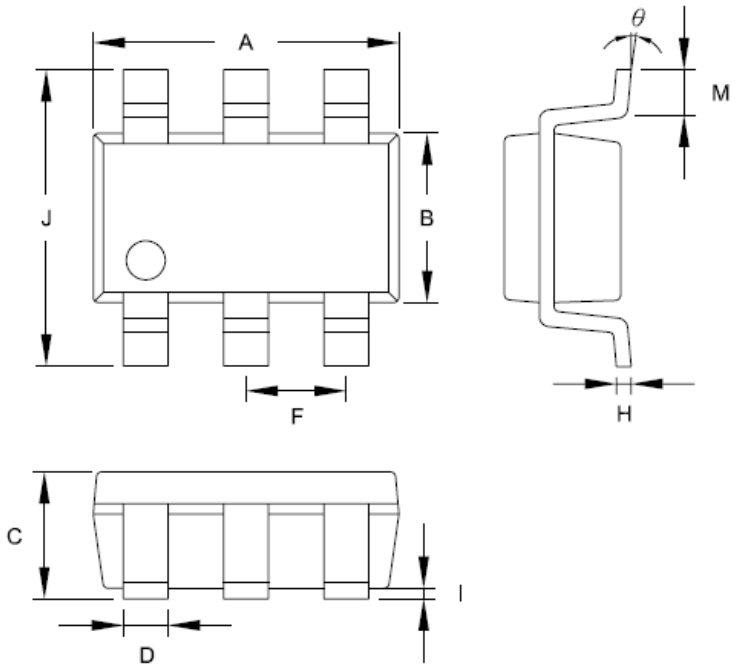
There are several critical protections integrated in the LD5538 to prevent from damage to the power supply. Those damages usually come from open or short conditions on the pins of LD5538.

In case under such conditions listed below, the gate output will turn off immediately to protect the power circuit.

1. CS pin floating
2. COMP pin floating

Package Information

SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	03/16/2016	Original Specification
01	09/29/2016	1. Modify COMP, OTP, CS absolute maximum ratings. 2. Add T_{CS_D} specification.