# Primary-Side Quasi-Resonant Controller, Operating in CV/CC Mode

*REV. 00*

## General Description

The LD5718AC is a primary-side Quasi-Resonant controller capable of operating in CV/CC mode for small to medium power AC/DC charger and adapter. When paired with LD8108A, the LD5718AC will support speedy charger design for MediaTek Pump Express Plus™ based and Qualcomm® Quick Charge™ 2.0 based protocol. Using Leadtrend Speedy Charge™ technology, it will be easy to minimize the component counts.

The LD5718AC can be programmed constant voltage output which only require single photo-coupler by LD8108. Also, the LD5718AC features external/internal OTP (Over Temperature Protection), wide-range and output voltage level OVP (Over Voltage Protection)… etc., to prevent the circuit from being damaged under abnormal conditions.

The LD5718AC is available in a SOP8 package.

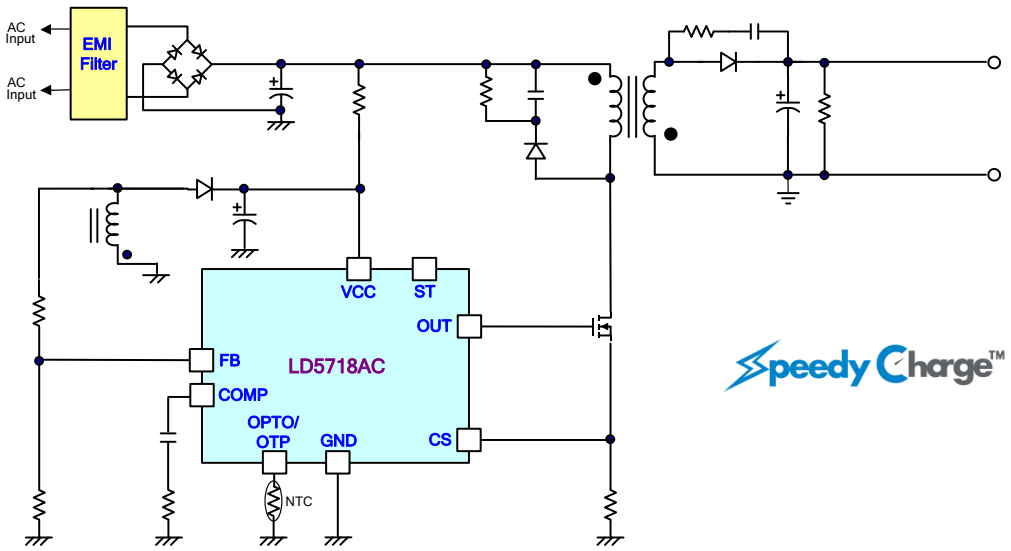
## Features

- Speedy Charge™ technology
- Normally 5V output
- Programming output voltage from 5V to 12V
- Meet DoE level-VI CoC V5 tier2 efficiency
- Specificated constant current control
- Adjustable load regulation compensation
- Built-in HV start-up control for depletion NMOS
- Ultra-low start-up current 1.5μA Max.
- LEB (Leading-Edge Blanking) on CS Pin
- OVP (Over Voltage Protection) on VCC

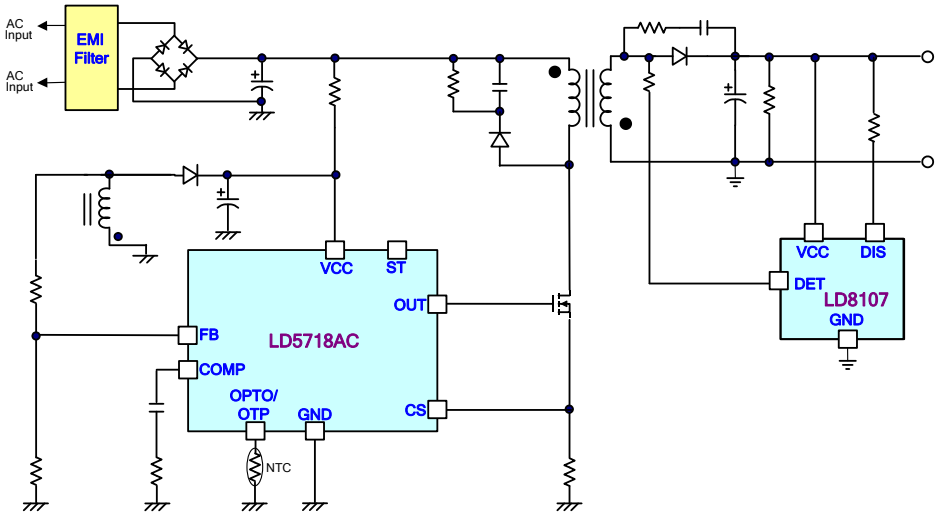
## Applications

- AC/DC Speedy Charger for Smart Phone and Tablet (5V-12V, 1A-2A)

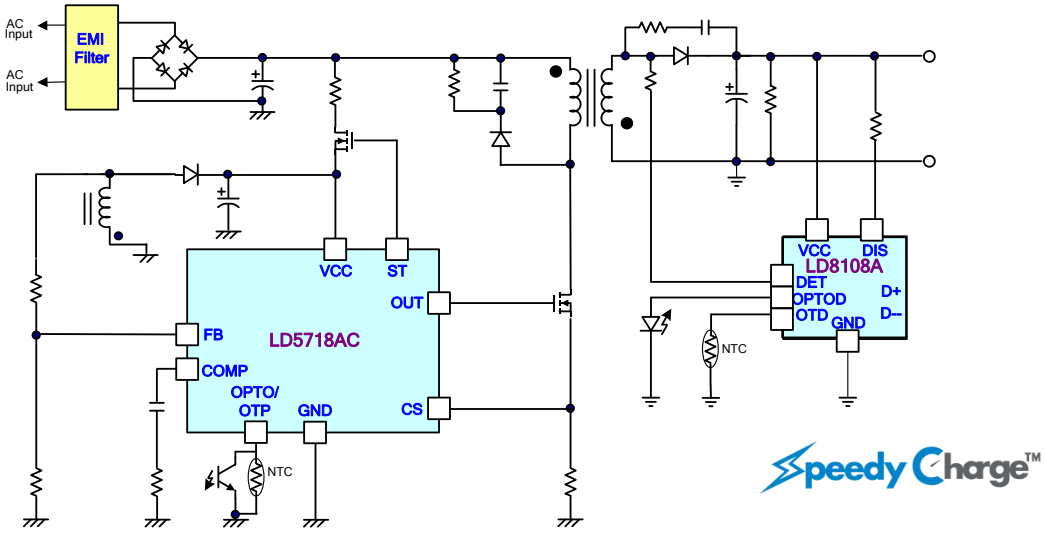
## Typical Application




Traditional LD5718AC PSR Charger and Adaptor Design



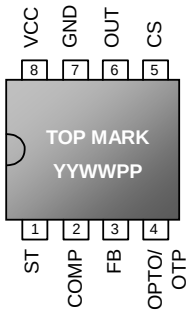

MediaTek Pump Express Plus™ Charger
LD5718AC Combined with LD8107 which is a Secondary-Side Discharging IC




Qualcomm® Quick Charge™ 2.0
LD5718AC Combined with LD8108A which is a Secondary-Side Controller

## Pin Configuration

SOP-8 (TOP VIEW)




YY: Year code (D:2004, E2005…)
WW: Week code
PP: Production code

## Ordering Information

| Part number | Max. output current limit ratio | | Min. Frequency | Max. Frequency | Package | Top Mark | Shipping |
|---|---|---|---|---|---|---|---|
| LD5718AC GS | 5V | x1 | 800Hz | 100kHz | SOP-8 | LD5718ACGS | 2500 /tape & reel |
| | 9V | x1 | | | | | |
| | 12V | x1 | | | | | |

The LD5718AC series are ROHS compliant/ Green Packaged.

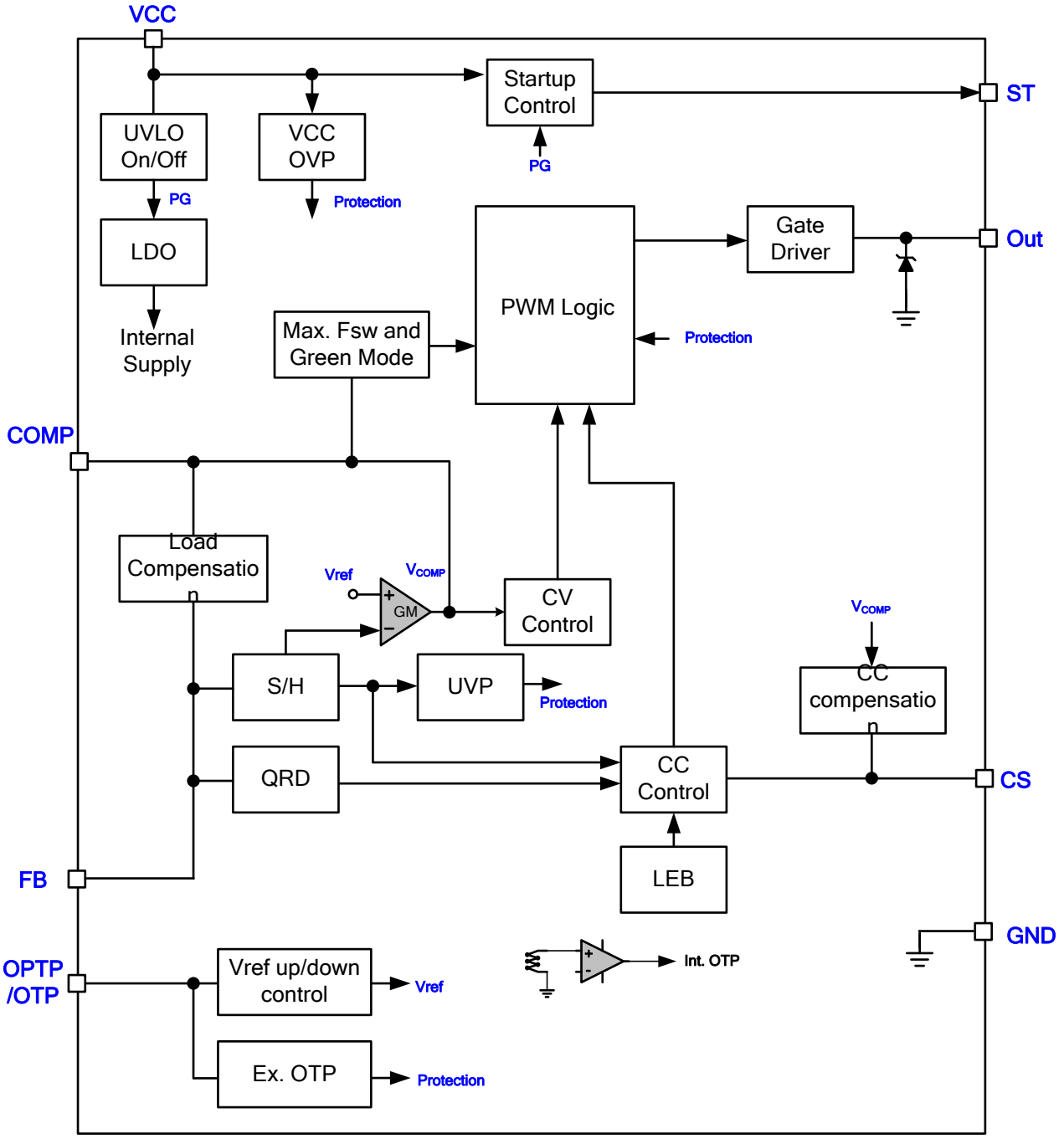
## Protection Mode

| Part number | VCC_OVP | UVP | OSCP | OTP |
|---|---|---|---|---|
| LD5718AC | Auto | Auto | Auto | Auto |

## Pin Descriptions

| Pin | NAME | FUNCTION |
|---|---|---|
| 1 | ST | HV startup driver |
| 2 | COMP | Output of the error amplifier for voltage compensation |
| 3 | FB | (1) Output Voltage Feedback, (2)QRD Detection |
| 4 | OPTO/OTP | (1) External OTP, (2)Output Regulation Setting Interface |
| 5 | CS | Current Sense Pin, connect to sense the MOSFET current |
| 6 | OUT | Gate Driver |
| 7 | GND | Ground |
| 8 | VCC | Supply voltage pin with OVP function |

## Block Diagram



## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage VCC, | -0.3V ~ 30V |
| ST, OUT | -0.3V ~ 30V |
| COMP, FB, OPTO/OTP, CS | -0.3V ~ 4.0V |
| FB (AC current ≤ 1mA) | -0.7V ~ 4.0V |
| Maximum Junction Temperature | 150°C |
| Storage Temperature Range | -65°C ~ 150°C |
| Package Thermal Resistance (SOP-8, $\theta_{JA}$) | 160°C/W |
| Power Dissipation (SOP-8, at Ambient Temperature = 85°C) | 250mW |
| Lead temperature (Soldering, 10sec) | 260°C |
| ESD Voltage Protection, Human Body Model | 2.5kV |
| ESD Voltage Protection, Machine Model | 250V |
| Gate Output Current | +120mA/-200mA |

**Caution:**

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

## Recommended Operating Conditions

| Item | Min. | Max. | Unit |
|---|---|---|---|
| Operating Junction Temperature | -40 | 125 | °C |
| VCC Capacitor | 2.2 | 22 | μF |
| COMP Pin Capacitor | 470 | 4700 | pF |

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF ~ 0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed to IC pin as possible.

## Electrical Characteristics

($T_A$ = +25°C unless otherwise stated, VCC=12.0V)

| PARAMETER | CONDITIONS | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Supply Voltage (VCC Pin)** | | | | | | |
| Startup Current | VCC=UVLO(ON) - 50mV | $I_{CC\_ST}$ | 0.05 | 1 | 2 | μA |
| Operating Current | $V_{COMP}$=0V, OUT=open, FB=2V | $I_{CC\_OP2}$ | 0.6 | 0.75 | 0.9 | mA |
| | OVP/FB UVP tripped, FB=0V | $I_{CC\_OPA}$ | 0.5 | 0.65 | 0.8 | mA |
| UVLO(OFF) | | $V_{CC\_OFF}$ | 5.5 | 6.0 | 6.5 | V |
| UVLO(ON) | | $V_{CC\_ON}$ | 14 | 15 | 16 | V |
| VCC OVP Level | | $V_{CC\_OVP}$ | 26.5 | 29 | 30 | V |
| **Error Amplifier (COMP Pin)** | | | | | | |
| Reference Voltage, $V_{REF}$ | For 5V output | $V_{REF\_5V}$ | 0.98 | 1.00 | 1.02 | V |
| | For 9V output | $V_{REF\_9V}$ | 1.65 | 1.73 | 1.8 | V |
| Load Compensation Current | $V_{COMP}$=2.5V | $I_{LOAD\_COMP}$ | 16 | 20 | 24 | μA |
| **Current Sensing (CS Pin)** | | | | | | |
| Maximum Input Voltage, $V_{CS-OFF}$ | | $V_{CS\_MAX}$ | 0.94 | 1 | 1.06 | V |
| Minimum $V_{CS-OFF}$ | $V_{COMP}$ < 0.45V | $V_{CS\_MIN}$ | 0.07 | 0.1 | 0.13 | V |
| Leading Edge Blanking Time | | $T_{LEB}$ | 300 | 450 | 600 | ns |
| **QRD (Quasi Resonant Detection, FB Pin)** | | | | | | |
| QRD Trip Level | * | $V_{QRD}$ | 70 | 100 | 130 | mV |
| | Hysteresis ,* | $V_{QRD\_HYS}$ | 30 | 50 | 70 | mV |
| **Oscillator for Switching Frequency** | | | | | | |
| Maximum Frequency | | $F_{SW\_MAX}$ | 92 | 100 | 108 | kHz |
| Minimum Frequency | | $F_{SW\_MIN}$ | 0.52 | 0.8 | 0.95 | kHz |
| **Output Drive (OUT Pin)** | | | | | | |
| Maximum On Time | | $T_{ON\_MAX}$ | 15 | 22 | 30 | μs |
| **FB Under Voltage Protection (UVP, FB Pin)** | | | | | | |
| Under Voltage Level for 5Vo | | $V_{FB\_UVP5VO}$ | 0.5 | 0.55 | 0.65 | V |
| UVP Delay Time | After soft start ,* | $T_{D\_FBUVP}$ | | 100 | | ms |
| **On Chip OTP (Over Temperature)** | | | | | | |
| OTP Level | * | $T_{INOTP}$ | 115 | 140 | 165 | °C |
| OTP Hysteresis | * | $T_{INOTP\_HYS}$ | 5 | 15 | 25 | °C |

| PARAMETER | CONDITIONS | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OPTO/OTP Pin** | | | | | | |
| OTP Pin Source Current | | $I_{OTP}$ | 90 | 100 | 110 | μA |
| Over Temperature Threshold | * | $V_{OTP}$ | 0.8 | 0.95 | 1.1 | V |
| Over Temperature Release Threshold | * | $V_{OTP\_R}$ | 0.9 | 1.05 | 1.2 | V |

*: Guaranteed by design.

## Typical Performance Characteristics

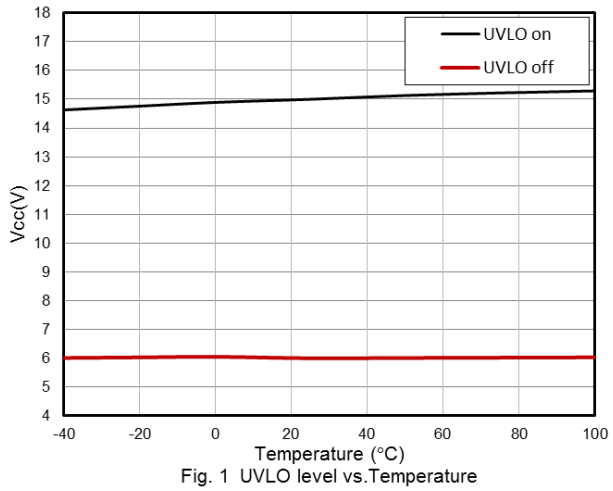



Fig. 1 UVLO level vs.Temperature

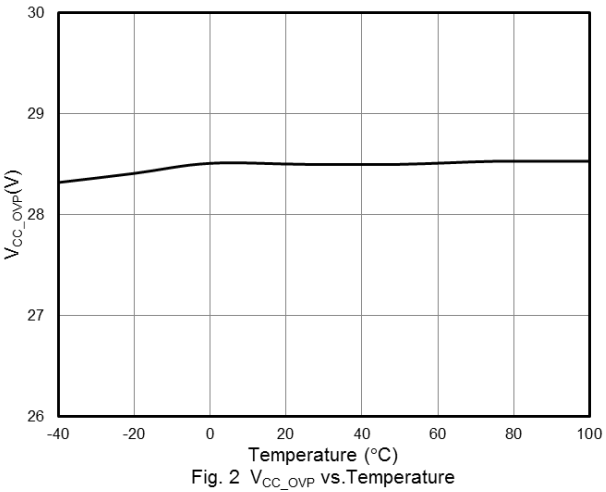



Fig. 2 $V_{CC\_OVP}$ vs.Temperature

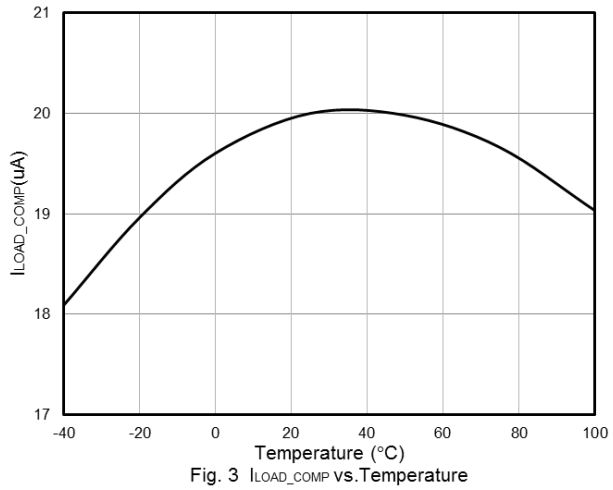



Fig. 3 $I_{LOAD\_COMP}$ vs.Temperature

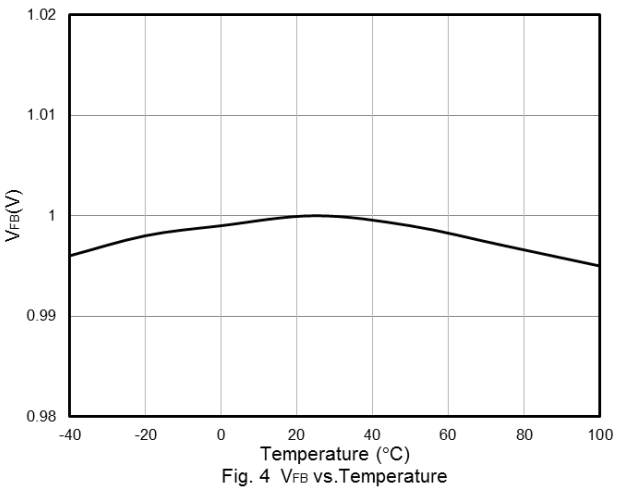



Fig. 4 $V_{FB}$ vs.Temperature

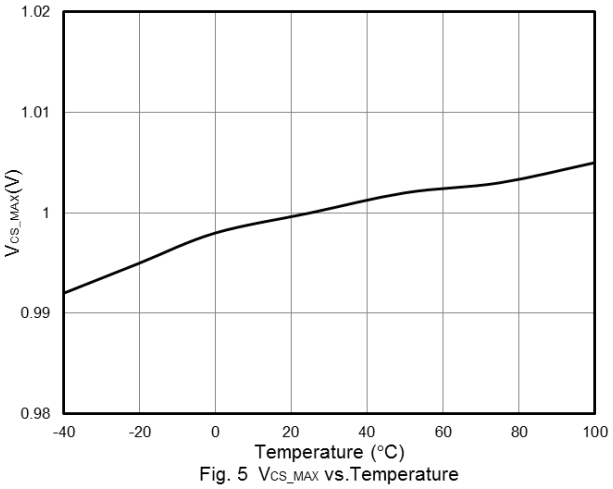



Fig. 5 $V_{CS\_MAX}$ vs.Temperature

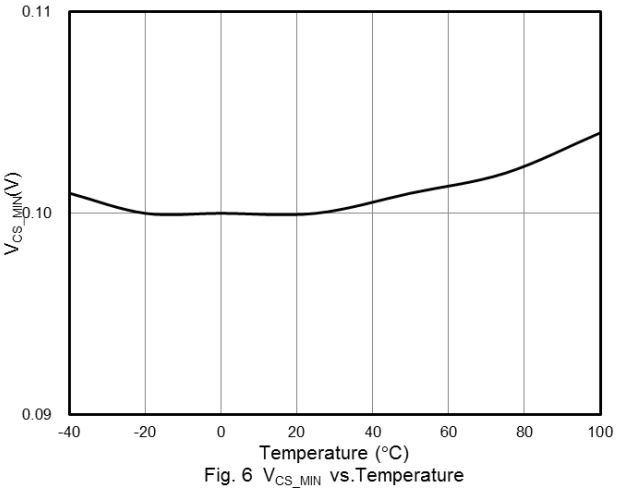



Fig. 6 $V_{CS\_MIN}$ vs.Temperature

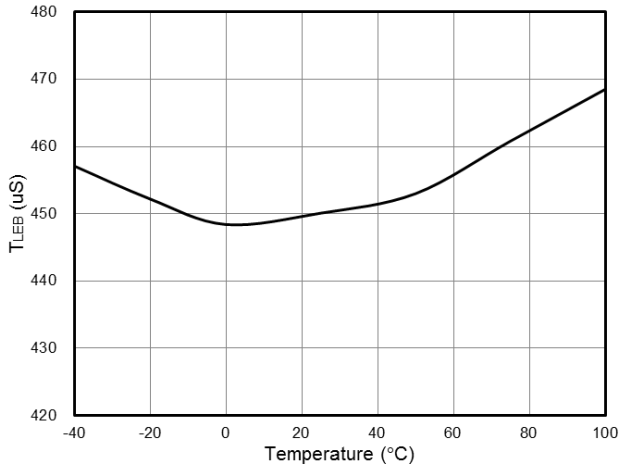



Fig. 7 $T_{LEB}$ Frequency vs.Temperature

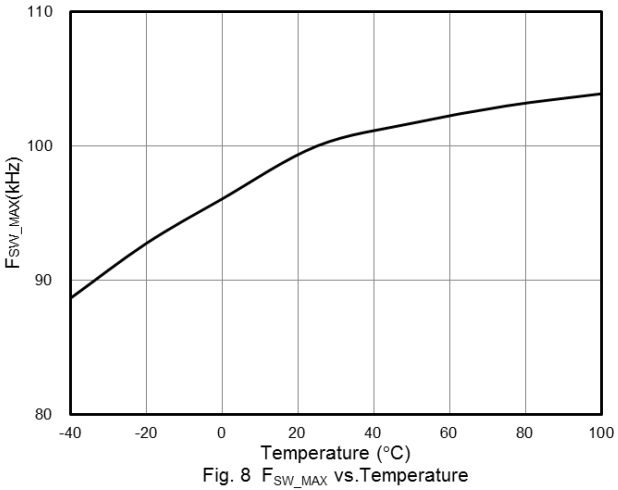



Fig. 8 $F_{SW\_MAX}$ vs.Temperature

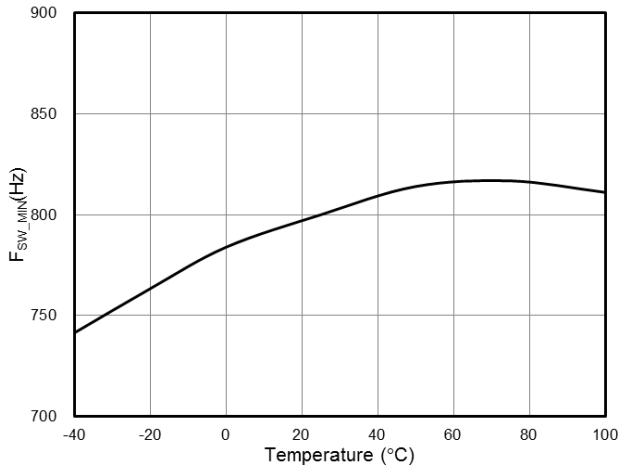



Fig. 9 $F_{SW\_MIN}$ vs.Temperature

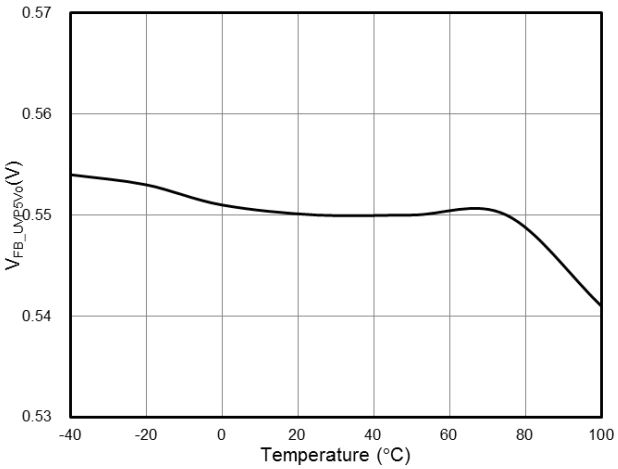



Fig. 10 $V_{FB\_UVP5Vo}$ vs.Temperature

# Application Information

## Operation Overview

The LD5718AC is an excellent primary side feedback controller with Quasi-Resonant operation to provide high efficiency and better EMI performance. The LD5718AC removes the need for secondary feedback circuits while achieving excellent line and load regulation. They meet the Green Power requirements and are intended for the use in those modern switching power suppliers and linear adaptors that demand higher power efficiency and power-saving. They integrate with more functions to reduce the external component counts and the size. Their major features are described as below.

## Under Voltage Lockout (UVLO)

An UVLO comparator is implemented to detect the voltage across VCC pin. It would assure the supply voltage high enough to turn on the LD5718AC PWM controller and further to drive the power MOS. As shown in Fig. 11, a hysteresis is built in to prevent shutdown from voltage drop during startup.

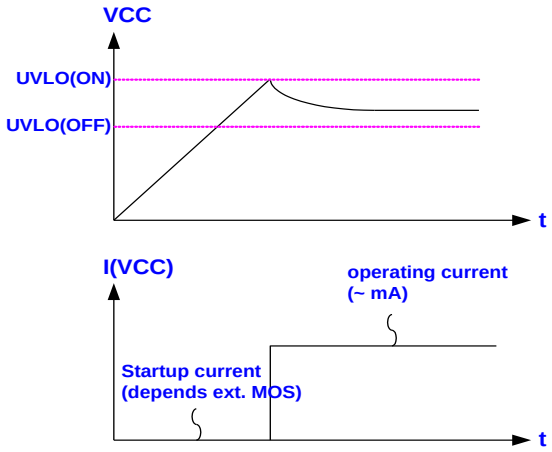



**Fig. 11**

## HV Startup Current and Circuit

The typical HV startup circuit generates VCC of the LD5718AC is shown in Fig. 12. During startup, the VCC sinks below the UVLO threshold, so there's no pulse delivering out from LD5718AC to drive the power MOS. Therefore, the current through R1 will be used to charge the capacitor C1. Until the VCC is fully charged to enable the LD5718AC and to deliver the drive-out signal, the auxiliary winding will provide the supply current instead. If PWM controller requires more current to start up, it can use external depletion NMOS, M1, which is controlled by ST pin and will provide ~mA to reduce the start-up time. For cost saving, user can skip the depletion MOS, M1, and let the ST pin be floating. By using CMOS process and some unique circuits design, the LD5718AC themself require only 1.5μA max to start up without using external depletion MOS. Higher resistance of R1 will spend much more time to start up. To save BOM cost, user is recommended to select proper value of R1 and C1 to optimize the power consumption and startup time.

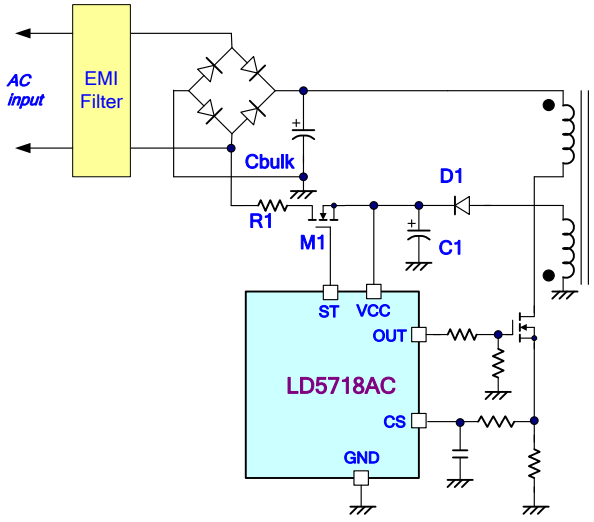



**Fig. 12**

## Principle of CV Operation

In the DCM Flyback converter, it senses the output voltage by auxiliary winding. LD5718AC samples the auxiliary winding on the primary-side to regulate the output voltage, as shown in the Fig. 13. The voltage induced in the auxiliary winding is a reflection of the secondary winding voltage while the power MOS is in off state. Via a resistor divider connected between the

auxiliary winding and FB pin, the auxiliary voltage is sampled after a sample delay time and will be hold until the next sampling. The sampled voltage is compared with internal reference $V_{REF}$ and the error will be amplified. The error amplifier output COMP reflects the load condition and controls the duty cycle to regulate the output voltage, thus constant output voltage can be achieved. The output voltage is given as:

$$V_{OUT} = 1.0V(1+\frac{Ra}{Rb})(\frac{Ns}{Na}) - V_F$$

where $V_F$ indicates the voltage drop of the output diode, Ra and Rb are top and bottom feedback resistor values, Ns and Na are the turns of transformer secondary and auxiliary windings.

In case that the output voltage is sensed through the auxiliary winding; the leakage inductance will induce ringing to affect output regulation. To optimize the collector voltage clamp circuit will minimize the high frequency ringing and achieve the best regulation. Fig. 14 shows the desired collector voltage waveform in compare to those with large undershoot due to leakage inductance induced ring (Fig. 15). This will make the sample error and cause poor performance for output voltage regulation. A proper selection for resistor RS, in series with the RC filter, may reduce any large undershoot.

LD5718AC supports Pump Express Plus™ fast charge agreement, the MCU can send current pattern to increase the charger output voltage, as shown in the Fig. 16. This method can achieve the effect of fast charging time.

LD5718AC supports Speedy Charge™, it can receive digital signal form secondary side controller (ex: LD8108A) to set output voltage to 5V, 9V, 12V, as shown in the Fig 16.

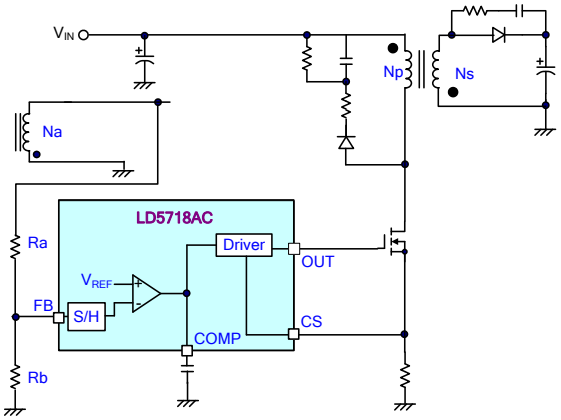



**Fig. 13**

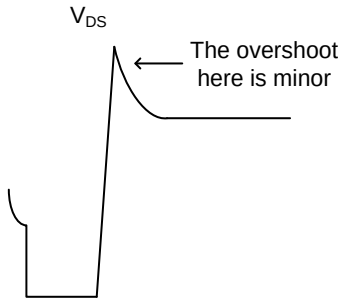



**Fig. 14**

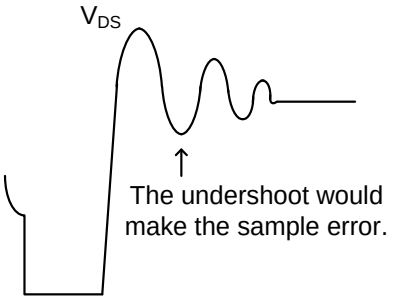



**Fig. 15**

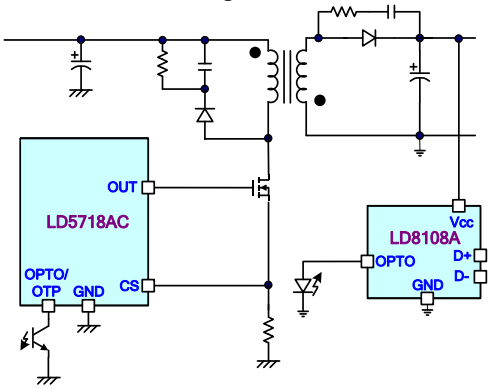



**Fig. 16**

## Load Regulation Compensation

LD5718AC implements load regulation compensation circuit to compensate the cable voltage droop and achieve a better voltage regulation. The offset voltage is created across FB pin by an internal sink current source which feeds out the FB pin during the sampling period. The internal sink current source is proportional to the value of $V_{COMP}$, as shown in Fig. 17. As a result, the drop due to the cable loss can be compensated. So that, the offset voltage decreases as the $V_{COMP}$ decreases in condition from full-load to no-load. It can also be programmed by adjusting the resistance of the divider to compensate the drop for various cable lines used. The equation of internal sink current source is shown as below.

$$I_{FB} = (V_{COMP} - 0.45) * 20 \ (\mu A)$$

The percentage of maximum compensation is shown as below.

$$\frac{\Delta V}{Vo} = \frac{I_{FB} \times (Ra // Rb)}{2} \times 100\%$$

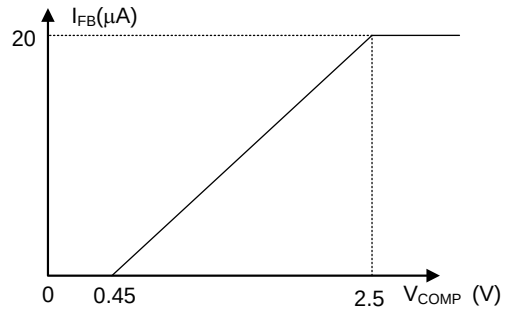



**Fig. 17**

## Quasi-Resonant Mode Detection

The LD5718AC employs quasi-resonant (QR) switching scheme to switch valley-mode either in CV or CC operation. This property feature greatly reduces the switching loss and dv/dt in the entire operating range for the power supply. The QR detection block will detect auxiliary winding signal to drive power MOS as FB pin voltage drops below 0.1V. The QR comparator would not operate if FB pin voltage remains above 0.3V. The 4ms of time-out-2 generates a power MOS turn-on signal as the driver output drops to low level for more than 4ms with the falling edge of the driver output.

## Multi-Mode Operation

The LD5718AC is a QR controller operating in multi-modes. The controller changes its operation modes according to line voltages and load conditions. At heavy-load ($V_{COMP}$>1.6V, Fig. 18), there might be two situations to meet. If the system AC input is in low line, the LD5718AC will turn on in first valley. If in high line, the switching frequency will increase till over the clamp of 100kHz and skips the first valley to turn on in 2nd valley. The switching frequency would vary depending on the line voltage and the load conditions when the system is operated in QR mode.

At medium or light load conditions, the frequency clamp is reduced to 25 kHz maximum as $V_{COMP}$ down to $V_{SG1}$. However, the valley switching characteristic behaves as well in these conditions. The LD5718AC will jump to turn on in 3rd, 4th…. Valley. That is, when load decreases, the system automatically skip more valleys and the switching frequency is thus reduced. In such way, a smooth frequency fold back is realized and high power efficiency is achieved.

At zero load or very light load conditions ($V_{COMP}$<0.3), the system operates in green mode for power saving. In green mode, the system modulates the frequency according to the load and $V_{COMP}$ conditions. Once $V_{COMP}$ is lower than $V_{SG2}$, the switching frequency starts to linearly decrease from 25 kHz to 800 Hz.

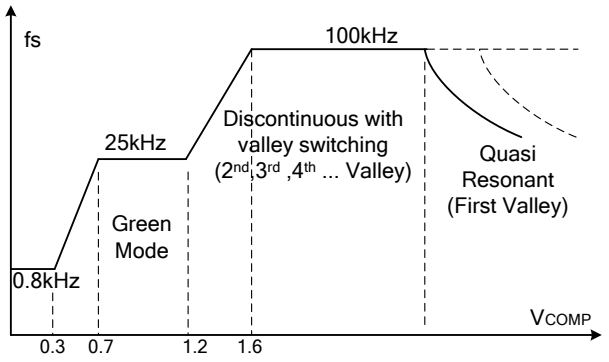



**Fig. 18**

## Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 19, the LD5718AC detects the primary power MOS current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 1V. From above, the power MOS peak current can be obtained as below.

$$I_{PEAK\,(MAX)} = \frac{1V}{R_S}$$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. LD5718AC can deliver more constant current at high input voltage than at low input voltage. To compensate this, an offset voltage is added to the RS signal by an internal current source ($I_{CC}$) and an external resistor ($R_1$) in series between the sense resistor (Rs) and the CS pin, By selecting a proper value of the resistor in series with the CS pin, the amount of compensation can be adjusted. The value of $I_{CC}$ (300 $\mu$A) depends on the COMP voltage($V_{COMP}$>0.9V). The equation of $I_{CC}$ (300 $\mu$A) is decreased as:

$$V_{CS} = V_S + (300\mu A \times R_1)$$

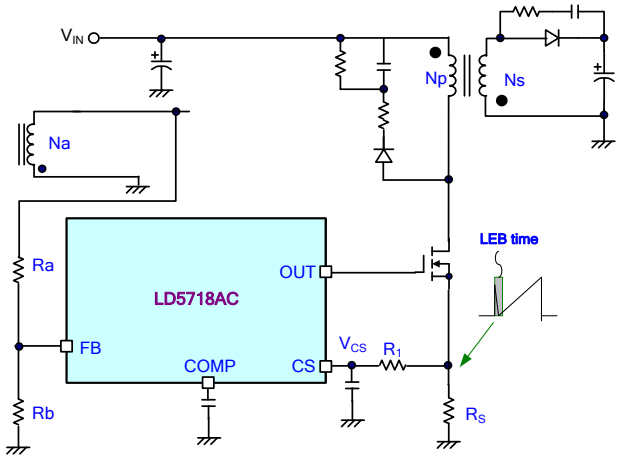



**Fig. 19**

## Principle of CC Operation

The primary side control scheme is applied to eliminate secondary feedback circuit or opto-coupler, which will reduce the system cost. The switching waveforms are shown in Fig. 20. The output current Io can be expressed as:

$$Io = \frac{1}{2}\frac{i_{S,PK} \times T_{DIS}}{T_S} = \frac{1}{2}\frac{N_P}{N_S} \times i_{P,PK} \times \frac{T_{DIS}}{Ts} = \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS}}{R_S} \times \frac{T_{DIS}}{T_S}$$

The primary peak current $i_{P,PK}$, inductor current discharge time ($T_{DIS}$) and switching period ($T_S$) can be detected by the IC. The ratio of $V_{CS}*T_{DIS}/T_S$ will be modulated as a constant (EX:$V_{CS}*T_{DIS}/T_S$ =1/2). $I_O$ can be induced finally by

$$Io \cong \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS}}{R_S} \times \frac{T_{DIS}}{T_S} \cong \frac{1}{2}\frac{N_P}{N_S} \times \frac{1}{R_S} \times \frac{1}{2}$$

However this is an approximate equation. The user may fine-tune it according to the experiment result.

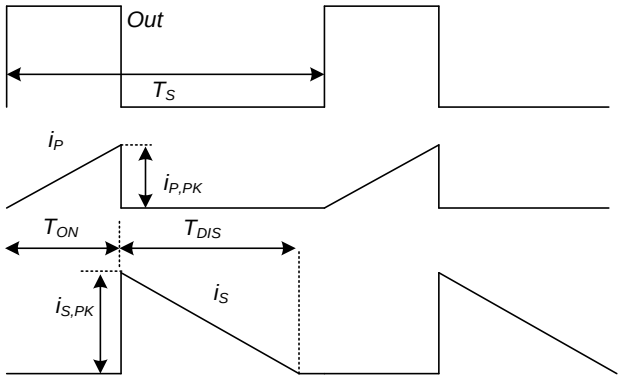



**Fig. 20**

## OVP (Over Voltage Protection) on VCC – Auto Recovery

LD5718AC implements OVP function over VCC pin. As the VCC voltage rises over the OVP threshold voltage, the output drive circuit will be shutdown simultaneously thus to stop the switching of the power MOS until the next UVLO(ON) arrives. The VCC OVP function of LD5718AC is an auto-recovery type protection. The Fig. 21 shows its operation. On the other hand, if the OVP condition is removed, the Vcc level will get back to normal level and the output will automatically return to the normal operation.

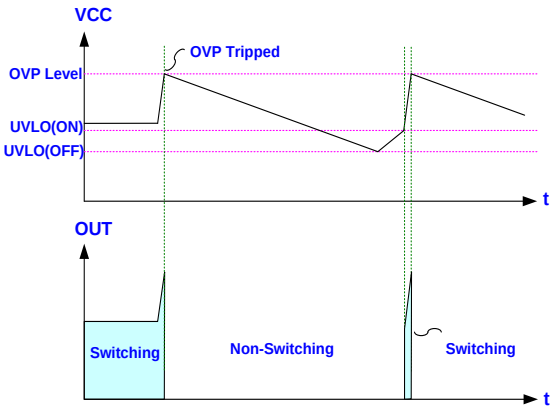



**Fig. 21**

## FB Under Voltage Protection (FB UVP) – Auto Recovery

LD5718AC implements the UVP function over FB pin. If the FB voltage falls below 0.55V for over the delay time of FB UVP, the protection will be activated to stop the switching of the power MOS until the next UVLO(ON) arrives. The FB UVP function in LD5718AC is an auto-recovery type protection. The Fig. 22 shows its operation. The FB UVP is disabled during the soft start. When LD5718AC is regulated to some other voltages, like 9Vo and 12Vo, the UVP level is set to 6.5V which complies with the Qualcomm QC2.0 recommended values while the 7Vo UVP is set to 5V.LD5718AC is also built-in the debounce time for hundred millisecond to avoid miss triggering.

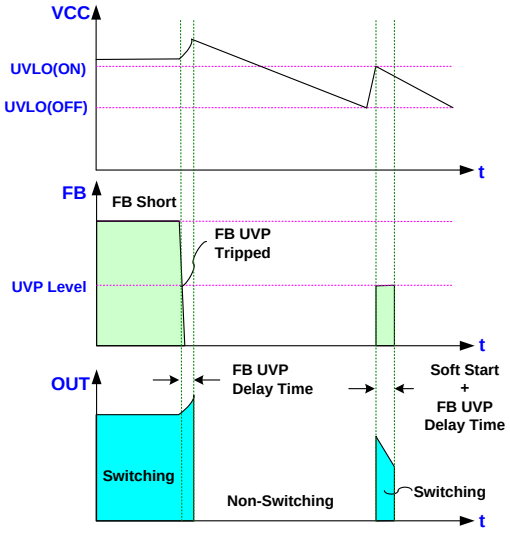
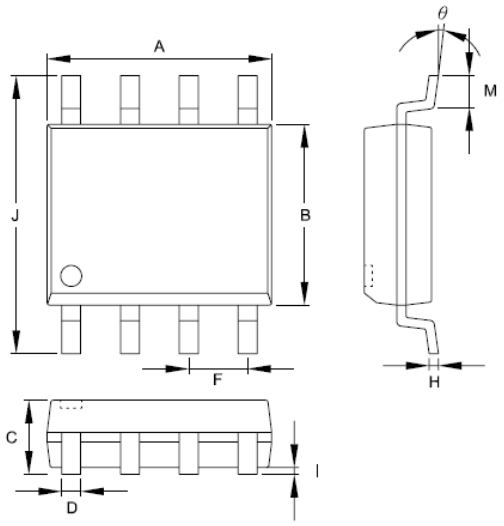



**Fig. 22**

# Package Information

**SOP-8**




| Symbols | Dimensions in Millimeters | | Dimensions in Inch | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.801 | 5.004 | 0.189 | 0.197 |
| B | 3.810 | 3.988 | 0.150 | 0.157 |
| C | 1.346 | 1.753 | 0.053 | 0.069 |
| D | 0.330 | 0.508 | 0.013 | 0.020 |
| F | 1.194 | 1.346 | 0.047 | 0.053 |
| H | 0.178 | 0.254 | 0.007 | 0.010 |
| I | 0.102 | 0.254 | 0.004 | 0.010 |
| J | 5.791 | 6.198 | 0.228 | 0.244 |
| M | 0.406 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

## Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

## Revision History

| REV. | Date | Change Notice |
|---|---|---|
| 00 | 09/22/2016 | Original Specification |