High Voltage Green-Mode PWM Controller Integrated with Brown-In/Out Function

REV: 03

General Description

The LD5760H is a Green Mode PWM IC built-in with brown-in function in a SOP-7 or SOP-8 package. It minimizes the component counts, circuit space, and reduces the overall material cost for the power applications.

The LD5760H features HV start, green-mode power-saving operation, and internal slope compensation, soft-start functions to minimize the power loss and enhance the system performance.

With complete protection in it, as OLP (Over Load Protection), OVP (Over Voltage Protection), fast SCP (short circuit protection) and brown-in protection, LD5760H prevents the circuit from being damaged under abnormal conditions.

Furthermore, the LD5760H features frequency swapping and soft driving function to reduce the noise and improve EMI.

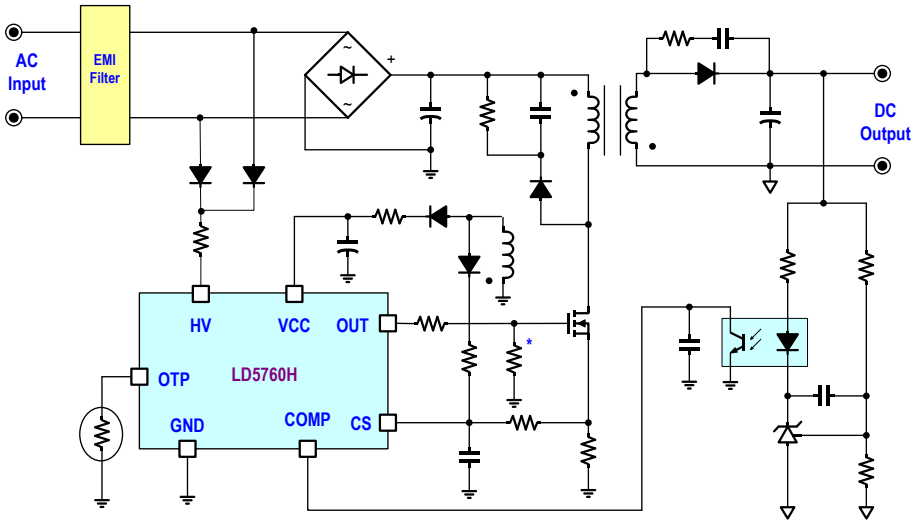
Features

- High-Voltage (650V) Startup Circuit
- Built-in Brown-in Function on HV pin
- Built-in X-Cap Discharge on HV pin
- Frequency Swapping for EMI improvement
- Non-Audible-Noise Green Mode Control
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Slope and OCP Compensation
- OVP (Over Voltage Protection) on VCC/CS
- OLP (Over Load Protection)
- OTP (Over Temperature Protection)
- SCP(Short Circuit Protection)
- Soft Start and Soft Driving
- +300mA/-800mA Driving Capability

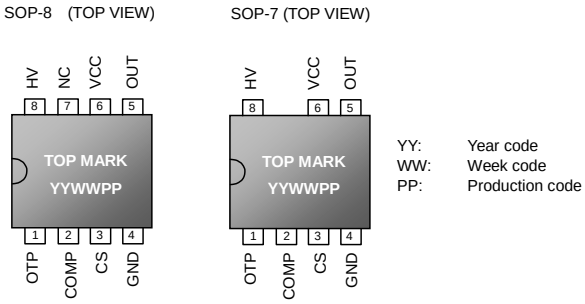
Applications

- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

Typical Application



Pin Configuration



Ordering Information

Part number	Package	Top Mark	Shipping
LD5760H GS	SOP-8	LD5760HGS	2500 /tape & reel
LD5760H GR	SOP-7	LD5760HGR	2500 /tape & reel

The LD5760H is RoHs compliant/ Green Packaged.

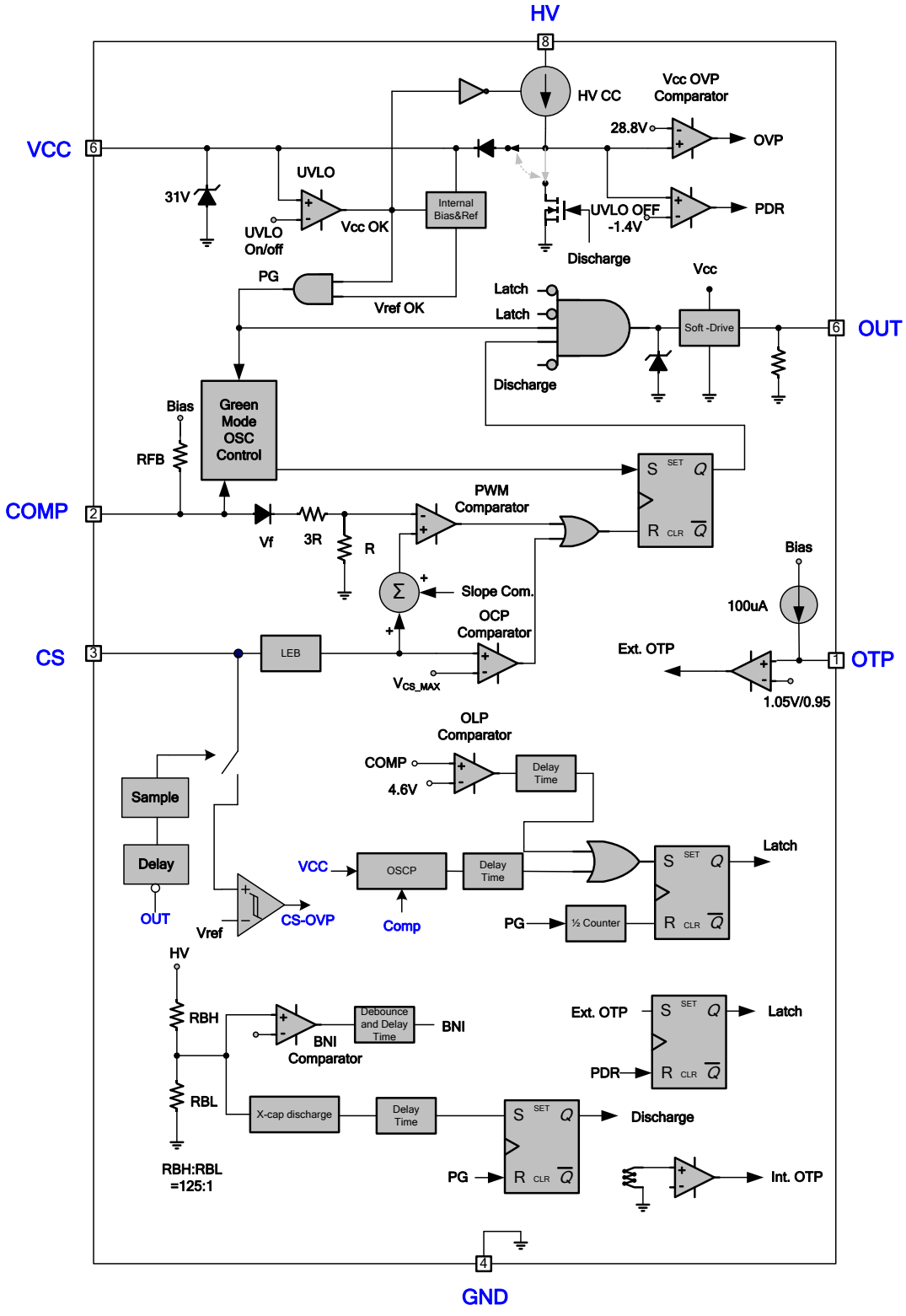
Protection Mode

Part number	VCC_OVP	OSCP	CS_OVP	OLP	OTP
LD5760H	Latch	Latch	Latch	Latch	Latch

Pin Descriptions

PIN	NAME	FUNCTION
1	OTP	Pulling this pin below 0.95V will force the controller enter into latch mode and it will not resume until the AC power recycles. Connect a NTC between this pin and ground to achieve OTP protection function. Let this pin float to disable the latch protection.
2	COMP	Voltage feedback pin. Connect a photo-coupler with it to close the control loop and achieve the regulation.
3	CS	Current sense pin, connect it to sense the MOSFET current
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Supply voltage pin
7	NC	Unconnected Pin
8	HV	Connect this pin to Line/ Neutral of AC main voltage through a resistor to provide the startup current for the controller. If VCC voltage increase to trip the point of UVLO(ON), this HV loop will be turned off to reduce the power loss on the startup circuit. An internal resistor divider between HV to GND pin will monitor AC line voltage to activate Brown-in/out function.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V ~ 31V
HV	-0.3V ~ 650V
COMP, OTP, CS	-0.3V ~ 6V
OUT	-0.3V ~ VCC+0.3V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOP-8/SOP-7, θ_{JA})	160°C/W
Power Dissipation (SOP-8/SOP-7, at Ambient Temperature = 85°C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV Pin)	2.5KV
ESD Voltage Protection, Machine Model (except HV Pin)	250V
ESD Voltage Protection, Human Body Model (HV Pin)	1KV
ESD Voltage Protection, Machine Model (HV pin)	200V
Gate Output Current	+300mA/-800mA

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.5	26.5	V
HV Resistor Value (AC Side)	8	12.5	KΩ
(HV to GND Resistor Value) ∗ (X-Capacitor Value)	0.5	--	Sec
HV to GND Resistor Value	--	12	MΩ
HV to GND Capacitor Value	--	300	pF
Comp Pin Capacitor	1	10	nF
CS Pin Capacitor Value	47	390	pF
OTP Pin Capacitor Value	NA	4.7	nF

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)						
High-Voltage Current Source	VCC< UVLO(ON), HV=500V	I_{HV}	2	2.8	3.6	mA
HV Discharge capability	HV=500V	I_{HV_DIS}	2	2.5	3	mA
HV Pin Total Input Current	HV=500 V_{DC}, VCC > UVLO(ON)	I_{HV_LEAK}			35	μA
HV Pin Brown-In Level		V_{HVBI}	85	95	105	V
HV Pin Brown-Out Level		V_{HVBO}	74	82	90	V
HV Pin BNO Hysteresis	V_{HVBI} - V_{HVBO}	ΔV_{HV}		15		V
Brown-in De-bounce Time		T_{D_HVBI}		170		μS
Brown-out Detection Delay time	V_{COMP}=3V	T_{D_HVBO}	110	138	165	mS
HV Pin Min. Operation Voltage	VCC=15V (DetVmin = VHV-VCC = 30V)	V_{HV_MIN}	45			V
X-Cap discharge Detection Delay time	V_{COMP}=3V	T_{D_XCAP}		132		mS
Supply Voltage (VCC Pin)						
Startup Current	VCC=15V ,HV=500V	I_{CC_ST}		25	50	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=3V	I_{CC_OP1}		1.5		mA
	V_{COMP}=0V	I_{CC_OP2}		0.3		mA
	Latch mode	I_{CC_OPL}		0.43		mA
UVLO(OFF)		VCC_{OFF}	6	7	8	V
UVLO(ON)		VCC_{ON}	15	16	17	V
PDR		VCC_{PDR}		$VCC_{\_OFF}$ -1.4V		V
VCC HVBI Level	HV>HVBI (Fig 1.)	VCC_{HVBI}		$VCC_{\_OFF}$ +3.8V		V
VCC OVP Level		VCC_{OVP}	27.8	28.8	29.8	V
VCC OVP De-bounce Time		T_{D_VCCOVP}		80		μS

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency						
Frequency		F_{SW}	60	65	70	kHz
Swapping Frequency		F_{SW_SWA}		±8		%
Green Mode Frequency		F_{SW_GREEN}	20.5	23.5	26	kHz
Modulation Frequency		F_{SW_MOD}		200		Hz
F_{SW} Temp. Stability	*, -40°C ~105°C	F_{SW_TS}	0	3	4	%
F_{SW} Voltage Stability	*	F_{SW_VS}	0		1	%
Maximum On Time		MXD	78	85	90	%
OSCP (Output Short Circuit Protection)						
OSCP Trip Level	*	VCC_{OSCP}		VCC_{-OFF} +2.4V		V
OSCP Delay Time	*, Exclude soft start time.	T_{D_OSCP}		10		ms
Voltage Feedback (Comp Pin)						
Input Voltage to Current-Sense Attenuation	*	A_V		1/4		V/V
Comp Impedance	V_{COMP}=3V	Z_{COMP}		42		kΩ
Open Loop Voltage		V_{COMP_OPEN}	4.9	5.2	5.5	V
OLP Tripped Level		V_{OLP}	4.4	4.6	4.8	V
PWM Mode Threshold VCOMP	F_{SW_SW} X 0.9 (Fig. 2)	V_P	2.6	2.8	3.0	V
Green Mode Threshold VCOMP	F_{SW_GREEN} X1.1 (Fig. 2)	V_G	2.2	2.5	2.7	V
Zero Duty Threshold	Zero Duty	V_{ZDC}		1.9		V
VCOMP on Burst mode	Hysteresis	V_{ZDCH}		100		mV
Current Sensing (CS Pin)						
Maximum Input Voltage		V_{CS_MAX}	0.675	0.71	0.745	V
Leading Edge Blanking Time		T_{LEB}		300		nS
Delay to Output		T_{PD}		70		nS
Slope Compensation Level	*, 0%-85% Linearly	V_{SLP_L}	0		0.2	V
Slope Compensation Position	*0%-85% Linearly	VSLP	0		85	%

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
OVP CS Pin						
OVP Trip Current Level	DC	$V_{CSOVP-1}$	0.18	0.2	0.22	V
	AC(High to Low)	$V_{CSOVP-2}$	0.165	0.182	0.201	V
De-bounce Cycle		T_{D_CSOVP}		160		μS
Sample Delay Time	*	T_{S_CSOVP}		1.5		μS
Gate Drive Output (OUT Pin)						
Output Low Level	VCC=15V, Io=20mA	V_{OL}	0	-	1	V
Output High Level	VCC=15V, Io=20mA	V_{OH}	8	-	VCC	V
Rising Time	Load Capacitance= 1000pF @ from OUT>4V	T_r	-	50		nS
Falling Time	Load Capacitance= 1000pF	T_f	-	20		nS
OUT Pin Clamping Voltage	VCC= 21V,1nF on OUT pin	V_{O_CLAMP}		12		V
Source capability	*Load Capacitance= 33nF@out=4V	I_{SOURCE}		300		mA
Sink capability	*Load Capacitance=33nF	I_{SINK}		800		mA
OLP (Over Load Protection)						
OLP Delay Time		T_{D_OLP}	100	120	150	mS
Soft Start						
Soft Start Duration	*soon as OLP, OTP, BNO, OVP is tripped	T_{SS}		6		mS
Internal OTP						
OTP Tripped Level	*	T_{INOTP}		150		°C
OTP Hysteresis	*	T_{INOTP_HYS}		30		°C
OTP De-bounce Time	*	T_{D_INOTP}		160		μS
Over Temperature Protection(OTP Pin)						
OTP Pin Source Current		I_{OTP}	92	100	108	μA
Turn-On Trip Level		V_{OTP_ON}	1.00	1.05	1.10	V
Turn-Off Trip Level		V_{OTP_OFF}	0.9	0.95	1.0	V
OTP pin de-bounce time	V_{COMP}=3V	T_{D_OTP}		300		μs
OTP Pin Open Voltage	R_{OTP}=100kΩ	V_{OTP_OPEN}	3		5.5	V

*: Guaranteed by design

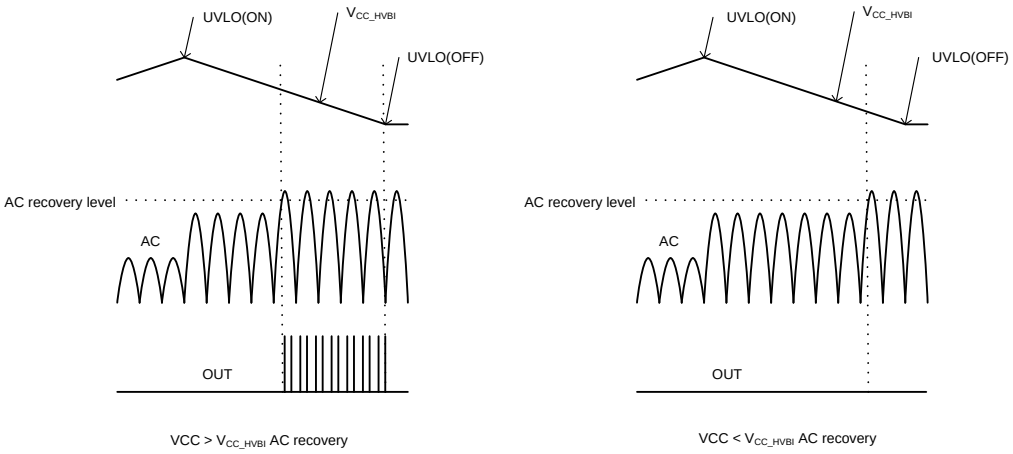


Fig. 1 VCC_{-HVBI} & AC recovery

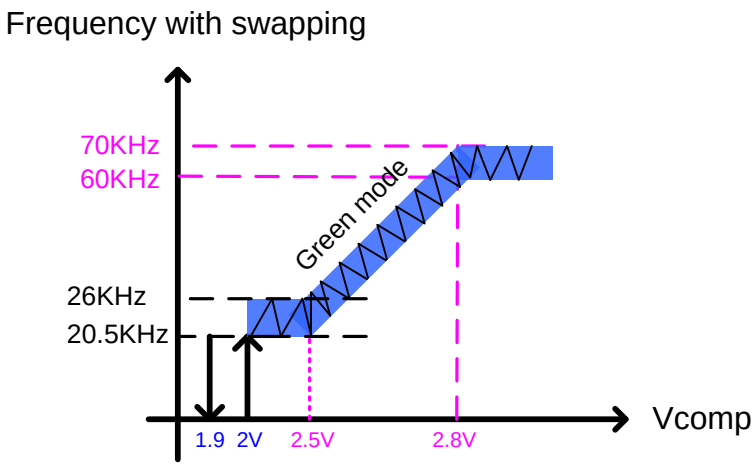


Fig. 2 V_{COMP} vs. Frequency with swapping

Typical Performance Characteristics

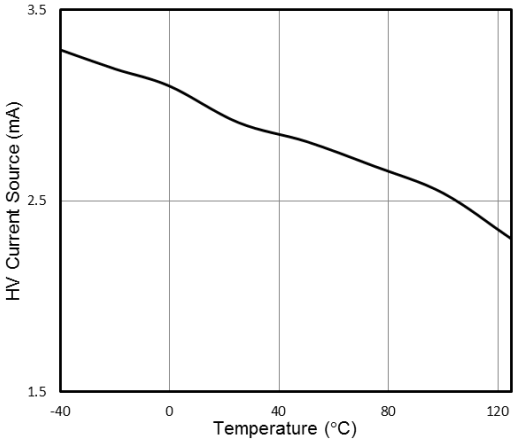


Fig.3 IHV vs. Temperature (HV=500V, Vcc=15V)

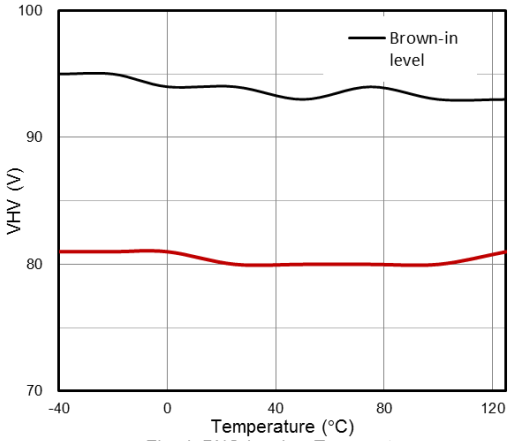


Fig. 4 BNO level vs.Temperature

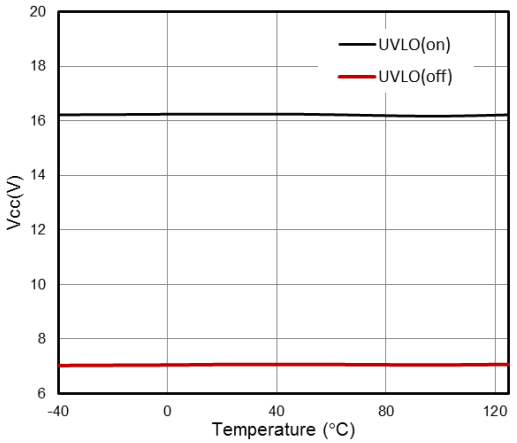


Fig. 5 UVLO level vs.Temperature

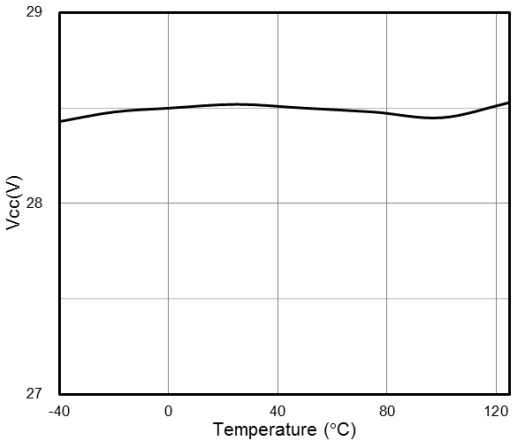


Fig. 6 Vcc OVP Level vs.Temperature

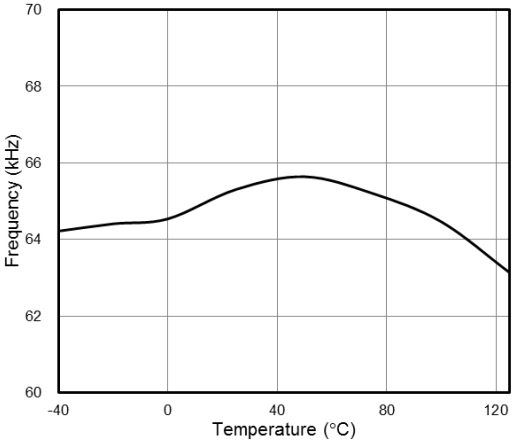


Fig. 7 Frequency vs.Temperature

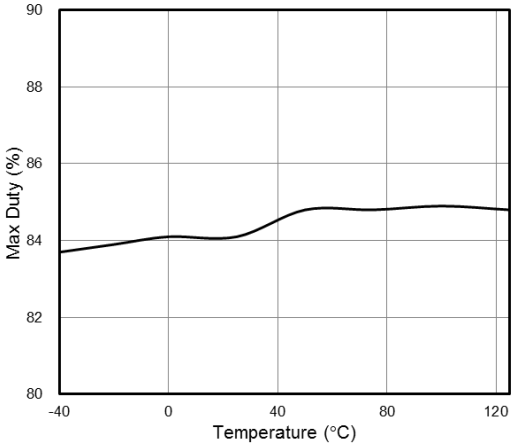


Fig. 8 Max Duty vs.Temperature

Typical Performance Characteristics

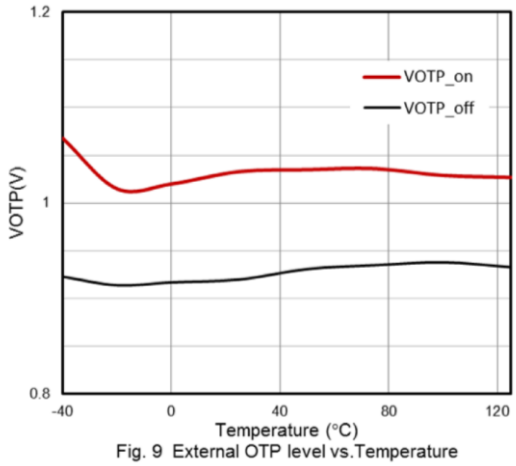


Fig. 9 External OTP level vs.Temperature

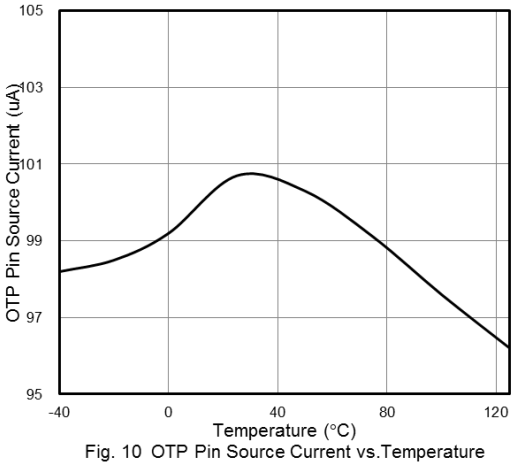


Fig. 10 OTP Pin Source Current vs.Temperature

Application Information

Operation Overview

As long as the requirement for green power becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Due to the cost and size limit, the PWM controller designer is bound to integrate with more functions to reduce the external part counts. The LD5760H is ideal for these applications. Its detailed features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes much significant power to meet the current power saving requirement. In most cases, startup resistors carry larger resistance and spend more time to start up.

To achieve the optimized topology, as shown in Fig. 11, LD5760H is implemented with a high-voltage startup circuit for such requirement. At startup, the high-voltage current source sinks current of AC Line/or Neutral to provide startup current and charge the capacitor C1 connected to VCC.

At the startup transient, the HV current will supply around 2.8mA to VCC capacitor until this VCC voltage reaches the UVLO threshold VCC. By using such configuration, the turn-on delay time will be almost same no matter under low-line or high-line conditions.

Once the LD5760H protection is triggered, IC will keep in latch mode until VCC is lower than PDR level. In latch mode, VCC capacitor is charged and discharged between UVLO(on) and UVLO(off).To prevent the result that BNO is triggered and IC restarts from happening, the start-up resistor of HV-pin should follow the calculation shown as below:

$$\text{HV pin voltage}: 90\sqrt{2} - 3.6mA \times R_{HV} > 82V$$

Hence, it is suggested that the value of start-up resistor should be lower than 12.5 kohm

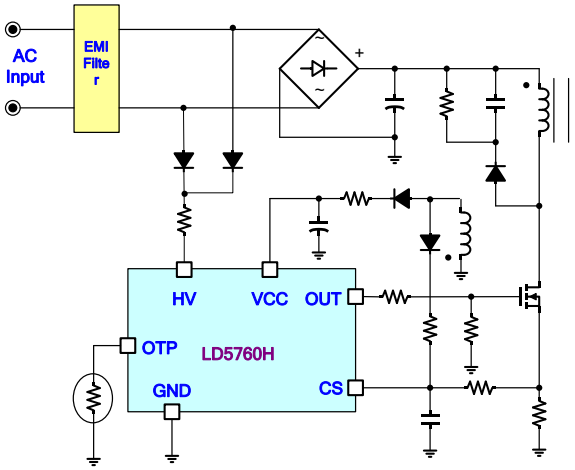


Fig. 11

As VCC trips UVLO(OFF), HV pin will recharge VCC capacitor till VCC voltage rises back to UVLO(ON) again. Since then, HV pin would no longer charge the capacitor and instead, send a gate drive signal to draw supply current for VCC from the auxiliary winding of the transformer. That minimizes the power loss on the start-up circuit successfully.

An UVLO comparator is embedded to detect the voltage across the VCC pin to ensure the supply voltage enough to power on the LD5760H and in addition, to drive the power MOSFET. As shown in Fig. 12, a hysteresis is provided to prevent shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16V and 7V, respectively.

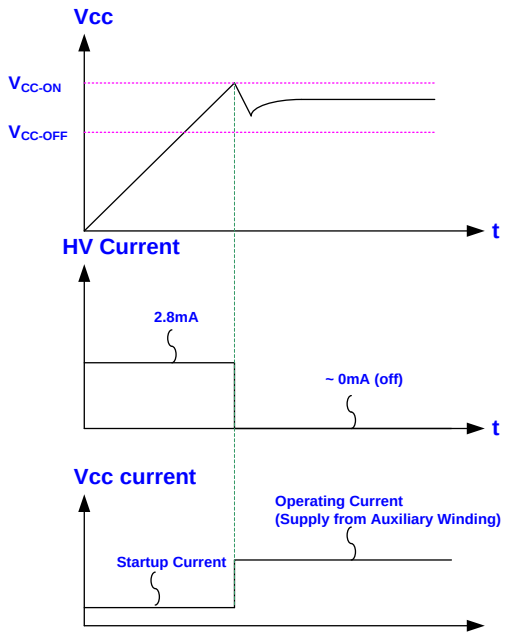


Fig. 12

Brown in Protection

The LD5760H features Burn-in function on HV pin. As the built-in comparator detects the half wave rectify line voltage condition, it will shut off the controller to prevent from any damage. Fig. 13 shows the operation.

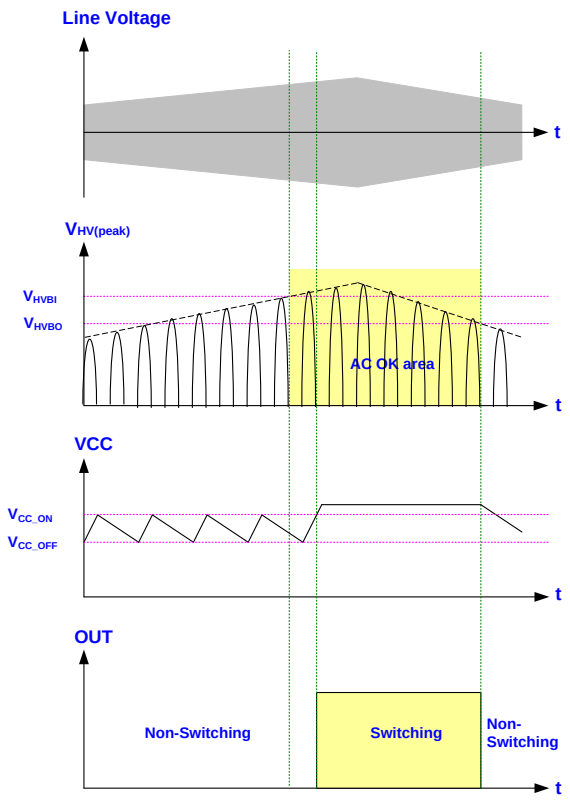


Fig. 13

Current Sensing, Leading-Edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD5760H detects the primary MOSFET current across CS pin to control in peak current mode and also limit the pulse-by-pulse current. The maximum voltage threshold of the current sensing pin is set at 0.7V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.7V}{R_S}$$

A 300nS leading-edge blanking (LEB) time is designed in the input of CS pin to prevent false-triggering from the current spike. In the low power applications, if the total pulse width of the turn-on spikes is less than 300nS and the negative spike on the CS pin does not exceed -0.3V, the R-C filter (as shown in Fig. 14) is free to eliminate.

However, the total pulse width of the turn-on spike is related to the output power, circuit design and PCB layout. It is strongly recommended to add a small R-C filter (as shown in Fig. 15) for larger power application to avoid the CS pin from being damaged by the negative turn-on spike.

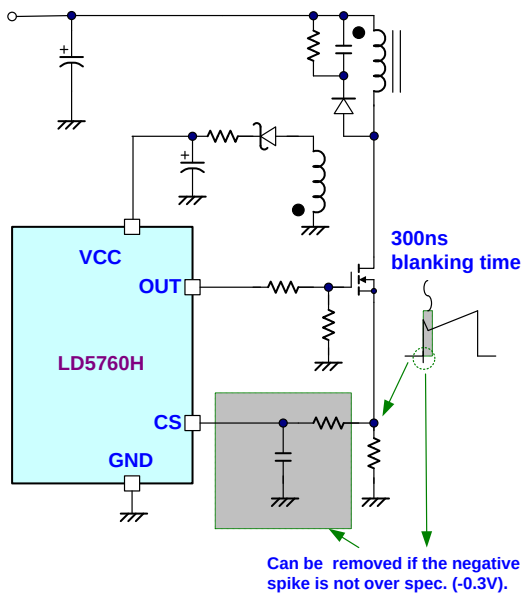


Fig. 14

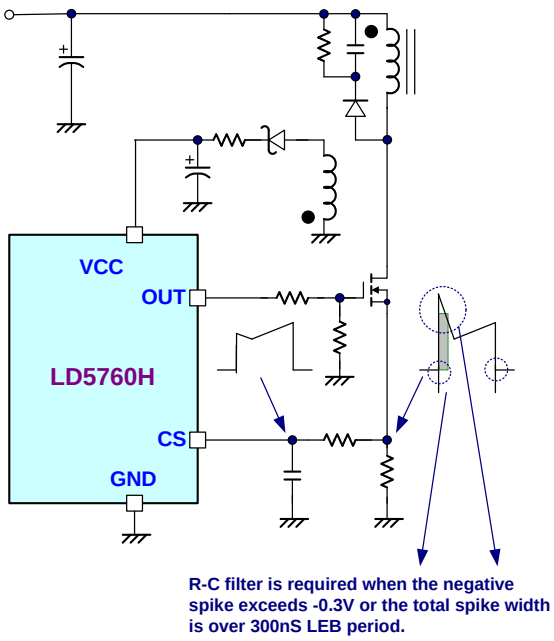


Fig. 15

Output Stage and Maximum Duty-Cycle

A CMOS buffer with output stage of typical 300mA driving capability is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD5760H is limited to 85% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 on the secondary side through the photo-coupler to the COMP pin of LD5760H. Similar to UC384X, its input stage is with a diode voltage offset to feed the voltage divider with 1/4 ratio, that is,

$$V_{CS(PWM\ COMPARATOR)} = \frac{1}{4} \times (V_{COMP} - V_F)$$

A pull-high resistor is embedded internally to optimize the external circuit.

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is operated for more than 50%. To stabilize the control loop, the slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. LD5760H has internal slope compensation circuit to simplify the external circuit design.

Oscillator and Switching Frequency

The LD5760H fixes the switching frequency at 65kHz internally to optimize its performance in EMI, thermal treatment, component sizes and transformer design.

Dual-Oscillator Green-Mode Operation

There are many different topologies has been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intended to reduce the switching cycles under light-load or no-load condition either by skipping

some switching pulses or reduce the switching frequency.

By using LD proprietary dual-oscillator technique, the green-mode frequency can be well controlled and further to avoid the generation of audible noise.

Frequency Swapping

The LD5760H is built in with frequency swapping function, which makes it easy for the power supply designers to optimize EMI performance and system cost. The frequency swapping is internally set for ±8%.

On/Off Control

Pulling COMP pin below VFB_B will immediately disable the gate output of LD5760H. Remove the pull-low signal to reset it.

Over Load Protection (OLP)- Latch Mode

To protect the circuit from being damaged during over load condition and short or open loop condition, the LD5760H is implemented with smart OLP function. LD5760H features latch mode function of it, see Fig. 16 for the waveform. In the example of the fault condition, the feedback system will force the voltage loop enter toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the V_{COMP} ramps up to the OLP tripped level (4.6V) and stays for more than the OLP delay time, the protection will be activate and then turn off the gate output to stop the switching of power circuit. The OLP delay time is set by internal high frequency counter. It is to prevent the false triggering from the power-on and turn-off transient.

Turn off AC power to let VCC fall below PDR level to release overvoltage protection. And then restart the power to resume the operation. The de-latch level is defined by internal PDR. See Fig. 16 for its operation.

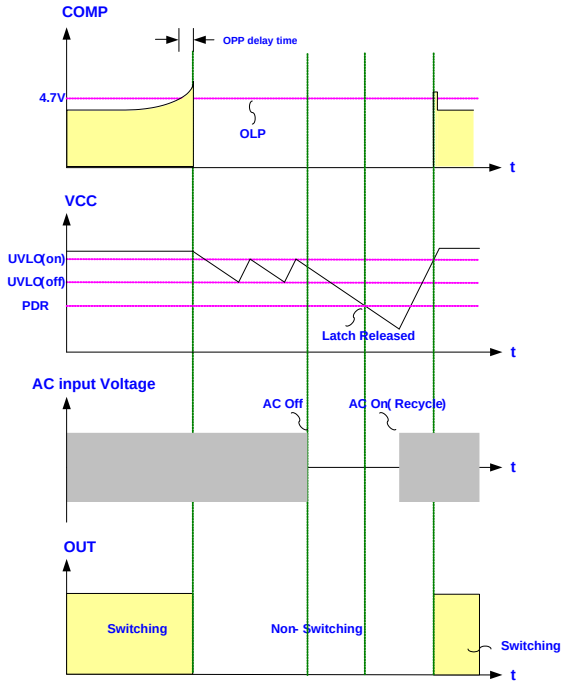


Fig. 16

OVP (Over Voltage Protection) on VCC – Latch Mode

The V_{GS} ratings of the nowadays power MOSFETs are mostly with 30V maximum. To protect the V_{GS} from the fault condition, LD5760H is implemented with OVP function on VCC. As the VCC voltage is larger than the OVP threshold voltage, the output gate drive circuit will be shut off simultaneously and stop switching the power MOSFET.

The VCC OVP is latch-off type of protection. Once the VCC trips OVP level (which is usually caused by the feedback loop opened), it will be latched off. Turn off AC power to let VCC fall below PDR level to release overvoltage protection. And then restart the power to resume the operation. The de-latch level is defined by internal PDR. See Fig. 17 for its operation.

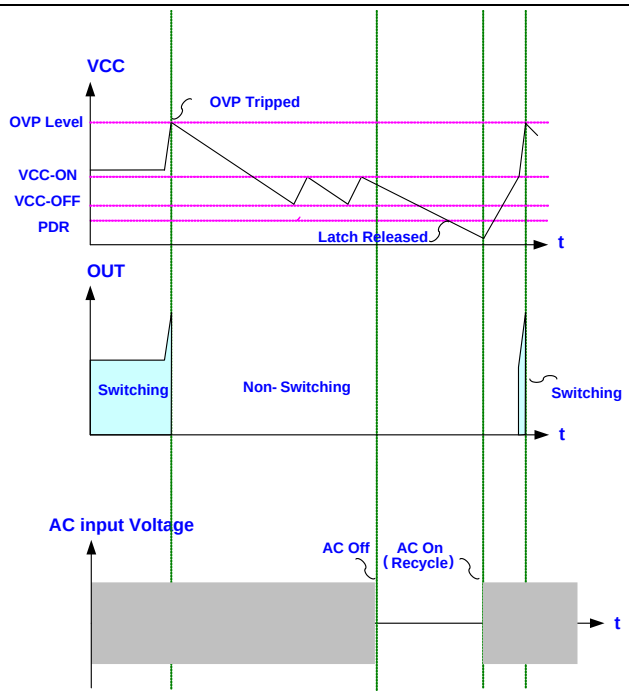


Fig. 17

On-Chip OTP - Auto Recovery

An internal OTP circuit is embedded inside the LD5760H to provide the worst-case protection for this controller. When the chip temperature rises higher than the trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window.

External OTP - Latched Mode Protection

The OTP circuit is implemented to sense whether there is any hot-spot of power circuit like power MOSFET or output rectifier. Typically, an NTC is recommended to connect with OTP pin. The NTC resistance will decrease as the device or ambient is in high temperature. The relationship is described as below.

$$V_{OTP} = 100\mu A \cdot R_{NTC}$$

When VOTP<V_{OTP-ON} (typical 0.95V), it will trigger the protection to shut down the gate output and latch off the power supply. The controller will remain latched unless the VCC drops below 7V (power down reset) and VCC stays on UVLO condition. Two conditions are required to restart the IC successfully, to cool down the circuit so that the NTC resistance will increase and to raise VOTP above 1.05V. Then, recycle the AC main power. The detailed operation is show in Fig. 18. Example: If resistor value of OTP pin is higher impedance or open, the OTP pin voltage is typically around 3.6V.

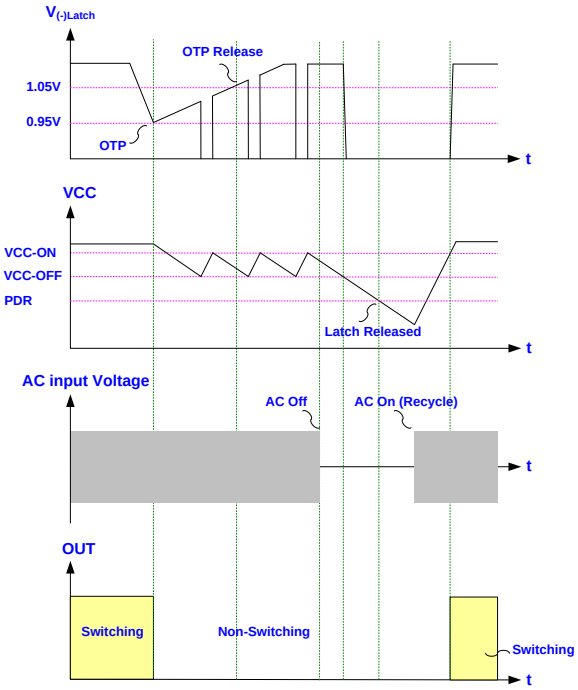


Fig. 18

Pull-Low Resistor on the Gate Pin of MOSFET

The LD5760H consists of an anti-floating resistor with OUT pin to protect the output from damage in abnormally operation or condition due to false triggering of MOSFET. Even so, we still recommend adding an external one at the MOSFET gate terminal to provide more protection in case of disconnection of gate resistor R_G during power-on.

In such single-fault condition, as shown in Fig. 19, the resistor R8 can provide a discharge path to avoid the MOSFET from being false-triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the MOSFET should be always pulled low and placed in the off-state as the gate resistor is disconnected or opened in any case.

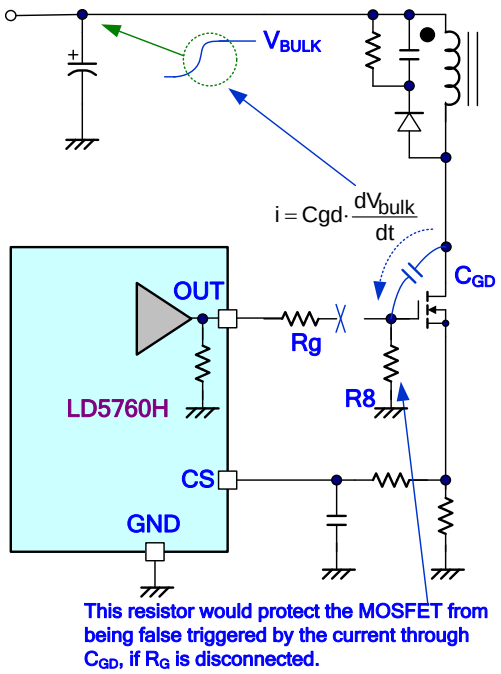


Fig. 19

Protection Resistor on the Hi-V Path

In some other Hi-V process and design, there may be a parasitic SCR caused around HV pin, VCC and GND. As shown in Fig. 20, a small negative spike on the HV pin may trigger this parasitic SCR and cause latch-up between VCC and GND. It may damage the chip because of the equivalent short-circuit induced by such latch-up behavior.

Leadtrend's proprietary of Hi-V technology will eliminate parasitic SCR in LD5760H. Fig. 21 shows the equivalent Hi-V structure circuit of LD5760H. So that LD5760H is more capable to sustain negative voltage than similar products. However, a 10KΩ resistor is recommended to add in the Hi-V path to play as a current limit resistor as a negative voltage is applied.

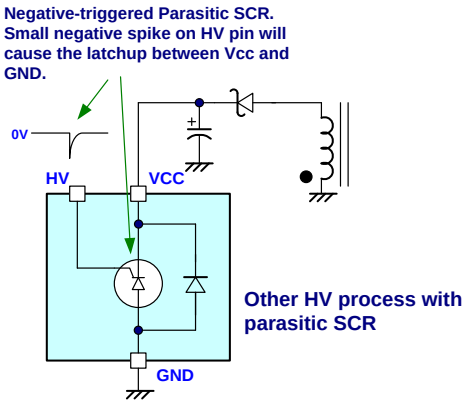


Fig. 20

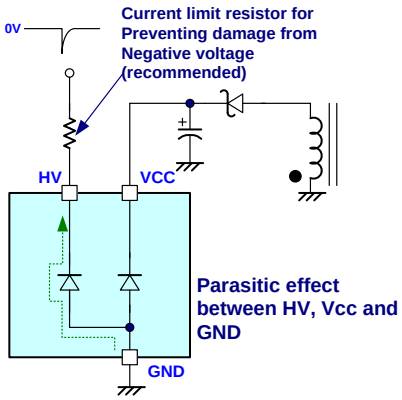


Fig. 21

Output Over Voltage Protection (CS Pin) - Latch Mode

An output overvoltage protection is implemented in the LD5760H, as shown in Fig. 22 and 23. The auxiliary winding voltage is reflected to secondary winding and therefore the flat voltage on the CS pin is proportional to the output voltage. By sensing the auxiliary voltage via the divided resistors, LD5760H can sample this flat voltage level after some delay time to perform output over-voltage protection. This delay time is used to ignore the voltage ringing from leakage inductance of PWM transformer. The sampling voltage level is compared with internal threshold voltage 0.2V. If the sampling voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP events. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. However, if typically 10 cycles of subsequent

OVP events are detected, the OVP circuit switches the power MOSFET off. Besides, the choices between D1 and C1 particularly need to be noticed. When power MOSFET gate turns off, the speed of CS pin voltage decreasing affect the OVP protection as shown in Fig. 23. The red line shows the situation that CS discharge too slow to steady state, it will cause mistrigger of OVP protection. The recommended range of C1 is 47~390pF, D1 trr≤50nS(EX: BAV21W, BAV103…).

As the protection is latched, the converter restarts only after the internal latch is reset. Thus the output over voltage can be calculated as:

$$(V_{AUX} - V_F)\frac{R1}{R1+R2} \geq 0.2V$$

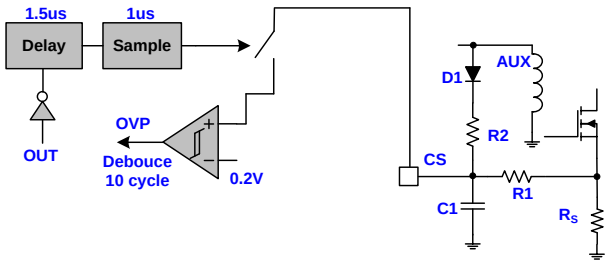


Fig. 22

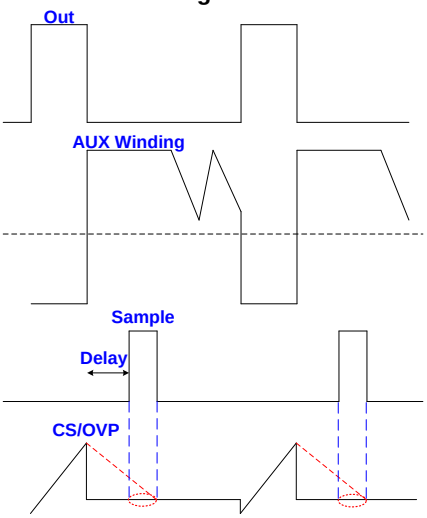
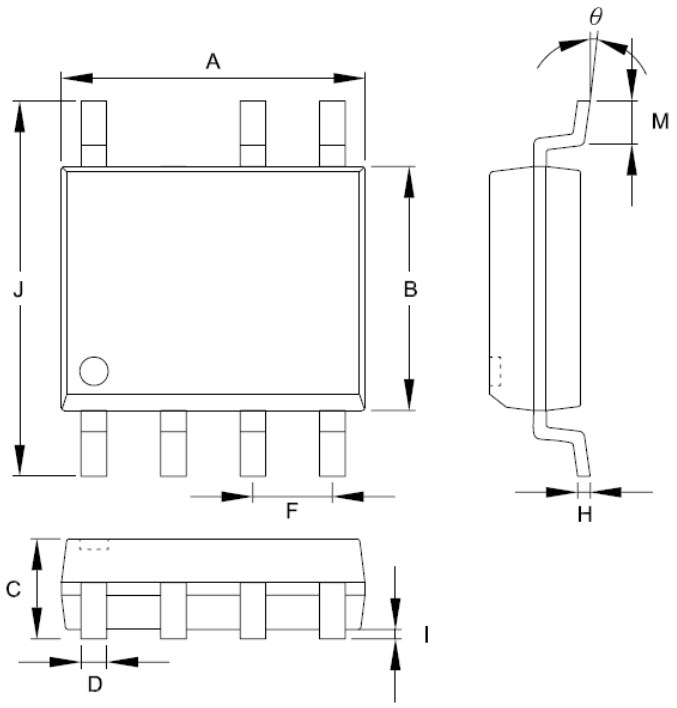


Fig. 23

Package Information

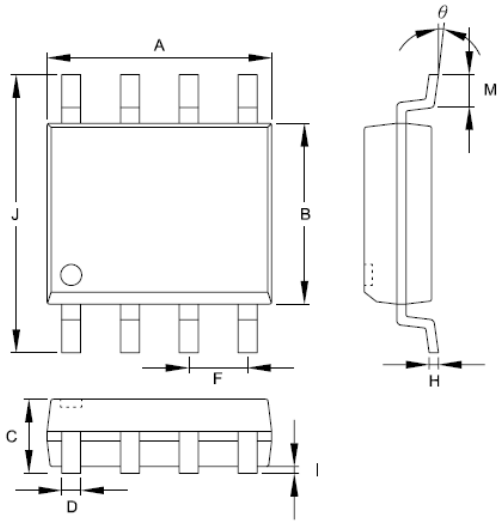
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	06/09/2015	Original Specification.
01	10/05/2015	Modify description about “Internal High-Voltage Startup Circuit and Under Voltage Lockout”, Modify $V_{CSOVP-2}$
02	03/17/2016	Add Recommended Operating Condition: C_{HV} to GND
03	12/15/2016	Add CS_OVP description