High Voltage PWM Controller with BNO Function

REV. 01

General Description

The LD5760T is a PWM IC with built-in brown-in/out functions in a SOP-7/SOP-8 package which can minimize the component counts, circuit space, and reduce the overall material cost of power applications.

The LD5760T provides HV start, internal slope compensation and soft-start functions which can minimum the power loss and improve the system performance.

With the complete protection modes, like OLP (Over Load Protection), OVP (Over Voltage Protection), fast SCP(short circuit protection) and brown-in/out protection, this chip prevents the circuit from being damaged in abnormal conditions.

Furthermore, the LD5760T features frequency trembling and soft driving function to minimize the noise and improve EMI.

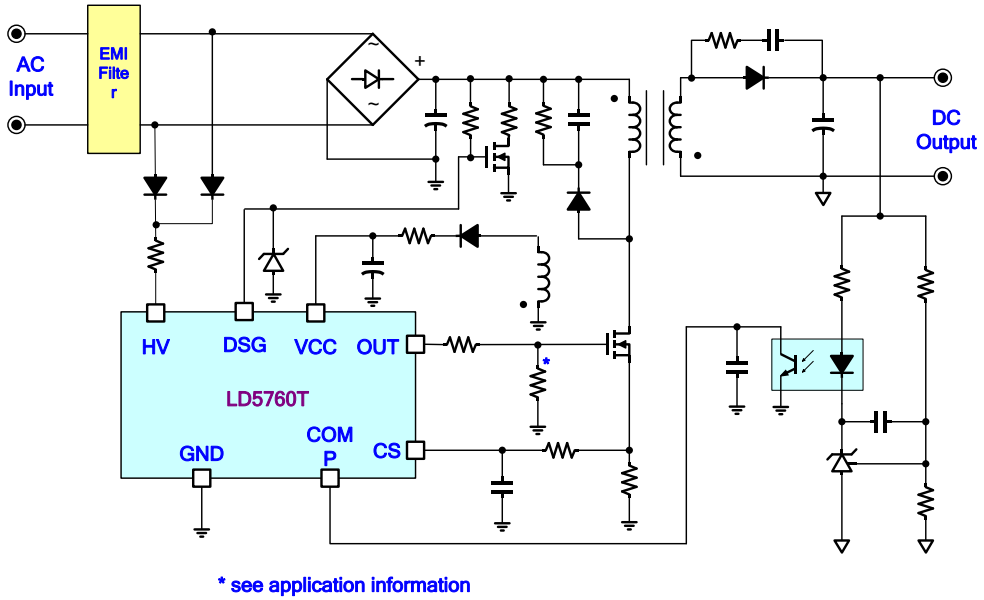
Features

- High-Voltage (650V) Startup Circuit
- Built-in Brown-in/out Function on HV pin
- Built- in X-Cap Discharge on HV pin
- Frequency Trembling for EMI improve
- Power Fail Control on DSG pin
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Slope Compensation
- Internal OCP Compensation
- OVP (Over Voltage Protection) on Vcc
- OLP (Over Load Protection)
- OTP (Over Temperature Protection)
- SCP(Short Circuit Protection)
- Bulk Open Protection
- Soft Start
- Soft Driving
- +300mA/-800mA Driving Capability

Applications

- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

Typical Application



Pin Configuration

SOP-8 & DIP-8 (TOP VIEW)

SOP-7 (TOP VIEW)

YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Frequency Trembling	Switching Freq.	Package	Top Mark	Shipping
LD5760T GS	Yes	130kHz	SOP-8	LD5760TGS	2500 /tape & reel
LD5760T GR	Yes	130kHz	SOP-7	LD5760TGR	2500 /tape & reel

The LD5760T is ROHS compliant/ Green Packaged.

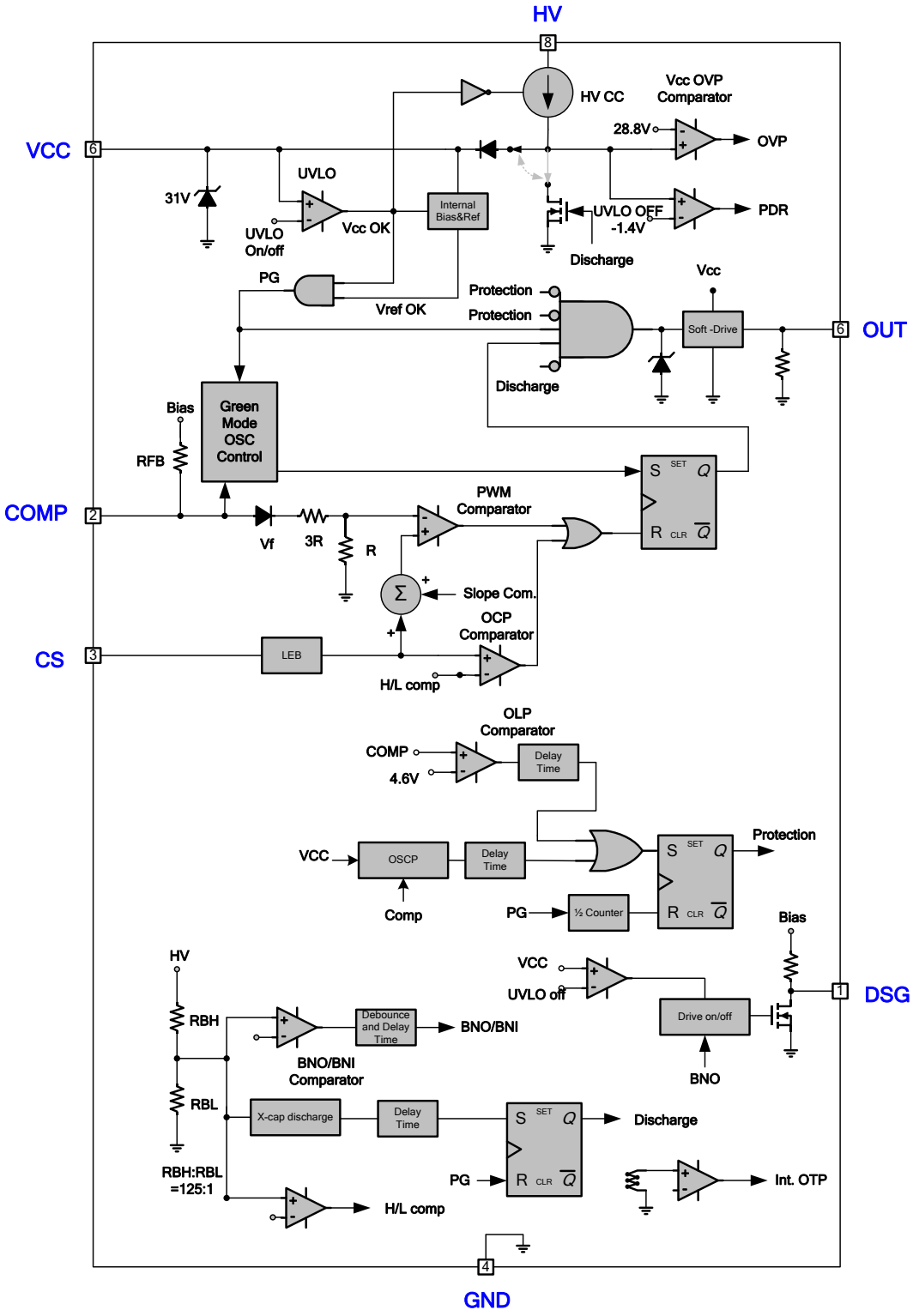
Protection Mode

Part number	VCC_OVP	OSCP	Bulk OVP	OLP	CS_OVP
LD5760T	Auto-Restart	Auto-Restart	Auto-Restart	Auto-Restart	Auto-Restart

Pin Descriptions

PIN	NAME	FUNCTION
1	DSG	Gate drive output to drive the external MOSFET. If input voltage is lower than brown out level, this DSG signal will be turned on the external MOSFET.
2	COMP	Voltage feedback pin, By connecting a photo-coupler to close the control loop and achieve the regulation.
3	CS	Current sense pin, connect to sense the MOSFET current
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Supply voltage pin
7	NC	Unconnected Pin
8	HV	Connect this pin to Line/Neutral of AC main voltage through resistor to provide the startup current for the controller. When Vcc voltage trips the UVLO(on), this HV loop will be turned off to reduce the power loss on the startup circuit. An internal resistor divider built-in between HV to GND pin to monitor AC line voltage, execute Brown-in/out function and detect High/low line compensation to achieve constant output power limiting.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V~30V
High-Voltage Pin, HV	-0.3V~650V
COMP, CS	-0.3 ~6V
DSG	-0.3 ~5V
OUT	-0.3 ~VCC+0.3V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8/ SOP-7, θ_{JA})	160°C/W
Power Dissipation (SOP-8/SOP-7, at Ambient Temperature = 85°C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV Pin)	2.5KV
ESD Voltage Protection, Machine Model (except HV Pin)	250V
ESD Voltage Protection, Human Body Model (HV Pin)	1KV
ESD Voltage Protection, Machine Model (HV Pin)	200V
Gate Output Current	300mA/800mA

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.5	26.5	V
HV resistor Value (AC Side)	8	17.5	KΩ
HV to GND Capacitor Value	--	300	pF
Comp Pin Capacitor	1	10	nF
CS Pin Capacitor Value	47	390	pF

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)						
High-Voltage Current Source	VCC< V_{CC-ON}, HV=500V	I_{HV}	2	2.8	3.6	mA
HV Discharge capability	HV=500V	I_{HV_DIS}	2	2.8	3.6	mA
HV Pin Total Input Current	VCC > V_{CC-ON}, HV=500 V_{DC}	I_{HV_LEAK}			35	μA
HV Pin Brown-In Level		V_{HVBI}	85	95	105	V_{DC}
HV Pin Brown-out Level		V_{HVBO}	74	82	90	V_{DC}
HV Pin BNO Hysteresis	V_{HVBI} - V_{HVBO}	ΔV_{HV}		15		V_{DC}
Brown-in De-bounce Time		T_{D_HVBI}		170		μS
Brown-out Detection Delay time		T_{D_HVBO}		200		mS
HV Pin Min. Operation Voltage		V_{HV_MIN}	45			V
X-Cap discharge Detection Delay time		T_{D_XCAP}		100		mS
Supply Voltage (VCC Pin)						
Startup Current	HV=500V	I_{CC_ST}		25	50	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=3V	I_{CC_OP1}		2.8		mA
	V_{COMP}=0V	I_{CC_OP2}		0.65		mA
	Auto recover mode	I_{CC_OPA}		0.43		mA
UVLO(OFF)		V_{CC_OFF}	6	7	8	V
UVLO(ON)		V_{CC_ON}	15	16	17	V
PDR		V_{CC_PDR}		V_{CC-OFF} -1.4V		V
VCC HVBI Level	HV> V_{HVBI} (Fig. 1)	V_{CC_HVBI}		V_{CC-OFF} +3.8V		V
VCC OVP Level		V_{CC_OVP}	27.8	28.8	29.8	V
VCC OVP De-bounce Time		T_{D_VCCOVP}		80		μS

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency						
Frequency		F_{SW}	110	125	140	KHz
Swapping Frequency		F_{SW_SWA}	±6	±8	±10	%
Modulation Frequency		F_{SW_MOD}	180	200	220	Hz
F_{SW} Temp. Stability	-40°C ~105°C	F_{SW_TS}	0	3	4	%
F_{SW} Voltage Stability	V_{CC}=8V-(OVP-1V)	F_{SW_VS}	0		1	%
Maximum On Time	HV>255Vdc	MXD_H		45		%
Maximum On Time	HV<255Vdc	MXD_L	78	85	90	%
OSCP (Output Short Circuit Protection)						
OSCP Trip Level	*	V_{CC_OSCP}		V_{CC_OFF} +2.4V		V
OSCP Delay Time	*Exclude soft start time	T_{D_OSCP}	5	10	15	ms
Voltage Feedback (Comp Pin)						
Input Voltage to Current-Sense Attenuation	*	A_V		1/4.0		V/V
Comp Impedance	V_{COMP}=3V	Z_{COMP}		25		kΩ
Open Loop Voltage	COMP pin open	V_{COMP_OPEN}	4.9	5.2	5.5	V
OLP Tripped Level	TC: track COMP pin open voltage	V_{OLP}	4.4	4.6	4.8	V
Zero Duty Threshold	Zero Duty, V_{FB_B}	V_{ZDC}	0.8	1	1.2	V
VCOMP on Burst mode	Hysteresis	V_{ZDCH}		200		mV
Current Sensing (CS Pin)						
Maximum Input Voltage(Vcs_off)	HV=125Vdc	V_{CS_MAX}	0.59	0.62	0.65	V
Minimum Input Voltage(Vcs_min)	HV=375Vdc	V_{CS_MIN}	0.43	0.45	0.47	V
Instant Maximum Input Voltage	(-20°C ~125°C)	$V_{\_2nd}$		1.3		V
Instant Maximum Input Voltage De-bounce cycle	(-20°C ~125°C)	$T_{\_2nd}$		8		Cycle
Leading Edge Blanking Time		T_{LEB}		200		nS
Delay to Output		T_{PD}		70	120	nS
Slope Compensation Level	*0%-85% Linearly	V_{SLP_L}	0		0.2	V
Slope Compensation Position	*0%-85% Linearly	V_{SLP}	0		85	%

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Gate Drive Output (OUT Pin)						
Output Low Level	VCC=15V, Io=20mA	V_{OL}	0	-	1	V
Output High Level	VCC=15V, Io=20mA	V_{OH}	8	-	Vcc	V
Rising Time	Load Capacitance= 1000pF @ from OUT>4V	T_r	-	50	95	nS
Falling Time	Load Capacitance= 1000pF	T_f	-	20	50	nS
OUT Pin Clamping Voltage	V_{CC}= 21V,1nF on OUT pin	V_{O_CLAMP}		12		V
Source capability	*Load Capacitance= 33nF@out=4V	I_{SOURCE}	300		550	mA
Sink capability	*Load Capacitance=33nF	I_{SINK}	750		1000	mA
OLP (Over Load Protection)						
OLP Delay Time	Auto restart, F_{SW}=125KHz	T_{D_OLP}	55	66	77	mS
Soft Start						
Soft Start Duration	UVLO(on) to PWM on (increase Fsw slowly)	T_{SS}		11		mS
Internal OTP						
OTP Tripped Level	*	T_{INOTP}		150		°C
OTP Hysteresis	*	T_{INOTP_HYS}		T_{OTP}-30		°C
OTP De-bounce Time	*	T_{D_INOTP}		160		µS
DSG (DSG Pin)						
DSG Pin Pull Low Resistor		R_{DSG}		5		kΩ

Typical Characteristics

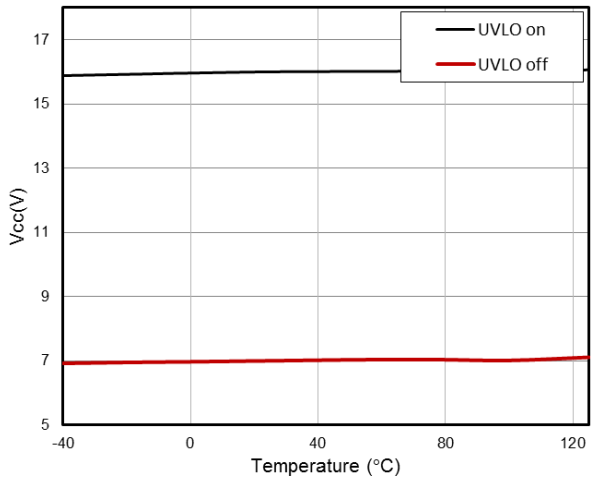


Fig. 1 UVLO level vs.Temperature

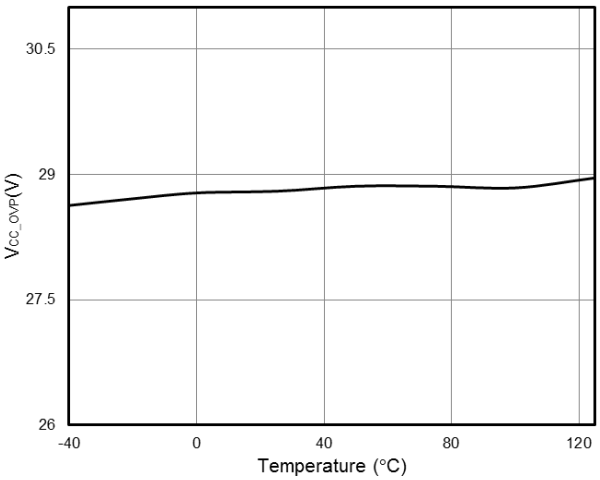


Fig. 2 VCC OVP vs.Temperature

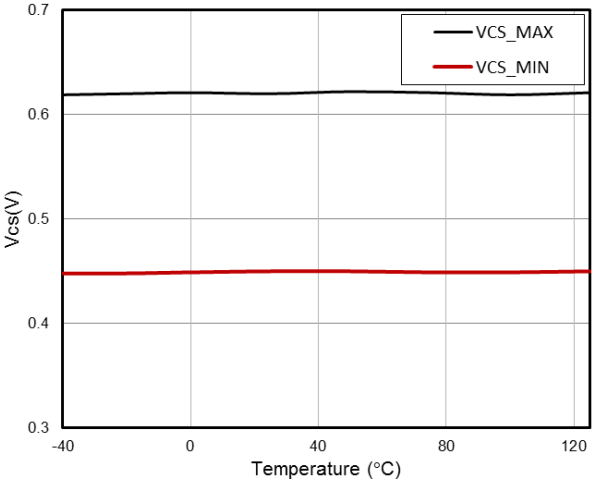


Fig. 3 VCS_MAX & VCS_MIN vs.Temperature

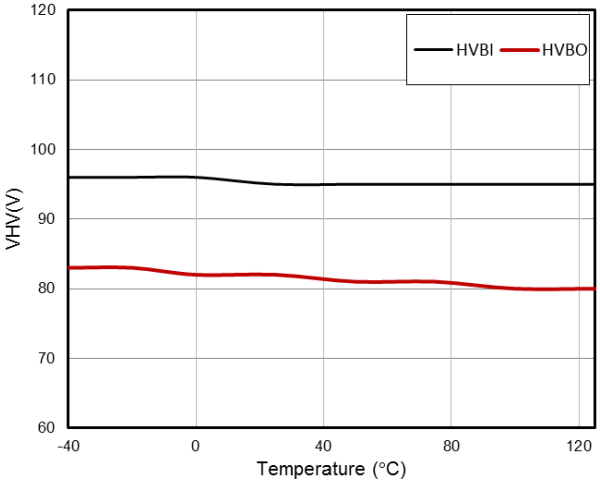


Fig. 4 HVBI & HVBO vs.Temperature

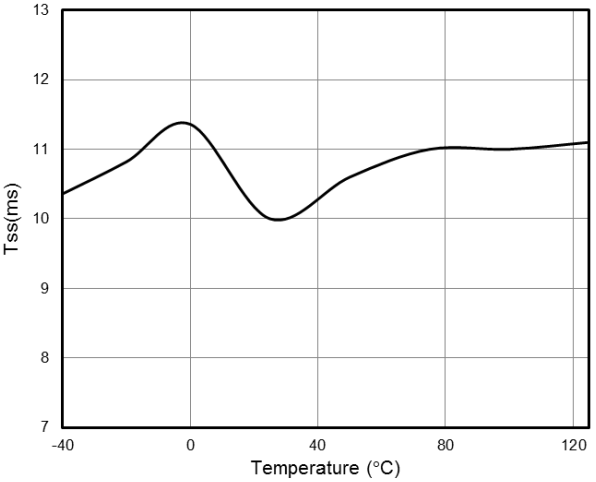


Fig. 5 Tss vs.Temperature

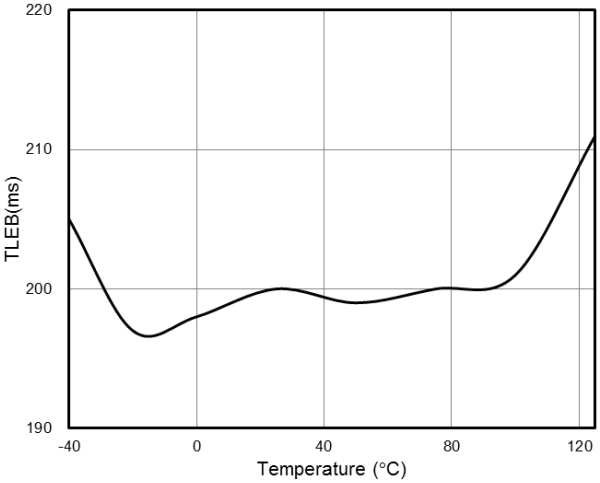


Fig. 6 TLEB vs.Temperature

Application Information

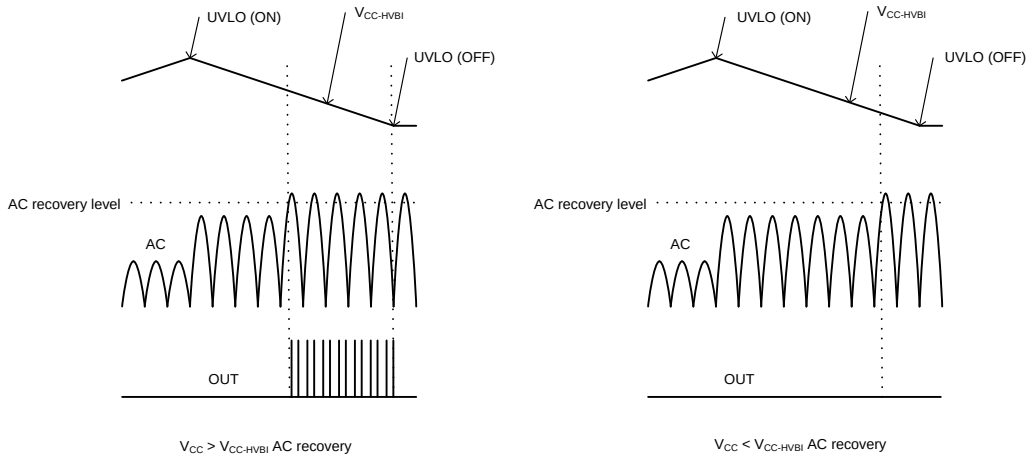


Fig 7 $V_{CC-HVBI}$ & AC recovery

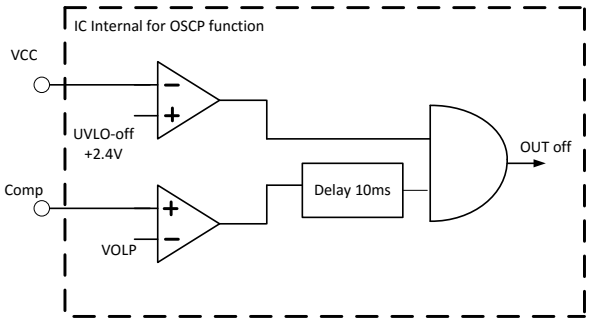


Fig. 8 OSCP Operation

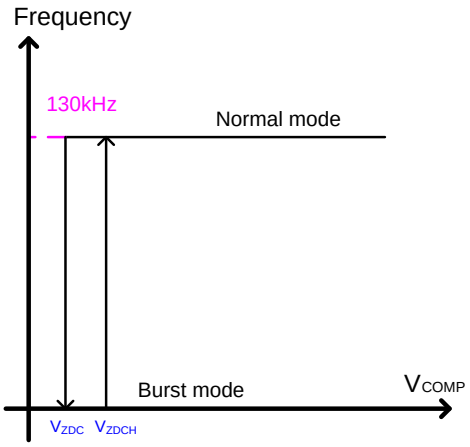


Fig. 9 V_{COMP} vs. PWM Frequency

Operation Overview

As long as the requirement for green power becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Due to the cost and size limit, the PWM controller designer is bound to integrate with more functions to reduce the external part counts. The LD5760T is ideal for these applications. Its detailed features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes much significant power to meet the current power saving requirement. In most cases, startup resistors carry larger resistance and spend more time to start up.

To achieve the optimized topology, as shown in Fig. 10, LD5760T is implemented with a high-voltage startup circuit for such requirement. At startup, the high-voltage current source sinks current of AC Line/or Neutral to provide startup current and charge the capacitor C1 connected to VCC.

At the startup transient, the HV current will supply around 2.8mA to Vcc capacitor until this VCC voltage reaches the UVLO threshold VCC. By using such configuration, the turn-on delay time will be almost same no matter under low-line or high-line conditions.

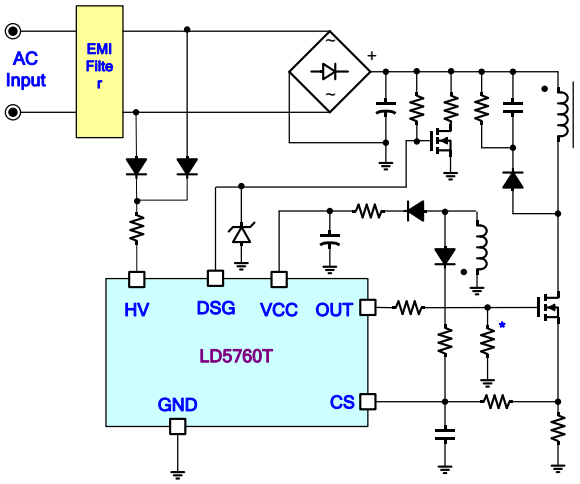


Fig. 10

As VCC trips UVLO(OFF), HV pin will recharge VCC capacitor till VCC voltage rises back to UVLO(ON) again. Since then, HV pin would no longer charge the capacitor and instead, send a gate drive signal to draw supply current for VCC from the auxiliary winding of the transformer. That minimizes the power loss on the start-up circuit successfully.

An UVLO comparator is embedded to detect the voltage across the VCC pin to ensure the supply voltage enough to power on the LD5760T and in addition, to drive the power MOSFET. As shown in Fig. 11, a hysteresis is provided to prevent shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16V and 7V, respectively.

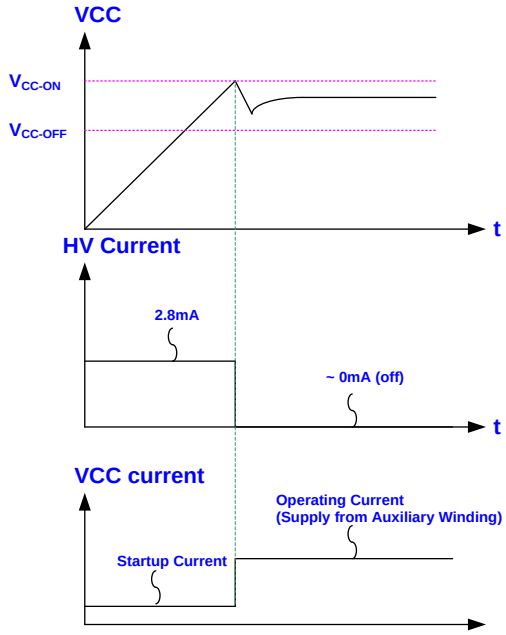


Fig. 11

Brown in/out Protection

The LD5760T features Burn-in/out function on HV pin. As the built-in comparator detects the half wave rectify line voltage condition, it will shut off the controller to prevent from any damage. Fig. 12 shows the operation. When V_{HV} < HVBO, the gate output will remain off even when the VCC already reaches UVLO(ON). It therefore forces the VCC hiccup between UVLO(ON) and UVLO(OFF). Unless the line voltage rises over HVBI V_{AC}, the gate output will not start switching even as the next UVLO(ON) is tripped. A hysteresis is implemented to prevent the false-triggering during turn-on and turn-off.

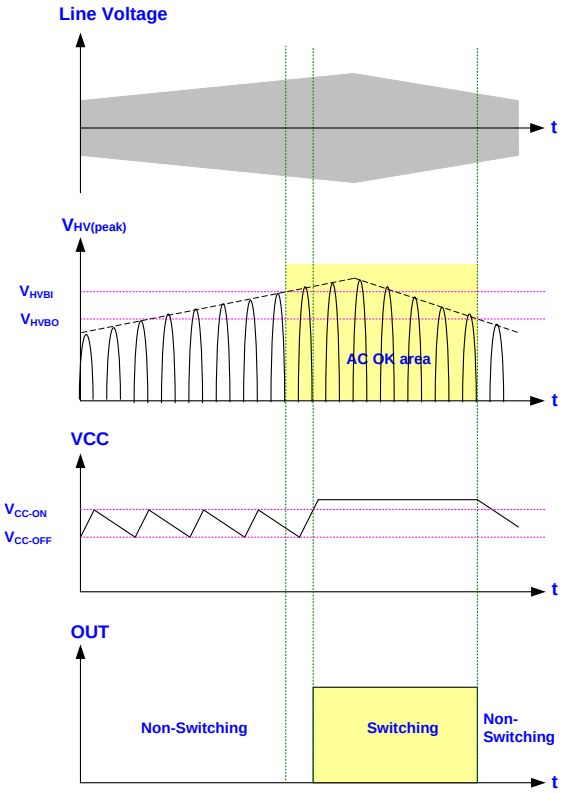


Fig. 12

Current Sensing, Leading-Edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD5760T detects the primary MOSFET current across CS pin to control in peak current mode and also limit the pulse-by-pulse current.

The maximum voltage threshold of the current sensing pin is set to 0.62V when HV=125V and 0.45V when HV=375V. BY this means the input voltage OLP compensation is achieved. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.45V \sim 0.62V}{R_S}$$

A 300nS leading-edge blanking (LEB) time is designed in the input of CS pin to prevent false-triggering from the current spike. In the low power applications, if the total pulse width of the turn-on spikes is less than 150nS and

the negative spike on the CS pin does not exceed -0.3V, the R-C filter (as shown in Fig. 13) is free to eliminate.

However, the total pulse width of the turn-on spike is related to the output power, circuit design and PCB layout. It is strongly recommended to add a small R-C filter (as shown in Fig. 14) for larger power application to avoid the CS pin from being damaged by the negative turn-on spike.

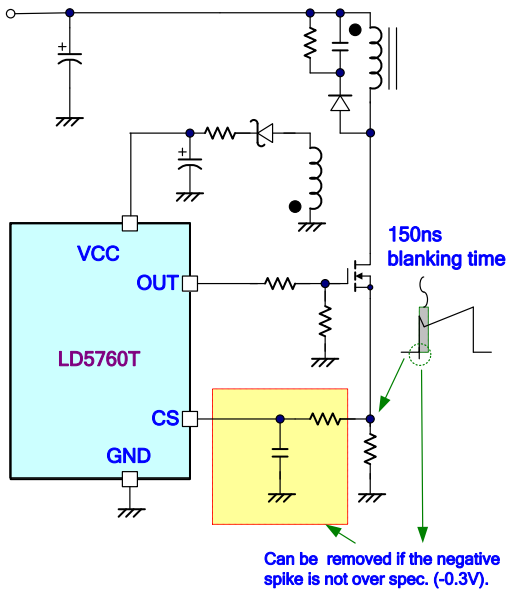


Fig. 13

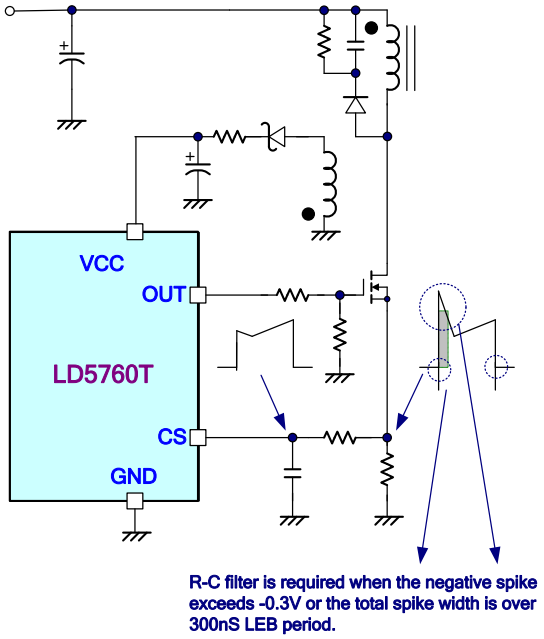


Fig. 14

Output Stage and Maximum Duty-Cycle

A CMOS buffer with output stage of typical 300mA driving capability is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD5760T is limited to 85% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 on the secondary side through the photo-coupler to the COMP pin of LD5760T. Similar to UC384X, its input stage is with a diode voltage offset to feed the voltage divider with 1/4 ratio, that is,

$$V_{CS(PWM\ COMPARATOR)} = \frac{1}{4} \times (V_{COMP} - V_F)$$

A pull-high resistor is embedded internally to optimize the external circuit.

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is operated for more than 50%. To stabilize the control loop, the slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin

through a coupling capacitor. LD5760T has internal slope compensation circuit to simplify the external circuit design.

Oscillator and Switching Frequency

The LD5760T fixes the switching frequency at 130kHz internally to optimize its performance in EMI, thermal treatment, component sizes and transformer design.

Frequency Swapping

The LD5760T is built in with frequency swapping function, which makes it easy for the power supply designers to optimize EMI performance and system cost. The frequency swapping is internally set for ±8%.

On/Off Control

Pulling COMP pin below VFB_B will immediately disable the gate output of LD5760T. Remove the pull-low signal to reset it.

Over Load Protection (OLP) - Auto Recovery

To protect the circuit from being damaged during over load condition and short or open loop condition, the LD5760T is implemented with smart OLP function. LD5760T features auto recovery function of it, see Fig. 15 for the waveform. In the example of the fault condition, the feedback system will force the voltage loop enter toward the saturation and then pull the voltage high on COMP pin (VCOMP). As the V_{COMP} ramps up to the OLP tripped level (4.6V) and stays for more than the OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit. The OLP delay time is set by internal high frequency counter. It is to prevent the false triggering from the power-on and turn-off transient.

A divide-2 counter is implemented to reduce the average power under OLP behavior. As soon as OLP is activated, the output will be latched off and the divide-2 counter will start to count the number of UVLO(OFF). The latch will not be released until the 3rd UVLO(OFF) point is counted, after that the output will resume to switch again. With the protection mechanism, the average input power will be minimized, so that the component temperature and stress can be controlled within the safe operating area.

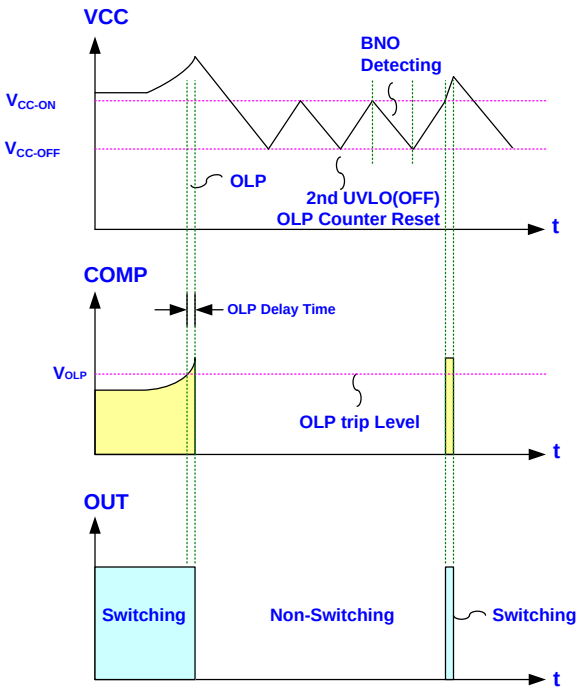


Fig. 15

OVP (Over Voltage Protection) on VCC –Auto Recovery

The maximum VCC ratings of the LD5760T are mostly for 30V. To prevent the controller enter fault condition, LD5760T series are implemented with OVP function on Vcc. Whenever the Vcc voltage is higher than the OVP threshold, the output gate drive circuit will be shutdown simultaneously and the switching of the power MOSFET is disabled until the next two UVLO(on).

The Vcc OVP functions of LD5760T are auto-recoverable. If the OVP condition, usually caused by open-loop of feedback, is not released, the Vcc will tripped the OVP level again and re-shutdown the output. The Vcc works in hiccup mode. Figure 17 shows its operation.

Otherwise, when the OVP condition is removed, the Vcc level will be resumed and the output will automatically return to the normal operation.

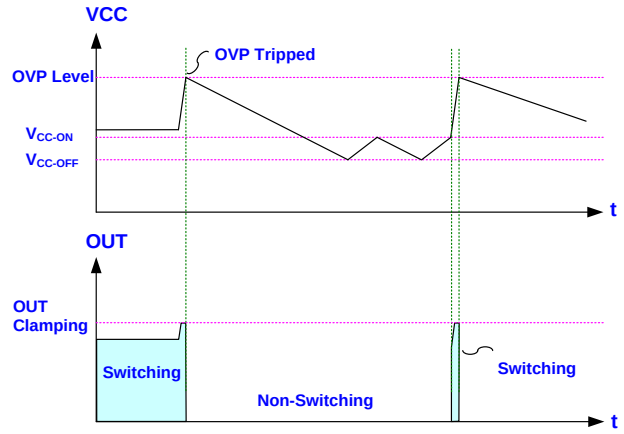


Fig. 16

On-Chip OTP - Auto Recovery

An internal OTP circuit is embedded inside the LD5760T to provide the worst-case protection for this controller. When the chip temperature rises higher than the trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window.

DSG PIN Function

The VCC voltage reaches the UVLO threshold on, and DSG pin will sink a current to pull low external MOSFET until HV Pin detects AC input which is lower than brown out protection level. It can meet safety specification of bulk voltage at AC off condition.

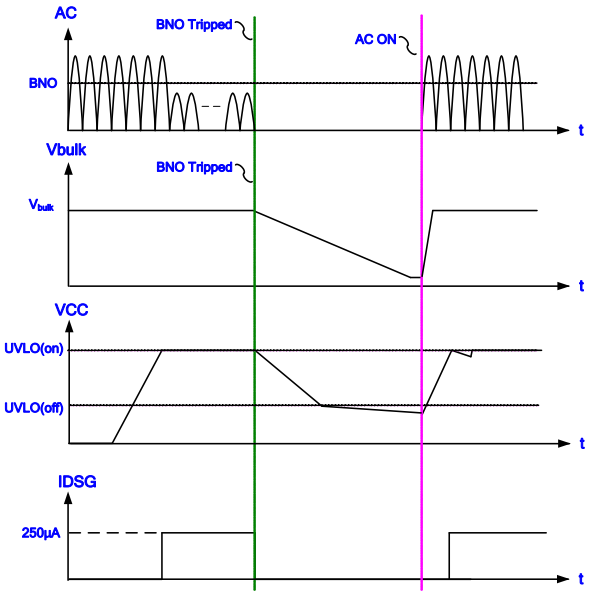


Fig. 17

Pull-Low Resistor on the Gate Pin of MOSFET

The LD5760T consists of an anti-floating resistor with OUT pin to protect the output from damage in abnormally operation or condition due to false triggering of MOSFET. Even so, we still recommend adding an external one at the MOSFET gate terminal to provide more protection in case of disconnection of gate resistor R_G during power-on.

In such single-fault condition, as shown in Fig. 18, the resistor R8 can provide a discharge path to avoid the MOSFET from being false-triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the MOSFET should be always pulled low and placed in the off-state as the gate resistor is disconnected or opened in any case.

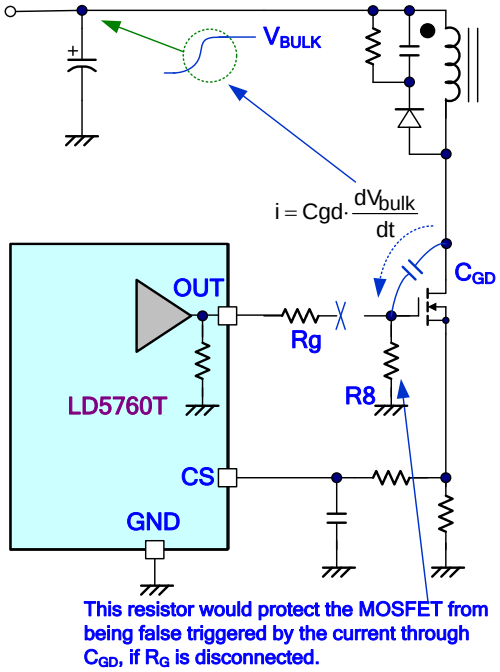


Fig. 18

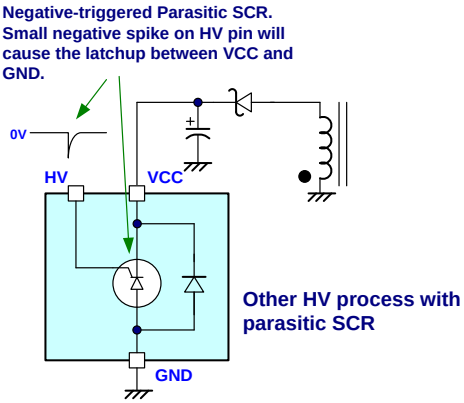


Fig. 19

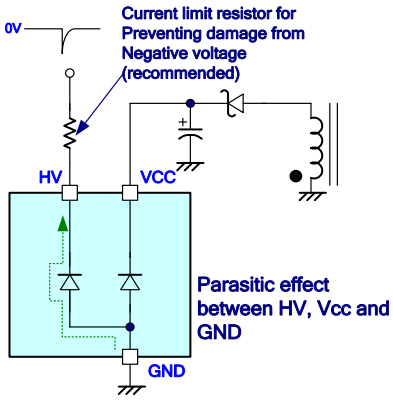


Fig. 20

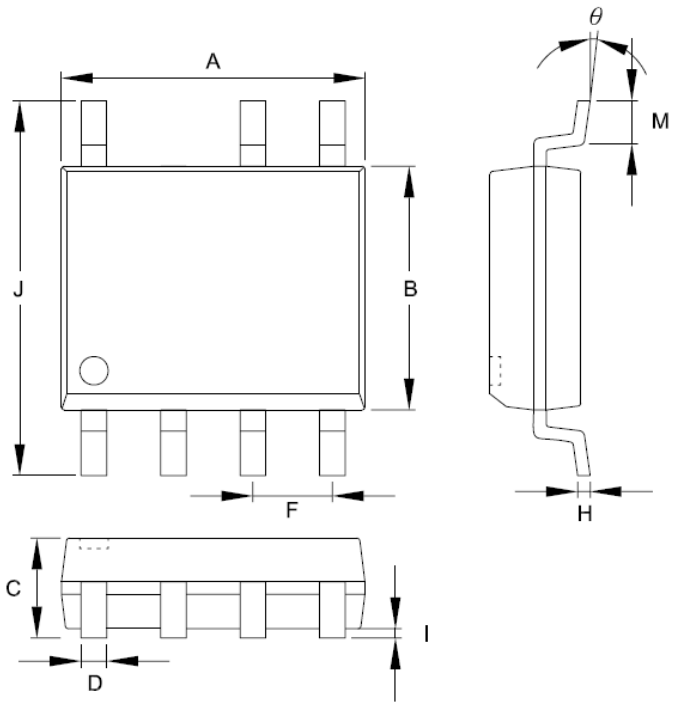
Protection Resistor on the Hi-V Path

In some other Hi-V process and design, there may be a parasitic SCR caused around HV pin, Vcc and GND. As shown in Fig. 19, a small negative spike on the HV pin may trigger this parasitic SCR and cause latch-up between VCC and GND. It may damage the chip because of the equivalent short-circuit induced by such latch-up behavior.

Leadtrend's proprietary of Hi-V technology will eliminate parasitic SCR in LD5760T. Fig. 20 shows the equivalent Hi-V structure circuit of LD5760T. So that LD5760T is more capable to sustain negative voltage than similar products. However, a 10KΩ resistor is recommended to add in the Hi-V path to play as a current limit resistor as a negative voltage is applied.

Package Information

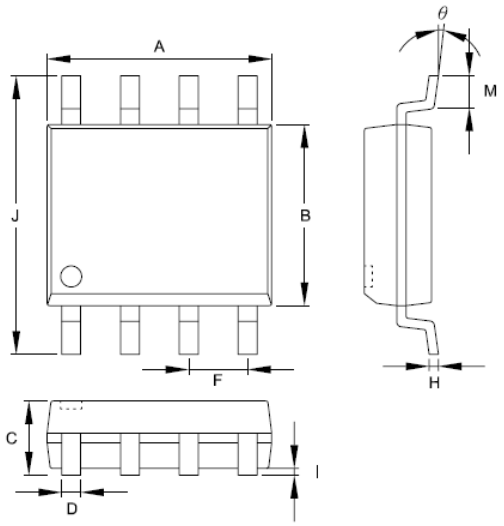
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

SOP-8



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M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	02/23/2016	Original Specification
01	03/17/2016	Add Recommended Operating Condition: C_{HV} to GND