High Voltage with Two-Level Frequency Green-Mode PWM Controller

REV: 01

General Description

The LD5761 is a Green Mode PWM IC which is built-in with brown-in/out functions in a SOP-7/SOP-8 package. The device could minimize the component counts, circuit space, and reduces the overall material cost of power applications.

The two-level frequency of operation enables excellent performance and high efficiency at nominal line. While in low line, just operate in high-level frequency to reduce $B_{MAX.}$ Without changing transformer design, the energy loss is perfectly minimized.

With complete protections in it, like OLP (Over Load Protection), OVP (Over Voltage Protection), fast OSCP (Output short circuit protection) and brown-in/out protection, the LD5761 protects the circuit from being damaged in abnormal conditions.

Furthermore, the LD5761 features frequency swapping and soft driving function to minimize the noise and enhance EMI.

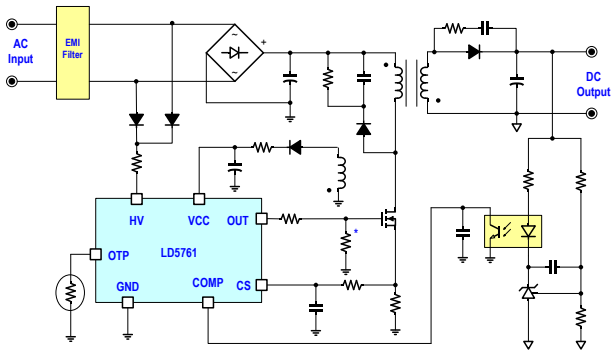
Features

- High-Voltage (650V) Start-up Circuit
- No-Load Power Consumption <30mW @230Vac with X-cap discharge
- Two-Level Frequency Operation at H/L Line
- Built- in Brown-in/out Function on HV pin
- Built- in X-Cap Discharge on HV pin
- Frequency Swapping for EMI Enhancement
- Non-Audible-Noise Green Mode Control
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Slope Compensation
- OVP (Over Voltage Protection) on VCC
- OLP (Over Load Protection)
- OTP (Over Temperature Protection)
- OSCP(Output Short Circuit Protection)
- Soft Driving
- +300mA/-800mA Driving Capability

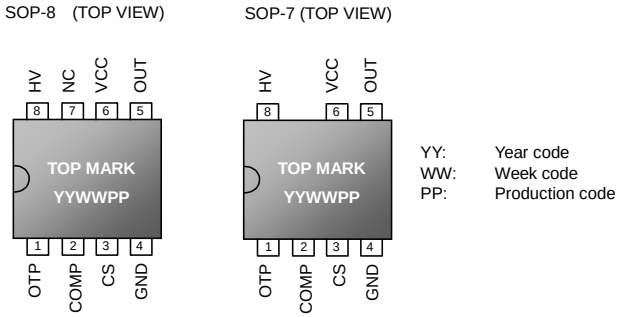
Applications

- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

Typical Application



Pin Configuration



Ordering Information

Part number	Package	Top Mark	Shipping
LD5761 GS	SOP-8	LD5761GS	2500 /tape & reel
LD5761 GR	SOP-7	LD5761GR	2500 /tape & reel

The LD5761 is ROHS compliant/Green Packaged.

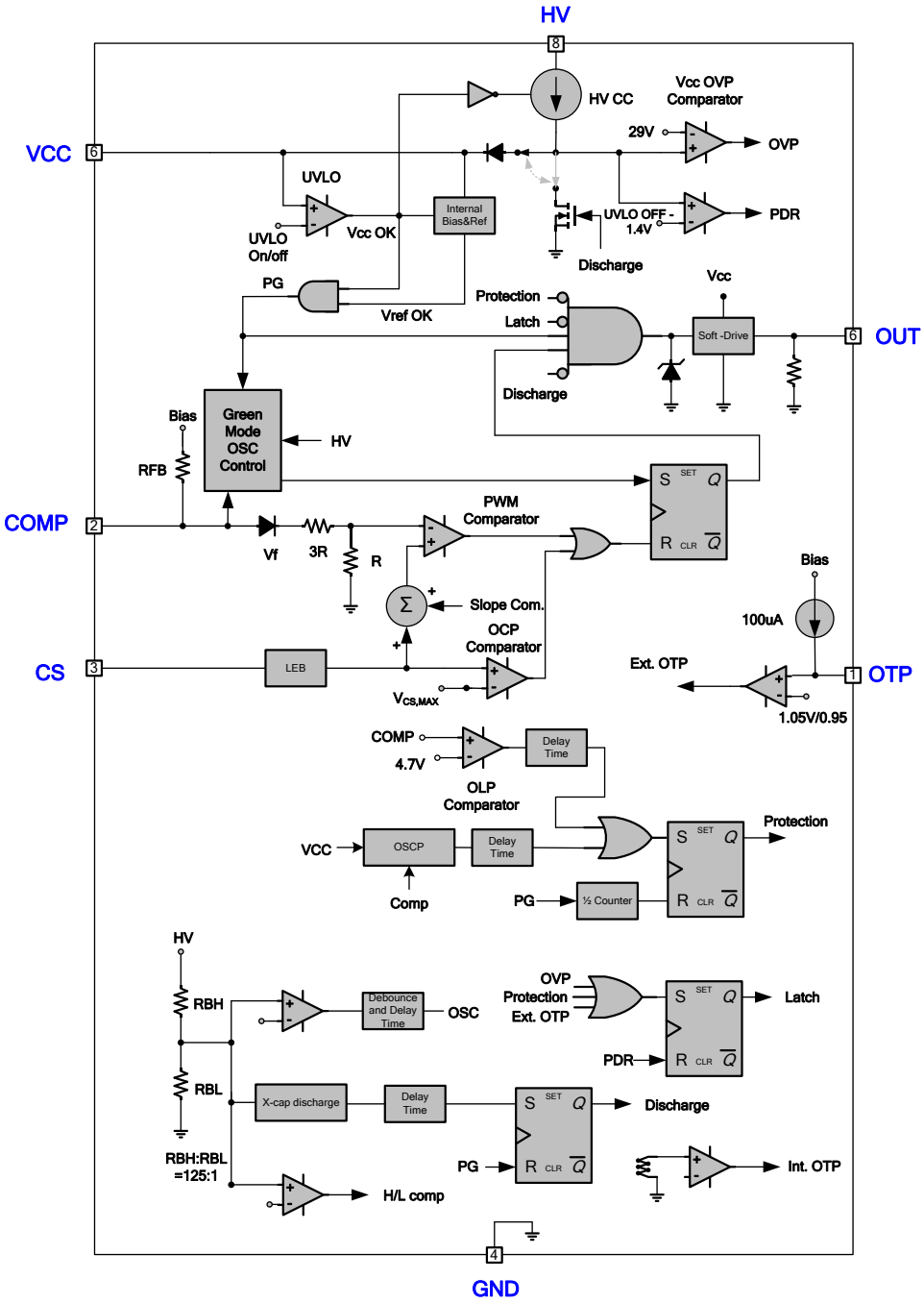
Protection Mode

Part number	VCC_OVP	OSCP	OLP	OTP
LD5761	Latch	Latch	Latch	Latch

Pin Descriptions

PIN	NAME	FUNCTION
1	OTP	Pulling this pin below 0.95V will force the controller enter into latch mode and it will not resume until the AC power recycles. Connect a NTC between this pin and ground to achieve OTP protection function. Let this pin float to disable the latch protection.
2	COMP	Voltage feedback pin. Connect a photo-coupler with it to close the control loop and achieve the regulation.
3	CS	Current sense pin, connect it to sense the MOSFET current
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Supply voltage pin
7	NC	Unconnected Pin
8	HV	Connect this pin to Line/ Neutral of AC main voltage through a resistor to provide the start-up current for the controller. When VCC voltage increase to trip the point of UVLO(on), this HV loop will be turned off to reduce the power loss on the start-up circuit. An internal resistor divider of HV pin will modulate the maximum frequency by control circuit. After AC disappear for few cycles, HV pin will sink current to discharge X-cap.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V~32V
High-Voltage Pin, HV	-0.3V~650V
COMP, OTP, CS	-0.3 ~6V
OUT	-0.3 ~VCC+0.3V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8/ SOP-7, θ_{JA})	160°C/W
Power Dissipation, PD@85°C (SOP-8/ SOP-7)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV Pin)	2.5KV
ESD Voltage Protection, Machine Model (except HV Pin)	250V
ESD Voltage Protection, Human Body Model (HV Pin)	1KV
ESD Voltage Protection, Machine Model (HV pin)	200V
Gate Output Current	300mA/800mA

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply VCC pin Voltage	8.5	27	V
HV Pin Series Resistor	8	120	kΩ
HV pin Capacitor	--	0	pF
Comp Pin Capacitor	1	10	nF
CS Pin Capacitor	47	390	pF

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)						
HV Pin Source Current	V_{CC} <UVLO$_{(ON)}$, HV=500V	I_{HV}	2.6	2.9	3.3	mA
HV Pin Discharge Capability	HV=500V	I_{HV_DIS}	2.2	2.6	3.0	mA
HV Pin Leakage Current	V_{CC} >UVLO$_{(ON)}$, HV=500V	I_{HV_LEAK}			35	μA
HV Pin Brown-In Level		V_{HVBI}	94.5	105	115.5	V_{DC}
HV Pin Brown-Out Level		V_{HVBO}	82.8	92	96.6	V_{DC}
HV Pin Hysteresis	V_{HVBI} - V_{HVBO}	V_{HVB_HYS}		13		V_{DC}
Brown-In De-bounce Time		T_{D_HVBI}		160		μS
Brown-Out De-bounce Time		T_{D_HVBO}		67		mS
Low Frequency Operation Range		V_{LSW}	265			V_{DC}
High Frequency Operation Range		V_{HSW}			195	V_{DC}
HV Pin Min. Operation Voltage	Vcc =15V	V_{HV_MIN}	45			V
X-Cap discharge Detection Delay time	V_{COMP} =3V	T_{D_XCAP}		65		mS
Supply Voltage (VCC Pin)						
Start-up Current	HV=500V	I_{CC_ST}		25	50	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=3V	I_{CC_OP1}		2		mA
	V_{COMP}=0V	I_{CC_OP2}	0.38	0.42	0.46	mA
	OTP Latch mode	I_{CC_OPLL}		0.55		mA
	Latch mode	I_{CC_OPL}		0.65		mA
UVLO$_{(OFF)}$		V_{CC_OFF}	6	7	8	V
UVLO$_{(ON)}$		V_{CC_ON}	15	16	17	V
PDR		V_{CC_PDR}		UVLO$_{OFF}$ - 1.4V		V
VCC HVBI Level	V_{CC} > V_{HVBI}, see Fig.1	V_{CC_HVBI}		UVLO$_{OFF}$ +4V		V

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
VCC OVP Level		V_{CC_OVP}	26	27.5	29	V
VCC OVP De-bounce Time		T_{D_VCCOVP}		120		μS
Oscillator for Switching Frequency						
Low Frequency	V_{COMP}=3.5V HV>265V	F_{LSW}	61		69	KHz
High Frequency	V_{COMP}=3.5V HV<195V	F_{HSW}	88		104	KHz
Green Mode Frequency	V_{COMP}= V_{ZDC}	F_{SW_GRN}	20		26	KHz
Modulation Frequency		F_{SW_MOD}		200		Hz
F_{SW} Temp. Stability	*-40°C ~105°C	F_{SW_TS}	0	3	4	%
F_{SW} Voltage Stability	*	F_{SW_VS}	0		1	%
Maximum Duty		D_{MAX}	78	85	90	%
OSCP (Output Short Circuit Protection)						
OSCP Trip Level	*	V_{CC_OSCP}		V_{CC_OFF} +4V		V
OSCP Delay Time	*, Exclude T_{SS}	T_{D_OSCP}		10		ms
Voltage Feedback (Comp Pin)						
Input Voltage to Current-Sense Attenuation	*	A_V		1/4		V/V
Comp Impedance	V_{COMP}=3V	Z_{COMP}	15	18	21	kΩ
Open Loop Voltage	Comp pin open	V_{COMP_OPEN}	4.9	5.2	5.5	V
OLP Tripped Level		V_{OLP}	4.5	4.7	4.9	V
PWM Mode Threshold V_{COMP} of Low Frequency	Frequency= 0.9*F_{LSW}, see Fig.2	V_{P_LSW}	2.80	2.95	3.10	V
Green Mode Threshold V_{COMP} of Low Frequency	Frequency= 1.1*$F_{LSW-GRN}$, see Fig.2	V_{G_LSW}	2.55	2.70	2.85	V
PWM Mode Threshold V_{COMP} of High Frequency	Frequency= 0.9*F_{HSW}, see Fig.2	V_{P_HSW}	2.00	2.15	2.30	V
Green Mode Threshold V_{COMP} of High Frequency	Frequency= 1.1*$F_{HSW-GRN}$, see Fig.2	V_{G_HSW}	1.85	2	2.15	V
Zero Duty Threshold V_{COMP} on Burst mode	Zero Duty in, see Fig.2	V_{ZDC}	1.55	1.7	1.85	V
	Zero Duty out, see Fig.2	V_{ZDCH}		V_{ZDC} +0.13V		V

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Current Sensing (CS Pin)						
Maximum limit Voltage		V_{CS_MAX}	0.684	0.72	0.756	V
Leading Edge Blanking Time		T_{LEB}		300		nS
Delay to Output		T_{PD}		90		nS
Slope Compensation Level	*0%-85% Linearly	V_{SLP_L}	0		0.3	V
Slope Compensation Position	*0%-85% Linearly	V_{SLP}	0		85	%
Gate Drive Output (OUT Pin)						
Output Low Level	V_{CC}=15V, Io=20mA	V_{OL}	0	-	1	V
Output High Level	V_{CC}=15V, Io=20mA	V_{OH}	9	-	V_{CC}	V
Rising Time	Load Capacitance=1nF	T_r		50		nS
Falling Time	Load Capacitance=1nF	T_f	-	20		nS
OUT Pin Clamping Voltage	Load Capacitance=1nF, V_{CC}= 21V	V_{O_CLAMP}		12		V
Source capability	*Load Capacitance=33nF	I_{SOURCE}		300		mA
Sink capability	*Load Capacitance=33nF	I_{SINK}		800		mA
OLP (Over Load Protection)						
OLP Delay Time		T_{D_OLP}	408	480	552	mS
Soft Start						
Soft Start Duration		T_{SS}		6		mS
Internal OTP						
OTP Tripped Level(T_{OTP})	*	T_{INOTP}		140		°C
OTP Hysteresis	*	T_{INOTP_HYS}		T_{INOT}-30		°C
OTP De-bounce Time	*	T_{D_INOTP}		160		µS
Over Temperature Protection(OTP Pin)						
OTP Pin Source Current		I_{OTP}	92	100	108	µA
Turn-On Trip Level		V_{OTP_ON}	1	1.05	1.1	V
Turn-Off Trip Level		V_{OTP_OFF}	0.9	0.95	1.00	V
OTP pin de-bounce time		T_{D_OTP}		300		µs

*: guaranteed by design

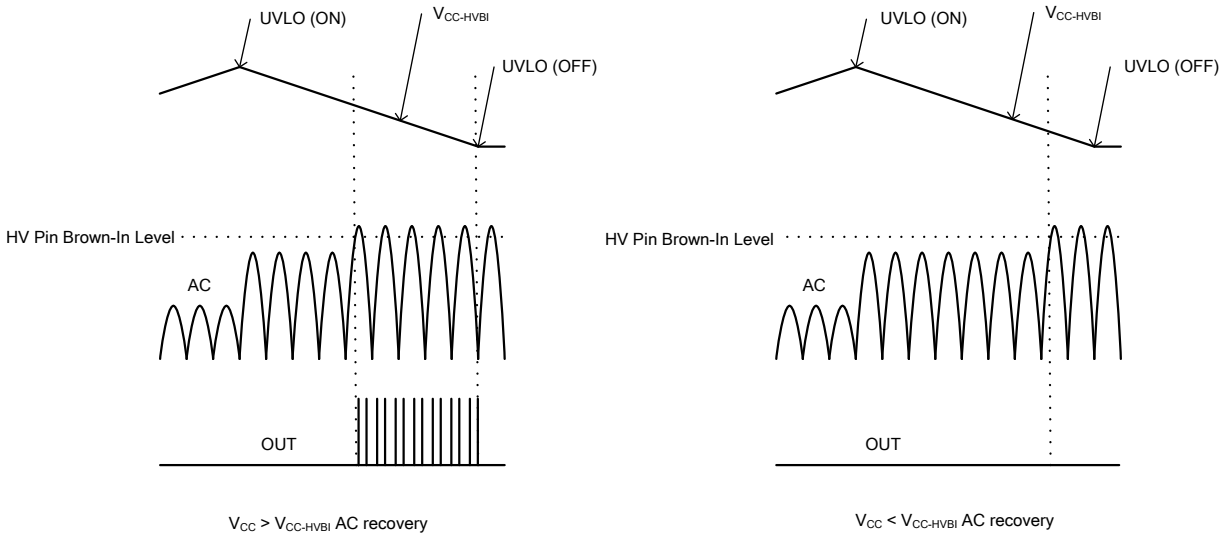


Fig. 1 $V_{CC-HVBI}$ & AC recovery

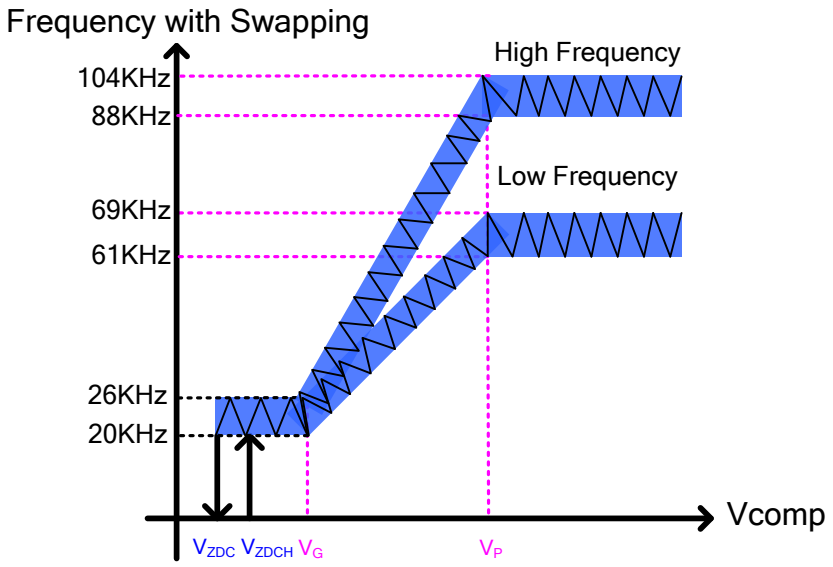


Fig. 2 V_{COMP} vs. Operation Frequency

Typical Performance Characteristics

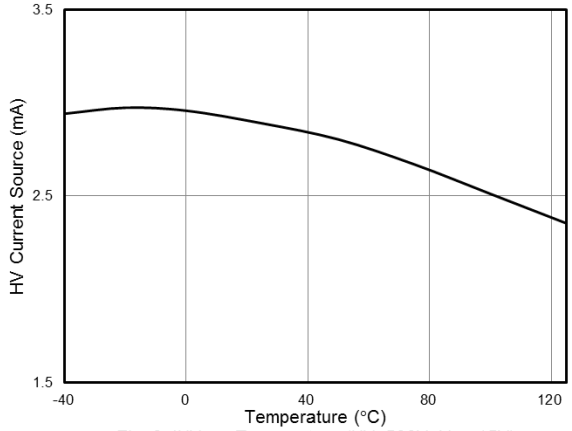


Fig. 3 IHV vs. Temperature (HV=500V, V_{CC}=15V)

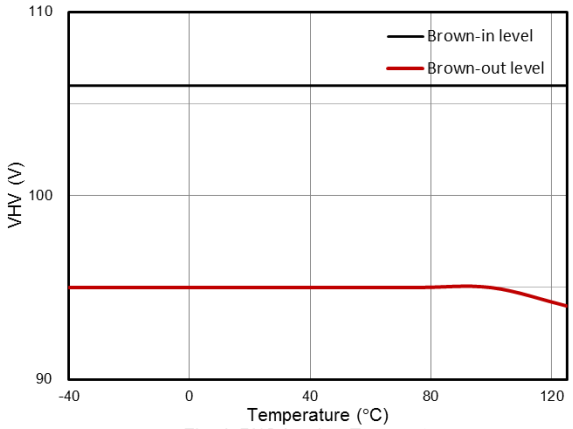


Fig. 4 BNO level vs.Temperature

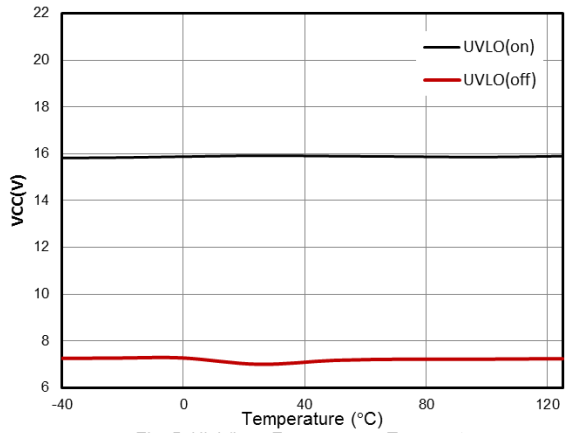


Fig. 5 High/Low Frequency vs.Temperature

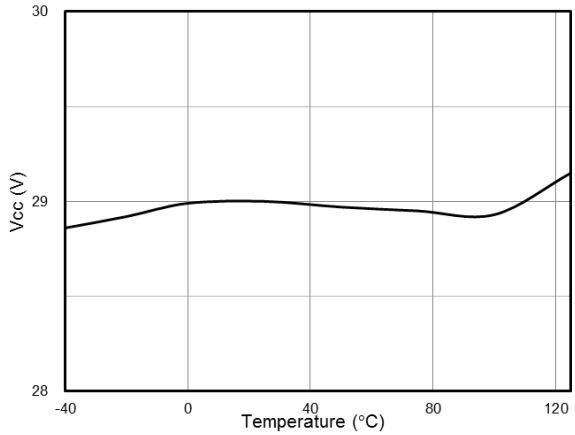


Fig. 6 Vcc OVP Level vs.Temperature

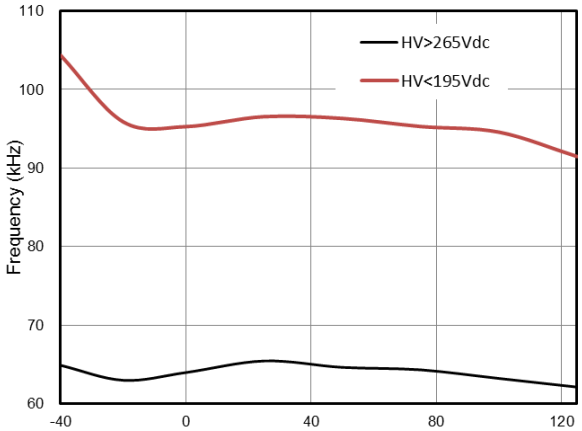


Fig. 7 High/Low Frequency vs.Temperature

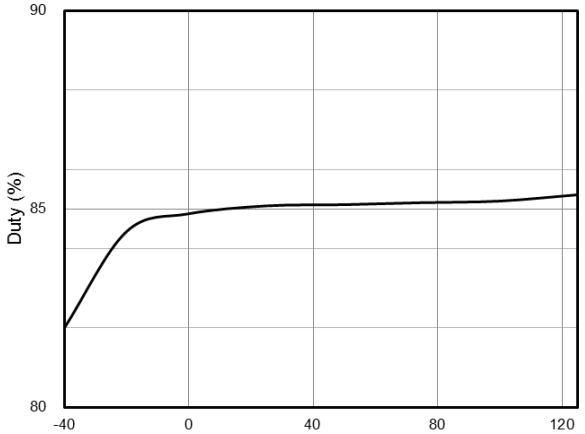


Fig. 8 Max Dutyvs.Temperature

Typical Performance Characteristics

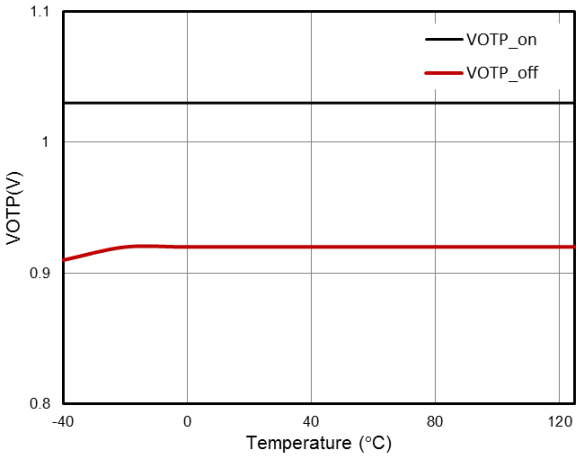


Fig. 9 External OTP Level vs.Temperature

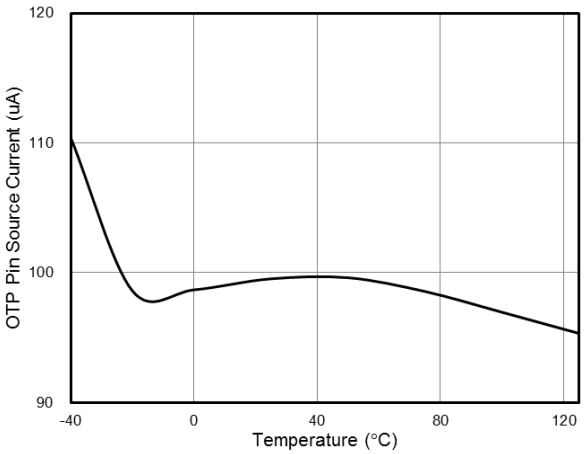


Fig. 10 OTP Pin Source Current vs.Temperature

Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation force the PWM controllers to be more powerful and with more functions to reduce the external part counts. The LD5761 is ideal for these applications. Its detailed features are described as below.

Internal High-Voltage Start-up Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the start-up current through a start-up resistor to power up the PWM controller. However, it consumes much significant power to meet the current power saving requirement. In most cases, start-up resistors carry larger resistance and spend more time to start-up.

To achieve the optimized topology, as shown in Fig. 11, LD5761 is implemented with a high-voltage start-up circuit for such requirement. At start-up, the high-voltage current source sinks current of AC Line or Neutral to provide start-up current and charge the capacitor C1 connected to VCC.

At the start-up transient, the HV current will supply around 2.9mA to VCC capacitor until this VCC voltage reaches the UVLO(on). By using such configuration, the turn-on delay time will be almost same no matter under low-line or high-line conditions.

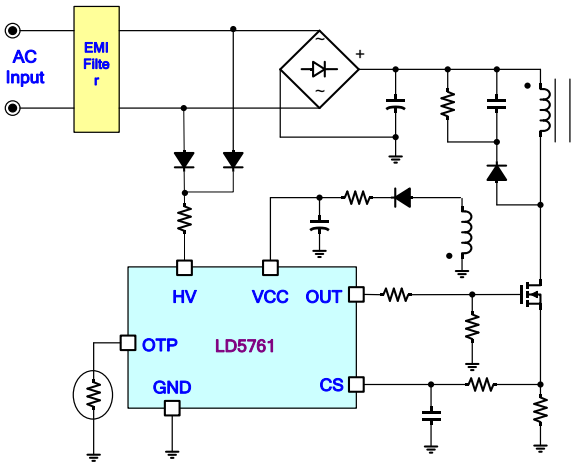


Fig. 11

As VCC trips UVLO(off), HV pin will recharge VCC capacitor till VCC voltage rises back to UVLO(on) again. Since then, HV pin would no longer charge the capacitor and instead, send a gate drive signal to draw supply current for VCC from the auxiliary winding of the transformer. That minimizes the power loss on the start-up circuit successfully.

An UVLO comparator is embedded to detect the voltage across the VCC pin to ensure the supply voltage enough to power on the LD5761 and in addition, to drive the power MOSFET. As shown in Fig. 12, a hysteresis is provided to prevent shutdown from the voltage dip during start-up. The turn-on and turn-off threshold level are set at 16V and 7V, respectively.

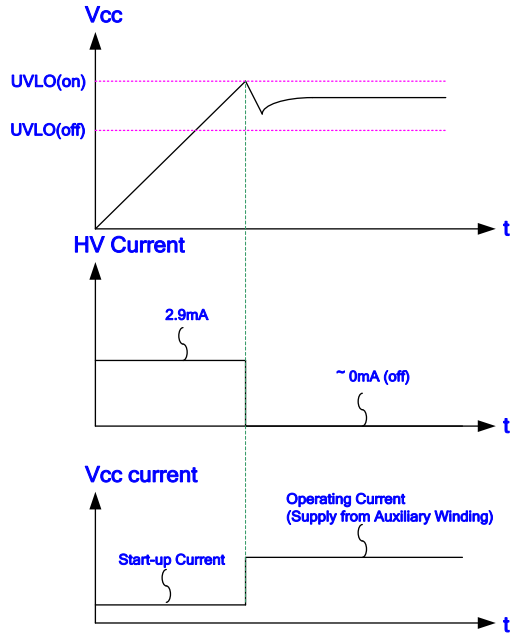


Fig. 12

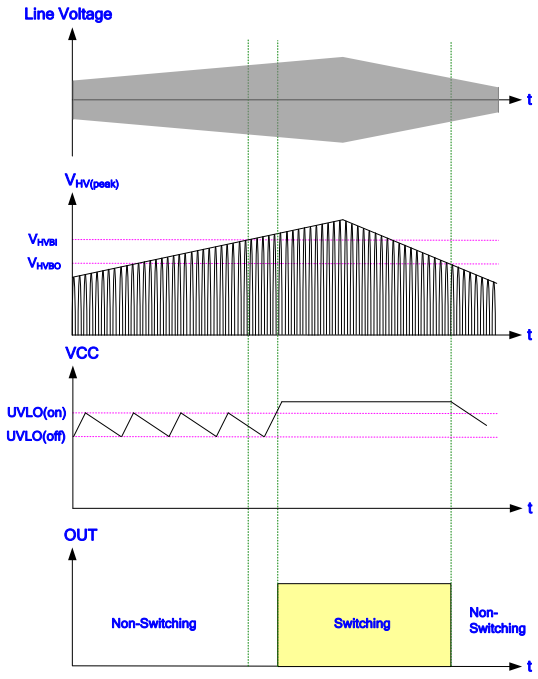


Fig. 13

Brown in/out Protection

The LD5761 features Burn-in/out function on HV pin. As the built-in comparator detects the half wave rectify line voltage condition, it will shut off the controller to prevent from any damage. Fig. 13 shows the operation. When $V_{HV} < H_{VBO}$, OUT pin will remain off even when the V_{CC} already reaches UVLO(ON). It therefore forces the V_{CC} hiccup between UVLO(ON) and UVLO(OFF). Unless the line voltage rises over HVBI, OUT pin will not start switching even as the next UVLO(ON) is tripped. A hysteresis is implemented to prevent the false-triggering during turn-on and turn-off.

Current Sensing, Leading-Edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD5761 detects the primary MOSFET current across CS pin to control in peak current mode and also limit the pulse-by-pulse current. The maximum voltage threshold of the current sensing pin is set at 0.72V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.72V}{R_S}$$

A 300nS leading-edge blanking (LEB) time is designed in the input of CS pin to prevent false-triggering from the current spike. In the low power applications, if the total pulse width of the turn-on spikes is less than 300nS and the negative spike on the CS pin does not exceed -0.3V, the R-C filter (as shown in Fig. 14) is free to eliminate.

However, the total pulse width of the turn-on spike is related to the output power, circuit design and PCB layout. It is strongly recommended to add a small R-C filter (as shown in Fig. 15) for larger power application to avoid the CS pin from being damaged by the negative turn-on spike.

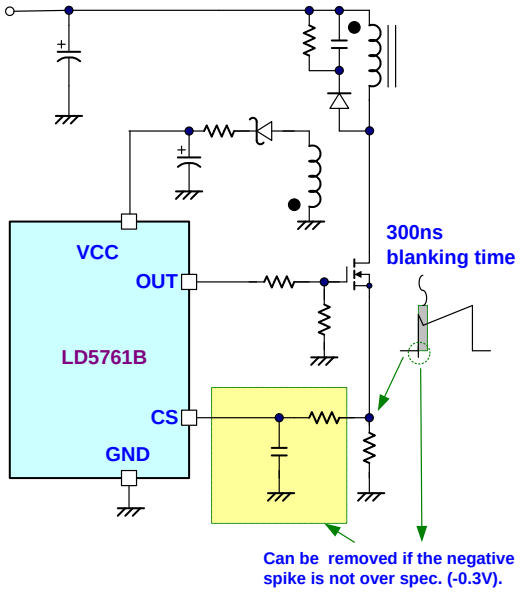


Fig. 14

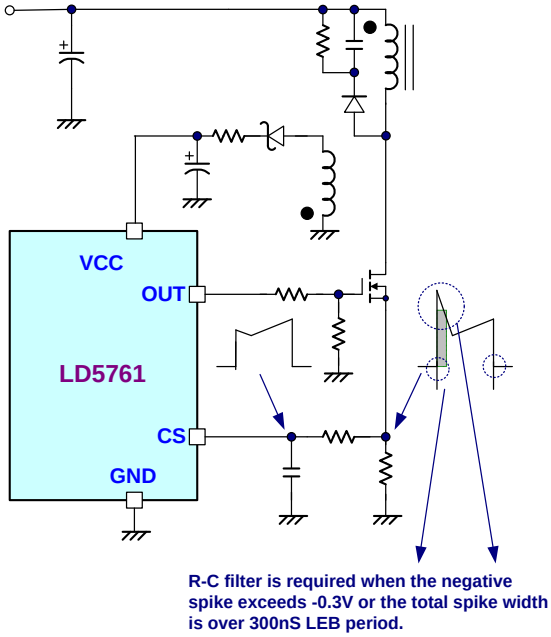


Fig. 15

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer with typical 300mA driving capability is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD5761 is limited to 85% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 on the secondary side through the photo-coupler to the COMP pin of LD5761. Similar to UC384X, its input stage is with a diode voltage offset to feed the voltage divider with 1/4 ratio, that is,

$$V_{CS} = \frac{1}{4} \times (V_{COMP} - V_F)$$

A pull-high resistor is embedded internally to optimize the external circuit.

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is operated for more than 50%. To stabilize the control loop, the slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. LD5761 has internal slope compensation circuit to simplify the external circuit design.

Oscillator and Switching Frequency

The LD5761 has two levels of operation frequency, 65kHz for high line and 100kHz for low line. With this design, it can solve B_{MAX} issue and achieves better efficiency easily.

Dual-Oscillator Green-Mode Operation

There are many different topologies has been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”,

"skipping-cycle mode", "variable off-time control "…etc. The basic operation theory of all these approaches intended to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reduce the switching frequency.

By using LD proprietary dual-oscillator technique, the green-mode frequency can be well controlled and further to avoid the generation of audible noise.

Frequency Swapping

The LD5761 is built in with frequency swapping function, which makes it easy for the power supply designers to optimize EMI performance and system cost. The frequency swapping is internally set for ±8%.

On/Off Control

Pulling COMP pin below V_{ZDC} will immediately disable the gate output of LD5761. Remove the pull-low signal to reset it.

Over Load Protection (OLP)- Latch Mode

To protect the circuit from being damaged at over-load condition and short or open loop condition, the LD5761 is implemented with smart OLP function. LD5761 features latch mode function, see Fig. 16 for the waveform. In the example of fault condition, the feedback system will force the voltage loop enter toward the saturation and then pull the voltage high on COMP pin (V_{COMP}). When the V_{COMP} ramps up to the OLP tripped level (4.7V) and stays for more than the OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit. The OLP delay time is set by internal high frequency counter. It is to prevent the false triggering from the turn-on and turn-off transient.

Turn off AC power to let VCC fall below PDR level to release over load protection. And then restart the power to resume the operation. The de-latch level is defined by internal PDR. See Fig. 16 for its operation.

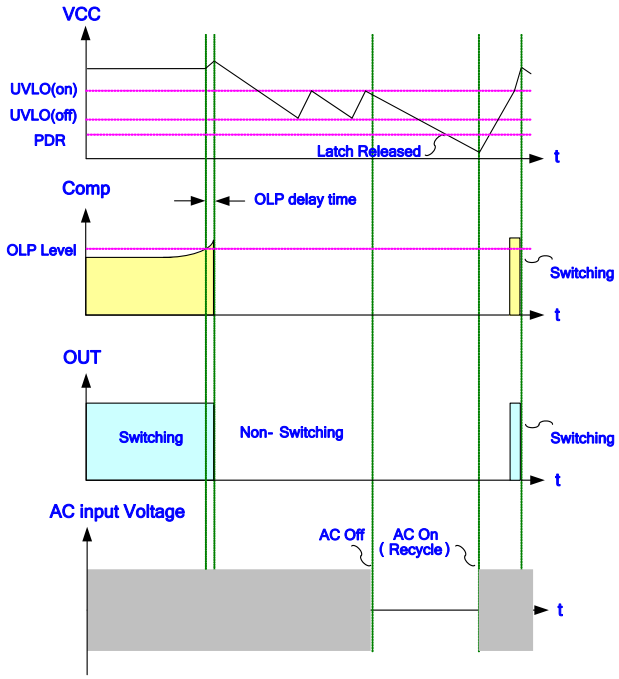


Fig. 16

OVP (Over Voltage Protection) on VCC – Latch Mode

The V_{GS} ratings of the nowadays power MOSFETs are mostly with 30.5V maximum. To protect the V_{GS} from the fault condition, LD5761 is implemented with OVP function on VCC. As the VCC voltage is larger than the OVP threshold voltage, it will shut off the output gate drive circuit simultaneously and stop switching the power MOSFET.

The VCC OVP is latch-off type of protection. Once the VCC trips OVP level (which is usually caused by the feedback loop opened), it will be latched off. Turn off AC power to let VCC fall below PDR level to release overvoltage protection. And then restart the power to resume the operation. The de-latch level is defined by internal PDR. See Fig. 17 for its operation.

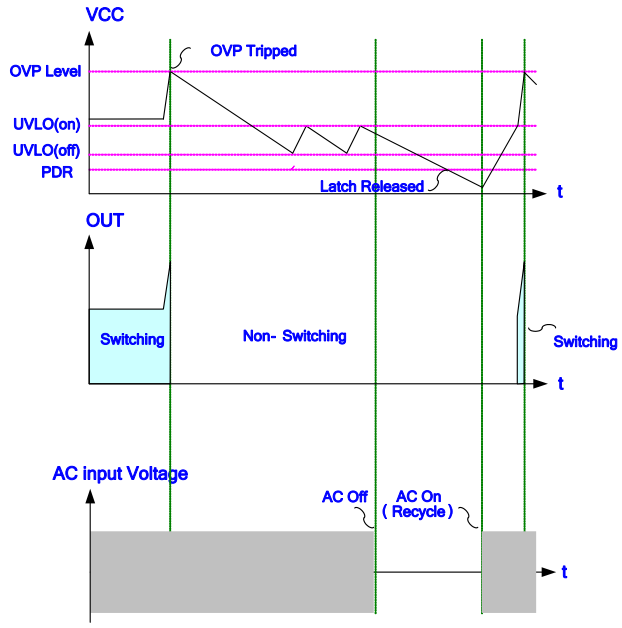


Fig. 17

On-Chip OTP - Auto Recovery

An internal OTP circuit is embedded inside the LD5761 to provide the worst-case protection for this controller. When the chip temperature rises higher than the trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window.

External OTP - Latched Mode Protection

The OTP circuit is implemented to sense whether there is any hot-spot of power circuit like power MOSFET or output rectifier. Typically, a NTC is recommended to connect with OTP pin. The NTC resistance will decrease as the device or ambient in high temperature. The relationship is described as below.

$$V_{OTP} = 100\mu A \cdot R_{NTC}$$

When V_{OTP} < $V_{OTP-OFF}$ (typical 0.95V), it will trigger the protection to shut down the gate output and latch off the power supply. The controller will remain latched unless the VCC drops below 7V (power down reset) and VCC stays on UVLO condition. Two conditions are required to restart the IC successfully, cool down the circuit so that the NTC resistance increase and raise V_{OTP} above 1.05V. Then, recycle the AC main power. The detailed operation is show in Fig. 18.

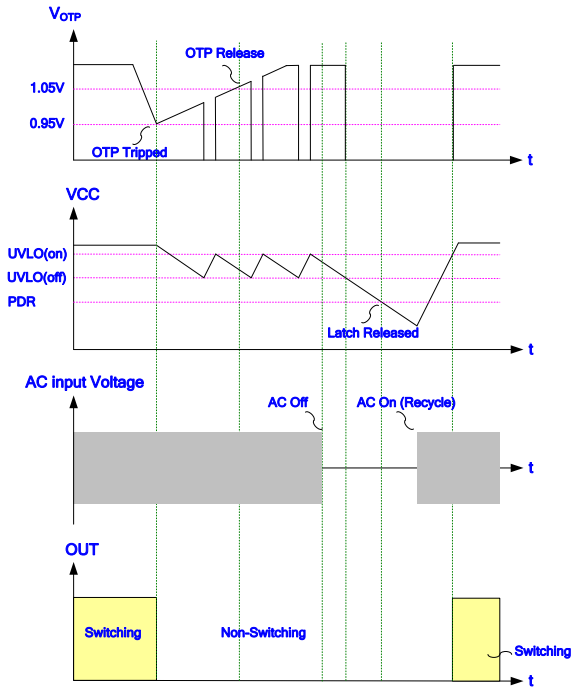


Fig. 18

Pull-Low Resistor on the Gate Pin of MOSFET

The LD5761 consists of an anti-floating resistor at OUT pin to protect the output from damage in abnormally operation or condition due to false triggering of MOSFET. Even so, we still recommend to add an external one at the MOSFET gate terminal to provide more protection in case of disconnection of gate resistor R_G during power-on.

In such single-fault condition, as shown in Fig. 19, the resistor R8 can provide a discharge path to avoid the

MOSFET from being false-triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the MOSFET should be always pulled low and placed in the off-state as the gate resistor is disconnected or opened in any case.

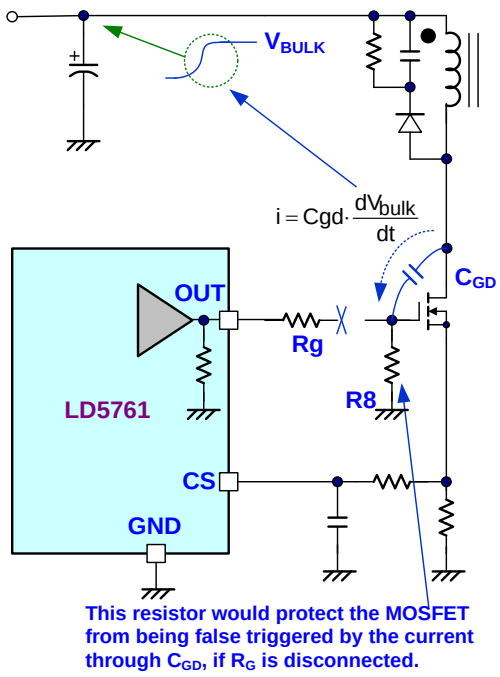


Fig. 19

Protection Resistor on the Hi-V Path

In some other Hi-V process and design, there may be a parasitic SCR caused around HV pin, VCC and GND. As shown in Fig. 20, a small negative spike on the HV pin may trigger this parasitic SCR and cause latch-up between VCC and GND. It may damage the chip because of the equivalent short-circuit induced by such latch-up behavior.

Leadtrend's proprietary of Hi-V technology will eliminate parasitic SCR in LD5761. Fig. 21 shows the equivalent Hi-V structure circuit of LD5761. So that LD5761 is more capable to sustain negative voltage than similar products. However, a 10KΩ resistor is recommended to be placed in the Hi-V path to play as a current limit resistor whenever a negative voltage is applied.

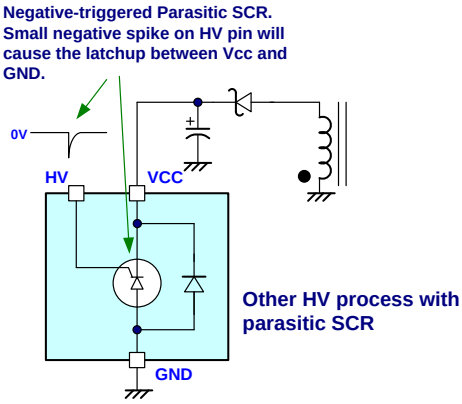


Fig. 20

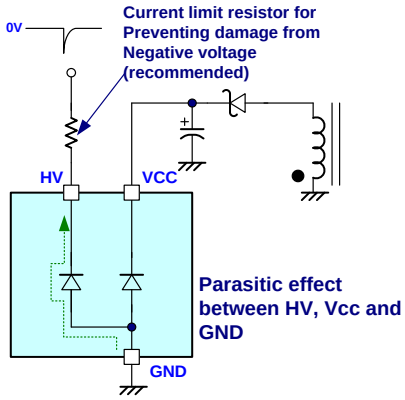
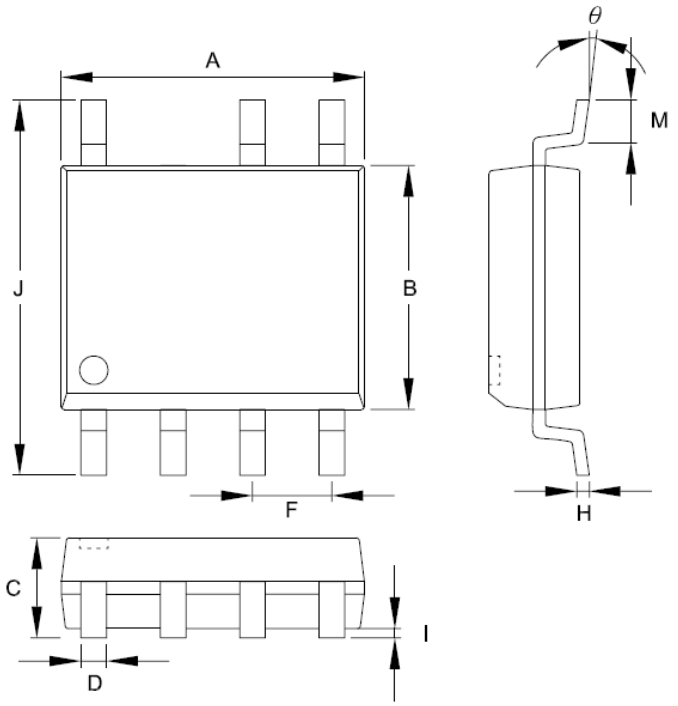


Fig. 21

Package Information

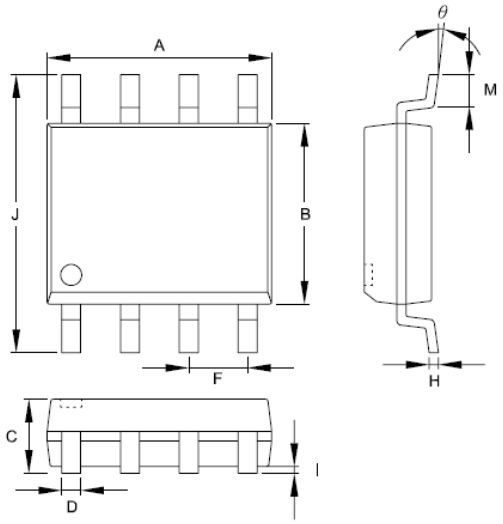
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	04/07/2014	Original Specification.
01	05/28/2015	Modify current limit and add“no-load power consumption <30mW @ 230Vac”. Modify V_{CC-OVP}, $V_{HVBO,}$ $V_{HVBO-HYS}$