High Voltage Green-Mode PWM Controller with BNO Function

REV: 00

General Description

The LD5763M1 is a green mode PWM IC built-in with brown-in/ out functions in a SOP-7 or SOP-8 package. It minimizes the component counts, circuit space, and reduces the overall material cost for the power applications.

The LD5763M1 features HV start, green-mode power-saving operation, and internal slope compensation, soft-start functions to minimize the power loss and enhance the system performance.

With complete protection in it, as OPP (Over Power Protection), OVP (Over Voltage Protection), fast OSCP (Output Short Circuit Protection) and brown-in/out protection, LD5763M1 prevents the circuit from being damaged under abnormal conditions.

Furthermore, the LD5763M1 features frequency swapping and soft driving function to reduce the noise and improve EMI.

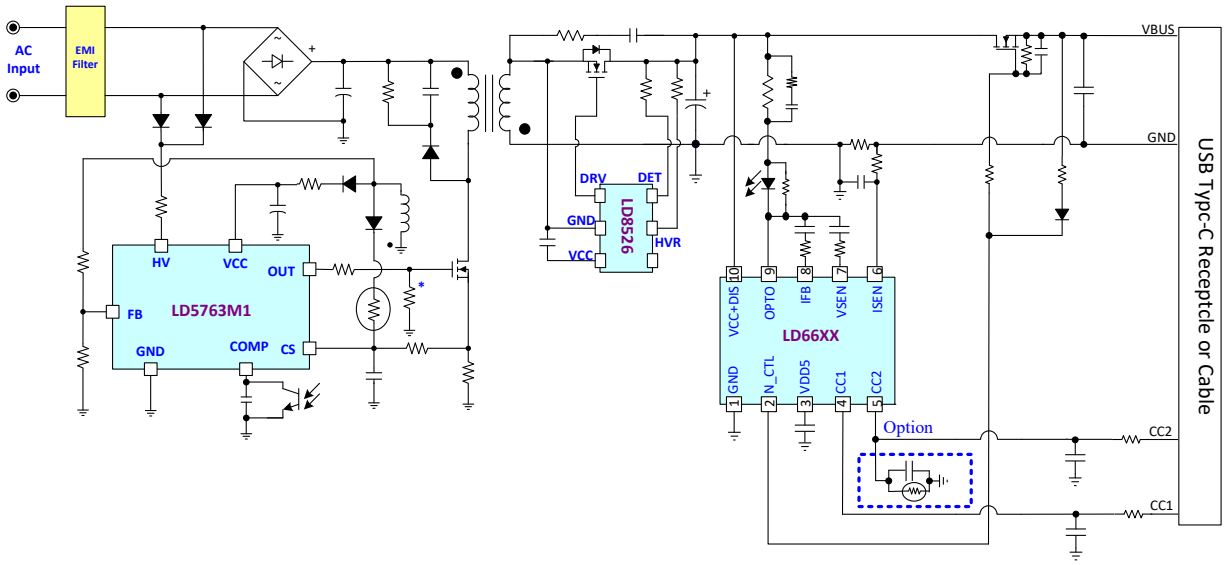
Features

- High-Voltage (700V) Startup Circuit
- Built- in X-Cap Discharge on HV pin
- OVP (Over Voltage Protection) on VCC
- OCP/OPP/OSCP Protections
- Smart stabilization system and high efficiency for USB-PD App
- Adj. CS_OTP (Over Temperature Protection)
- +250mA/-500mA Driving Capability

Applications

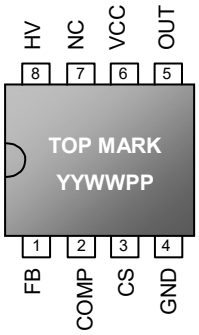
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

Typical Application



Pin Configuration

SOP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package	Top Mark	Shipping
LD5763M1 GS	SOP-8	LD5763M1GS	2500 /tape & reel

The LD5763M1 is ROHS compliant/green packaged.

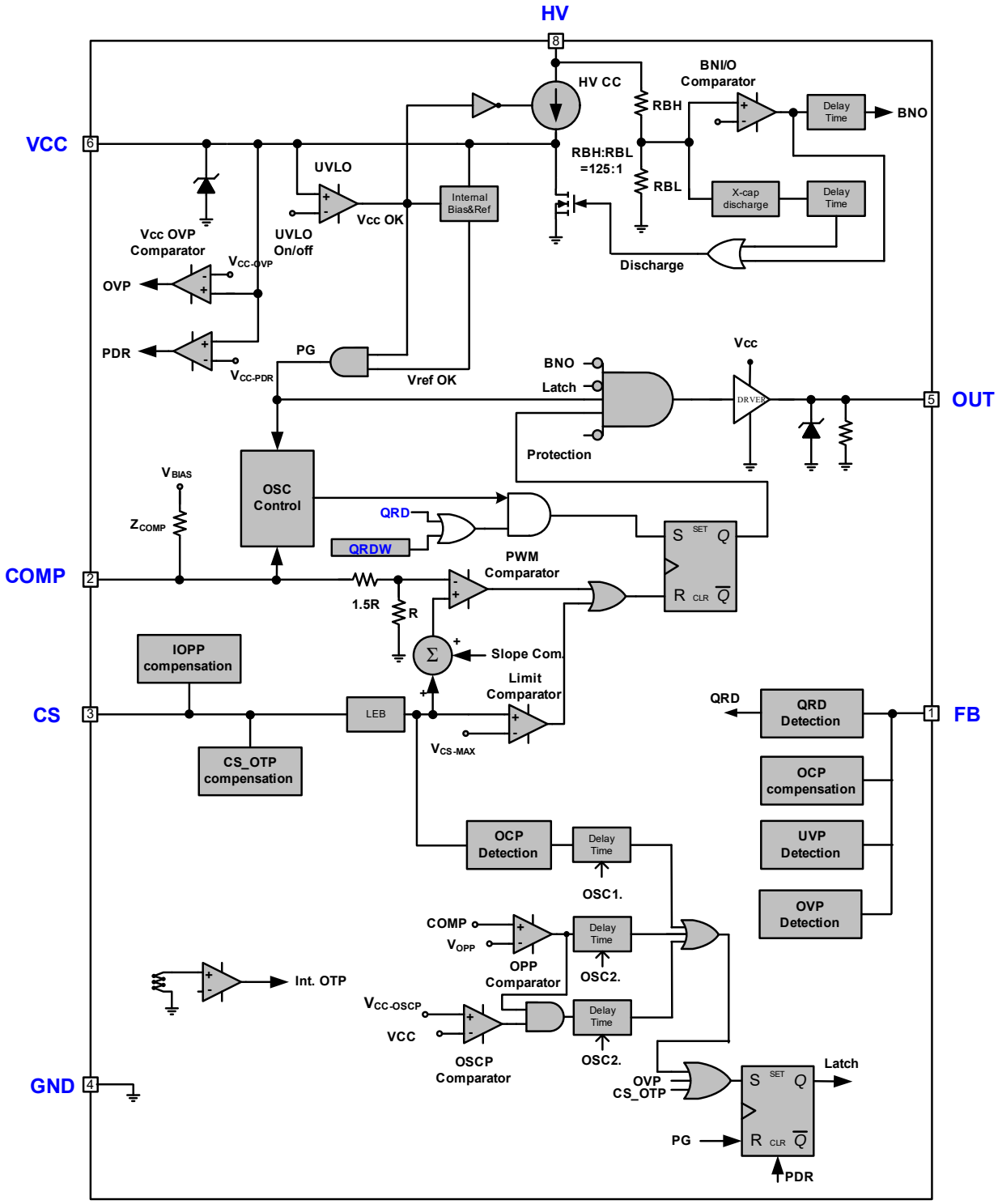
Protection Mode

Part number	VCC_OVP	OSCP	OPP	OCP	CS_OTP
LD5763M1	Latch	Auto-Restart	Auto-Restart	Auto-Restart	Latch

Pin Descriptions

PIN	NAME	FUNCTION
1	FB	Auxiliary voltage sense, output voltage protection and quasi resonant detection.
2	COMP	Voltage feedback pin. Connect a photo-coupler with it to close the control loop and achieve the regulation.
3	CS	Current sense pin, connect it to sense the MOSFET current
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Supply voltage pin
7	NC	Unconnected Pin
8	HV	Connect this pin to Line/ Neutral of AC main voltage through a resistor to provide the startup current for the controller. If VCC voltage increase to trip the point of UVLO(on), this HV loop will be turned off to reduce the power loss on the startup circuit. An internal resistor divider between HV to GND pin will monitor AC line voltage to activate Brown-in/out function.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V ~ 80V
HV	-0.3V ~ 700V
COMP, FB, CS	-0.3V ~ 6V
OUT	-0.3V ~ 20V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOP-8, θ_{JA})	160°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV Pin)	2.5KV
ESD Voltage Protection, Machine Model (except HV Pin)	250V
ESD Voltage Protection, Human Body Model (HV Pin)	1KV
ESD Voltage Protection, Machine Model (HV pin)	200V
Gate Output Current	+250mA/-500mA

Caution:

Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stress above recommended operating conditions may affect device reliability.

Note1: When COMP/CS/FB/OUT pin voltage <-0.3V~-0.7V, the time must be < 100ns.
(The state of note 1 simply happens when user's system is designed according to the application information.)

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	10.5	55	V
HV resistor Value (AC Side)	20	110	KΩ
HV to GND Capacitor Value	--	300	pF
COMP Pin Capacitor	1	10	nF
CS Pin Capacitor Value	47	390	pF

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)						
High-Voltage Current Source	VCC< $UVLO_{(ON)}$, HV=500V	I_{HV}	2.5	3	3.5	mA
HV Discharge capability	HV=500V	I_{HV_DIS}	1.0	1.5	3.6	mA
HV Pin Brown-In Level	HV pin =half rectifier wave increase	V_{HVBI}	101	110	119	V_{DC}
HV Pin Brown-out Level	HV pin = half rectifier wave decrease	V_{HVBO}	91	100	109	V_{DC}
HV Pin BNO Hysteresis	HV_{BI}-HV_{BO}	ΔV_{HV}	5		20	V_{DC}
Brown-in De-bounce Time	*V_{COMP}=3V	T_{D_HVBI}		150		μs
Brown-out Detection Delay time	V_{COMP}=3V	T_{D_HVBO}	59	68	77	ms
HV Pin Min. Operation Voltage	VCC=15V (DetVmin = VHV-Vcc = 30V)	V_{HV_MIN}			45	V
X-Cap discharge Detection Delay time	V_{COMP}=3V	T_{D_XCAP}	59	68	77	ms
Supply Voltage (VCC Pin)						
Startup Current	HV=500V	I_{CC_ST}		25	60	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=3V	I_{CC_OP1}		2		mA
	V_{COMP}=0V	I_{CC_OP2}		0.37		mA
	Auto recover mode	I_{CC_OPA}		0.32		mA
	Latch mode	I_{CC_OPL}		0.32		mA
UVLO(OFF)		V_{CC_OFF}	7.5	8.5	9.5	V
UVLO(ON)		V_{CC_ON}	15.1	16	16.9	V
Holding Voltage		V_{HD}	8.5	9.5	10.5	V
PDR		V_{CC_PDR}	6.1	6.8	7.5	V
VCC HVBI Level	HV>HVBI (Fig 1.)	V_{CC_HVBI}		$UVLO_{OFF}$ +4V		V
VCC OVP Level		V_{CC_OVP}	66		71	V
Oscillator for Switching Frequency						
Frequency	Vac<180V	F_{SWL}	92	100	108	KHz
	Vac>190V	F_{SWH}	55.2	60	64.8	KHz
Green Mode Frequency	With fsw swapping	F_{SW_GREEN}	22	25	28	KHz

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency						
Trembling Frequency	Frequency= 25KHz	F_{TRM1}		4		KHz
	Frequency= 100KHz	F_{TRM2}		14		KHz
F_{SW} Temp. Stability	-40°C ~105°C	F_{SW_TS}	0	3	4	%
F_{SW} Voltage Stability	VCC=8V-(OVP-1V)	F_{SW_VS}	0		1	%
Maximum On Time		DMAX	79	81	83	%
CS_OTP (Over Temperature Protection Protection)						
OTP Trip Current Level	VFB=4V, Vo=20V	V_{CSOTP4}	0.845	0.87	0.895	V
OTP Sample Delay Time	*	$T_{D\_SAMPLE1}$		2.7		μs
Current Sensing (CS Pin)						
Limit Voltage		V_{CS_MAX1}	0.795	0.82	0.845	V
CS OCP Level	VFB=1V	V_{CS_OCP}	0.609	0.63	0.68	V
OPP Compensation Current	Duty≤50%	I_{OPP_50}		0		μA
	Duty≤20%	I_{OPP_20}	400	450	500	μA
IOPP Threshold VCOMP	*Duty≤20%	V_{IOPP}		1.8		V
OCP Delay Time		T_{D_OCP}	360	400	440	ms
Leading Edge Blanking Time		T_{LEB}	460	520	580	ns
Delay to Output		T_{PD}		70		ns
Slope Compensation Level	*0%-D_{MAX} Linearly	V_{SLOPE}		300		mV
Voltage Feedback (Comp Pin)						
Input Voltage to Current-Sense Attenuation	*	A_V		1/2.5		V/V
Short Circuit Current	VFB=1V	I_{COMP}	0.107	0.136	0.145	mA
Open Loop Voltage	*	V_{COMP_OPEN}	3.1	3.2	3.35	V
Zero Duty Threshold VCOMP	VFB=4V	V_{ZDC_4}		0.25		V
Zero Duty Hysteresis	VFB=4V	V_{ZDCH_4}		50		mV

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Gate Drive Output (OUT Pin)						
Output Low Level	VCC=15V, Io=20mA	V_{OL}	0		1	V
Output High Level	VCC=15V, Io=20mA	V_{OH}	8		15	V
Rising Time	*Load Capacitance= 1000pF	T_r		250		ns
Falling Time	*Load Capacitance= 1000pF	T_f		40		ns
OUT Pin Clamping Voltage	*VCC=21V, 1nF on OUT pin	V_{O_CLAMP}		10		V
OPP (Over Power Protection)						
OPP Trip Level		V_{COMP_OPP}		2.6		V
OPP Delay Time	Exclude soft start time	T_{D_OPP}		40		ms
Soft Start						
Soft Start Duration(1)	*After OPP, OCP, BNO, OVP is tripped	T_{SS1}	5	6	7	ms
Soft Start Duration(2)	*Fsw=100kHz	T_{SS2}	30			ms
Internal OTP						
OTP Tripped Level(T_{OTP})	*	T_{INOTP}		140		°C
OTP Hysteresis	*	T_{INOTP_HYS}		T_{OTP}-30		°C
QRD (Quasi Resonant Detection, FB Pin)						
QRD Trip Level	*	V_{QRD}		20		μA
QRD Delay Time	*	T_{QRD}		100		ns
QRD Window Time		T_{D_QRDWD}		3		μs
OVP Trip voltage Level		V_{FB_OVP}	4.09	4.2	4.3	V
De-bounce Cycle		T_{D_FBOVP}		8		Cycle

*: Guaranteed by design.

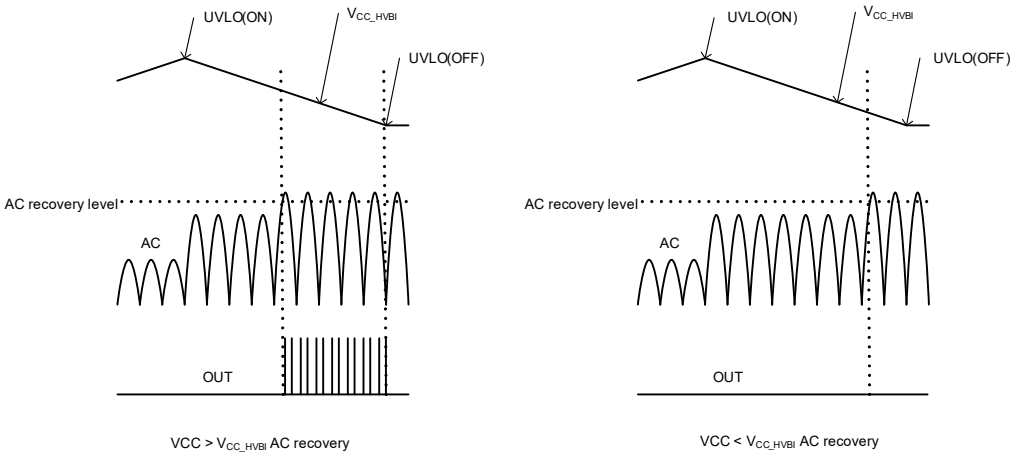


Fig. 1 V_{CC_HVBI} & AC recovery

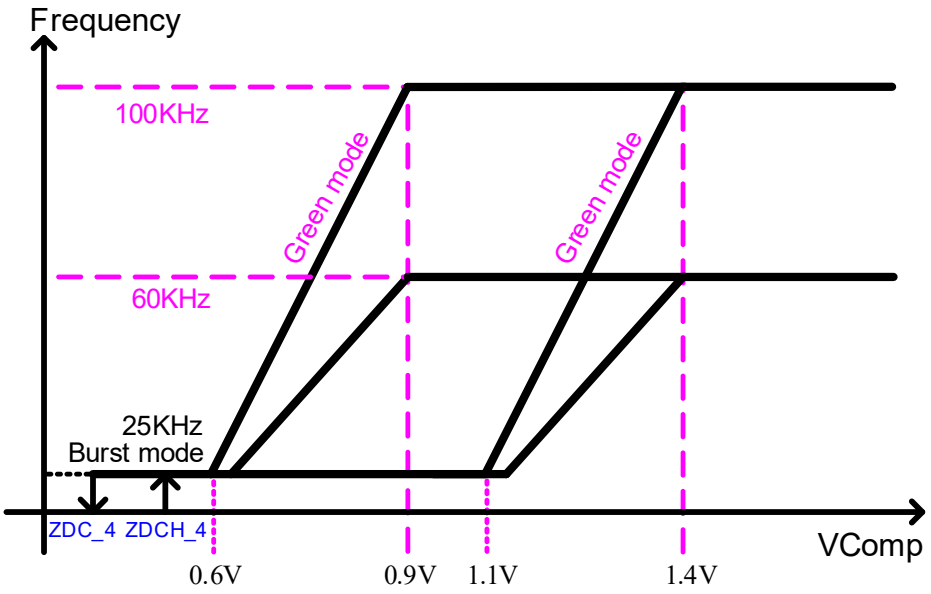


Fig. 2 V_{COMP} vs. PWM Frequency

Typical Performance Characteristics

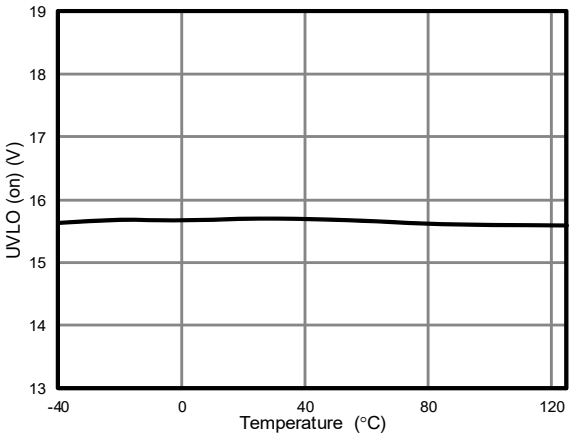


Fig. 3 UVLO (on) vs. Temperature

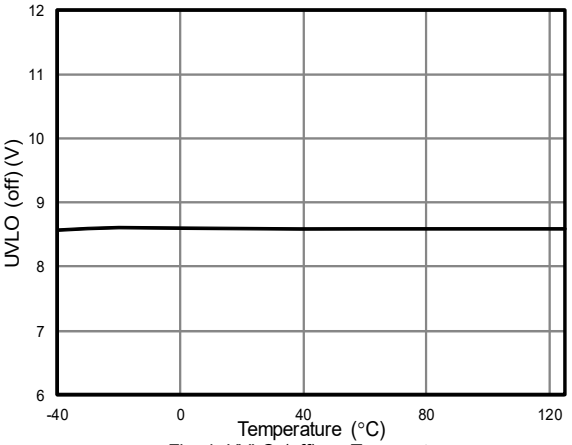


Fig. 4 UVLO (off) vs. Temperature

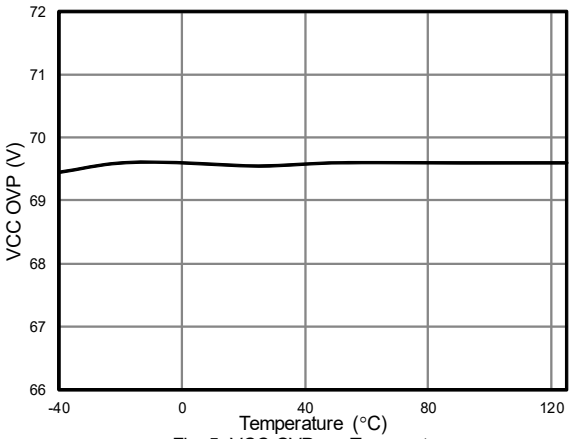


Fig. 5 VCC OVP vs. Temperature

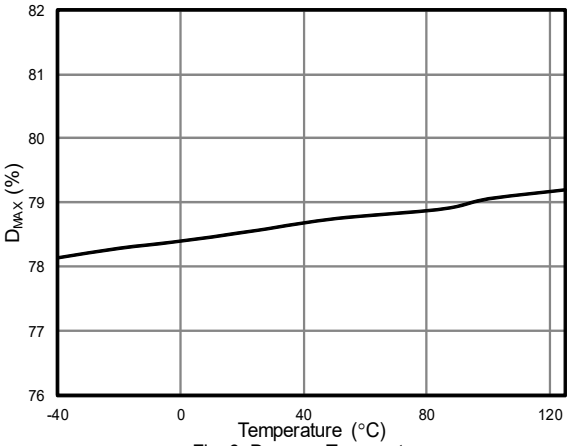


Fig. 6 D_{MAX} vs. Temperature

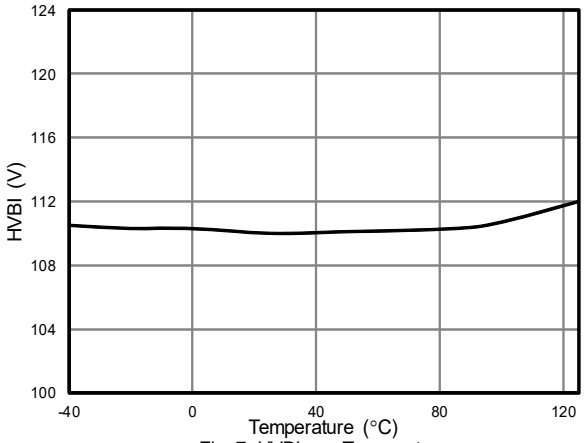


Fig. 7 HVBI vs. Temperature

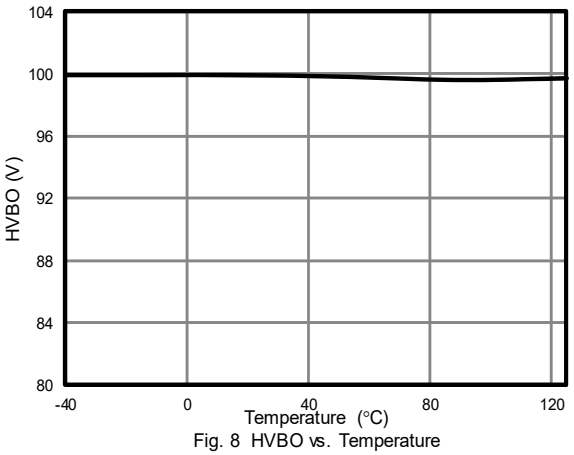


Fig. 8 HVBO vs. Temperature

Application Information

Operation Overview

As long as the requirement for green power becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Due to the cost and size limit, the PWM controller designer is bound to integrate with more functions to reduce the external part counts. The LD5763M1 is ideal for these applications. Its detailed features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes much significant power to meet the current power saving requirement. In most cases, startup resistors carry larger resistance and spend more time to start up.

To achieve the optimized topology, as shown in Fig. 9, LD5763M1 is implemented with a high-voltage startup circuit for such requirement. At startup, the high-voltage current source sinks current of AC line/or neutral to provide startup current and charge the capacitor C1 connected to VCC.

At the startup transient, the HV current will supply around 3mA to VCC capacitor until this VCC voltage reaches the UVLO threshold VCC. By using such configuration, the turn-on delay time will be almost same no matter under low-line or high-line conditions.

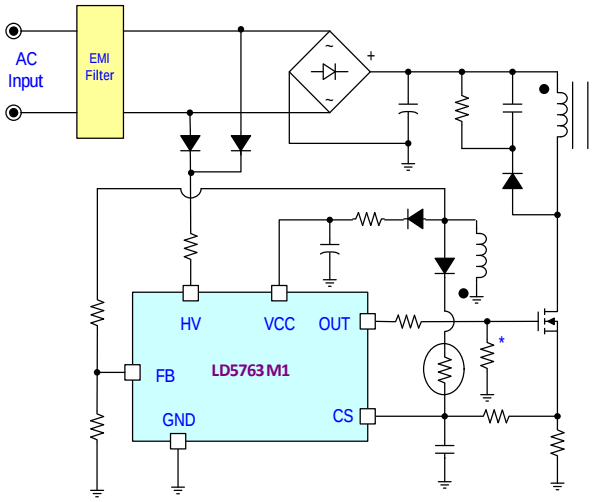


Fig. 9

As VCC trips UVLO(OFF), HV pin will recharge VCC capacitor till VCC voltage rises back to UVLO(ON) again. Since then, HV pin would no longer charge the capacitor and instead, send a gate drive signal to draw supply current for VCC from the auxiliary winding of the transformer. That minimizes the power loss on the start-up circuit successfully.

An UVLO comparator is embedded to detect the voltage across the VCC pin to ensure the supply voltage enough to power on the LD5763M1 and in addition, to drive the power MOSFET. As shown in Fig. 10, a hysteresis is provided to prevent shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16V and 8.5V, respectively.

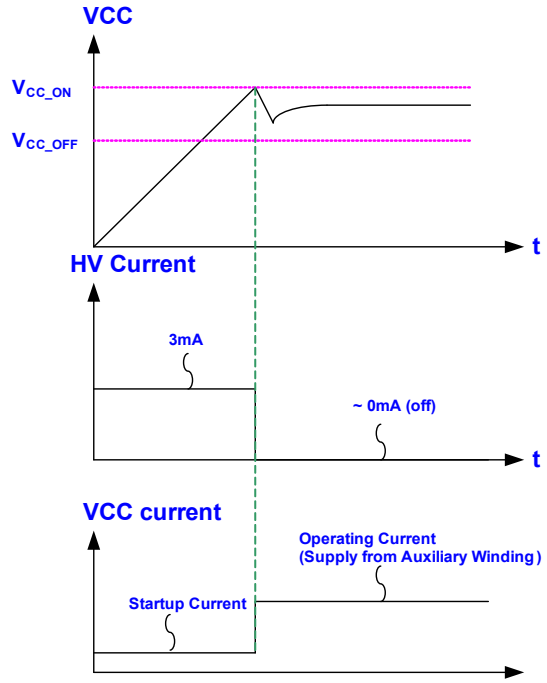


Fig. 10

Brown in/out Protection

The LD5763M1 features burn-in/out function on HV pin. As the built-in comparator detects the half wave rectify line voltage condition, it will shut off the controller to prevent from any damage. Fig. 11 shows the operation. When V_{HV} < HVBO, the gate output will remain off even when the VCC already reaches UVLO(ON). It therefore forces the VCC hiccup between UVLO(ON) and UVLO(OFF). Unless the line voltage rises over HVBI V_{AC}, the gate output will not start switching even as the next UVLO(ON) is tripped. A hysteresis is implemented to prevent the false-triggering during turn-on and turn-off.

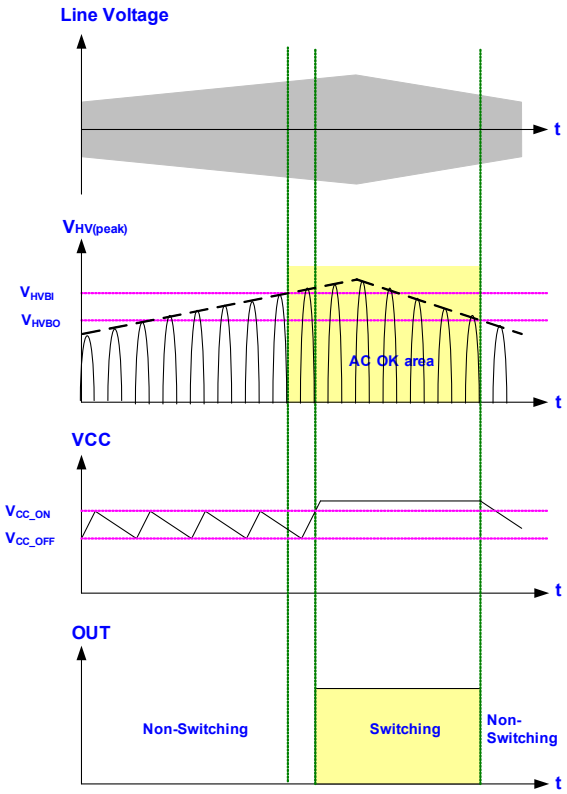


Fig. 11

Current Sensing, Leading-Edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD5763M1 detects the primary MOSFET current across CS pin to control in peak current mode and also limit the pulse-by-pulse current. The maximum voltage threshold of the current sensing pin is set at 0.82V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.82V}{R_S}$$

A 520ns leading-edge blanking (LEB) time is designed in the input of CS pin to prevent false-triggering from the current spike. In the low power applications, if the total pulse width of the turn-on spikes is less than 520ns and the negative spike on the CS pin does not exceed -0.3V, the R-C filter (as shown in Fig. 12) is free to eliminate.

However, the total pulse width of the turn-on spike is related to the output power, circuit design and PCB layout. It is strongly recommended to add a small R-C filter (as shown in Fig. 13) for larger power application to avoid the CS pin from being damaged by the negative turn-on spike.

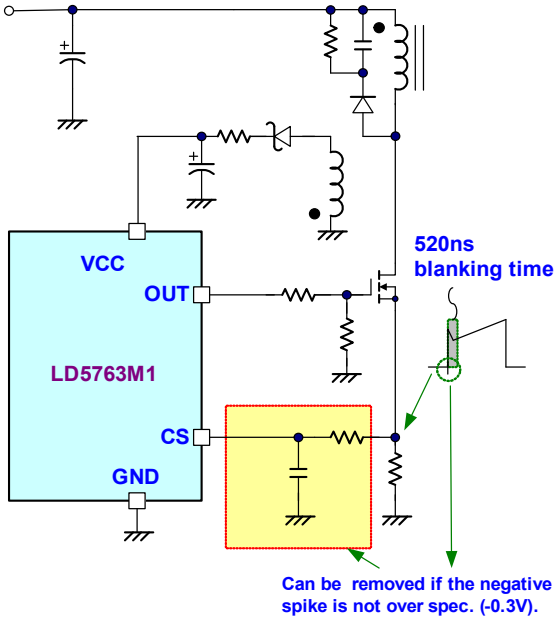


Fig. 12

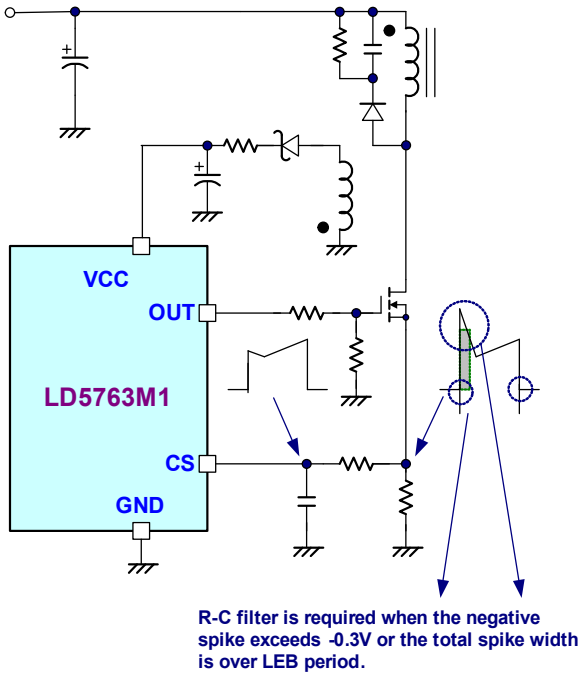


Fig. 13

Output Stage and Maximum Duty-Cycle

A CMOS buffer with output stage of typical 250mA driving capability is incorporated to drive a power MOSFET directly. The maximum duty-cycle of LD5763M1 is limited to 78% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 on the secondary side through the photo-coupler to the COMP pin of LD5763M1. Similar to UC384X, its input stage is with a diode voltage offset to feed the voltage divider with 1/2.5 ratio, that is,

$$V_{CS(PWM_{COMPARATOR})} = \frac{1}{2.5} \times V_{COMP}$$

A pull-high resistor is embedded internally to optimize the external circuit.

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is operated for more than 50%. To stabilize the control loop, the slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. LD5763M1 has internal slope compensation circuit to simplify the external circuit design.

Oscillator and Switching Frequency

The LD5763M1 fixes the switching frequency at 100kHz internally to optimize its performance in EMI, thermal treatment, component sizes and transformer design.

Dual-Oscillator Green-Mode Operation

There are many different topologies has been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intended to reduce the switching cycles under light-load or no-load condition either by skipping

some switching pulses or reduce the switching frequency.

By using LD proprietary dual-oscillator technique, the green-mode frequency can be well controlled and further to avoid the generation of audible noise.

Frequency Swapping

The LD5763M1 is built in with frequency swapping function, which makes it easy for the power supply designers to optimize EMI performance and system cost. The frequency swapping is internally set for ±8%.

On/Off Control

Pulling COMP pin below ZDC will immediately disable the gate output of LD5763M1. Remove the pull-low signal to reset it.

Over Power Protection (OPP) – Auto Recovery

To protect the circuit from being damaged during over load condition and short or open loop condition, the LD5763M1 is implemented with smart OPP function. LD5763M1 features auto recovery function of it, see Fig. 14 for the waveform. In the example of the fault condition, the feedback system will force the voltage loop enter toward the saturation and then pull the voltage high on COMP pin (V_{COMP}). As the V_{COMP} ramps up to the OPP tripped level and stays for more than the OPP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit. The OPP delay time is set by internal high frequency counter. It is to prevent the false triggering from the power-on and turn-off transient.

A divide-2 counter is implemented to reduce the average power under OPP behavior. As soon as OPP is activated, the output will be latched off and the divide-2 counter will start to count the number of UVLO(OFF). The latch will not be released until the 3rd UVLO(OFF) point is counted, after that the output will resume to switch again. With the protection mechanism, the average input power will be minimized, so that the component temperature and stress can be controlled within the safe operating area.

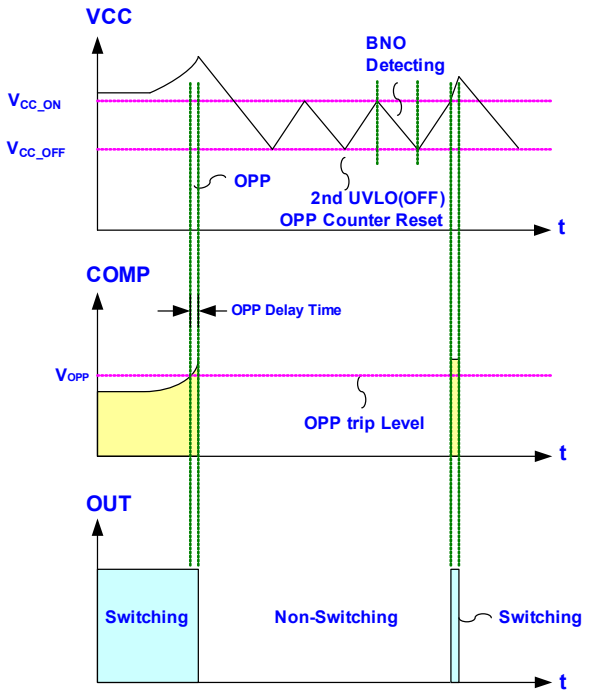


Fig. 14

OVP (Over Voltage Protection) on VCC – Latched Mode

The V_{GS} ratings of the nowadays power MOSFETs are mostly with 30.5V maximum. To protect the V_{GS} from the fault condition, LD5763M1 is implemented with OVP function on VCC. As the VCC voltage is larger than the OVP threshold voltage, it will shut off the output gate drive circuit simultaneously and stop switching the power MOSFET.

The VCC OVP is latch-off type of protection. Once the VCC trips OVP level (which is usually caused by the feedback loop opened), it will be latched off. Turn off AC power to let VCC fall below PDR level to release overvoltage protection. Then, restart the power to resume the operation. The de-latch level is defined by internal PDR. See Fig. 15 for its operation.

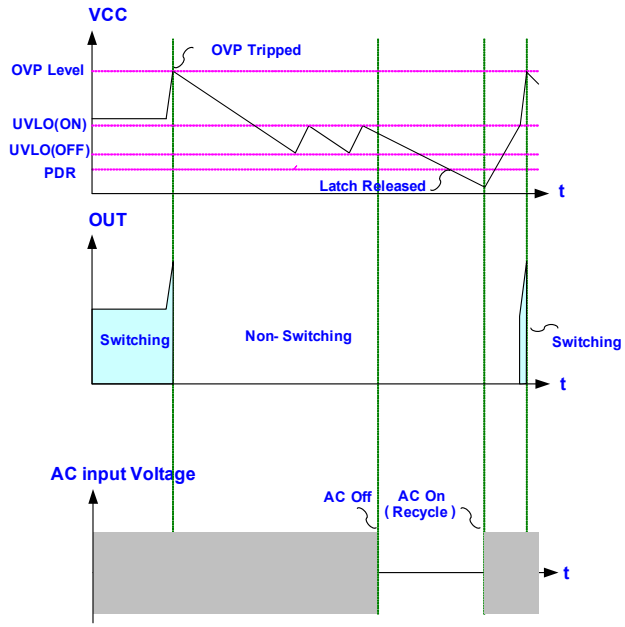


Fig. 15

Adjustable Over Power Compensation on CS Pin

In general, the power converter can deliver more current at high input voltage than the low input voltage. To compensate this, an offset voltage is added to the CS signal by an internal current source (IOPP) and an external resistor (ROPP) in series between the sense resistor (RS) and the CS pin, as shown in Fig. 16. By choosing the value of the resistor in series with the CS pin, the amount of compensation can be adjusted. The value of IOPP depends on the duty cycle of OUT pin. The equation of IOPP is decreased as:

$$I_{OPP} = \begin{cases} 1500uA(0.5 - Duty), & 0.2 < Duty < 0.5 \\ 0\mu A, & Duty \geq 0.5 \\ 450\mu A, & Duty \leq 0.2 \end{cases}$$

Since in light load conditions this offset is in the same order of magnitude as the current sense signal, it must be removed. Therefore the compensation current is only added when the COMP voltage is higher than 1.8V, as shown in Fig. 16.

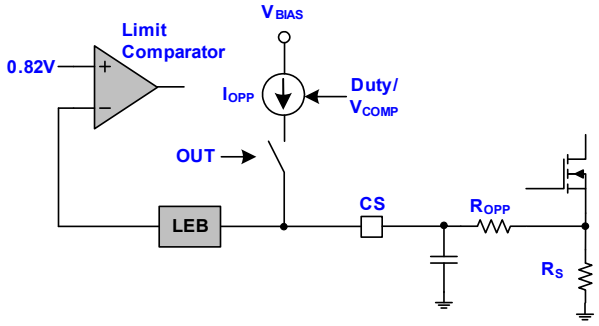


Fig. 16

On-Chip OTP – Auto Recovery

An internal OTP circuit is embedded inside the LD5763M1 to provide the worst-case protection for this controller. When the chip temperature rises higher than the trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window.

Over Voltage Protection on FB Pin (FB_OVP) – Latch Mode

An output overvoltage protection is implemented in the LD5763M1. The auxiliary winding voltage can be reflected from secondary winding, in which the FB pin voltage is proportional to output voltage during the gate off time. OVP is worked by sensing the auxiliary voltage via the divided resistors R2, referring to Fig. 17. The equation of FB OVP is shown as follows.

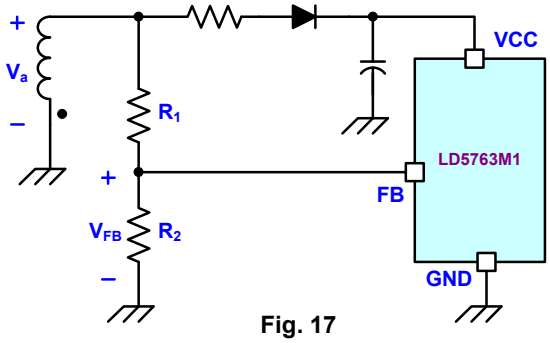


Fig. 17

$$R_2 = \frac{R_1 \cdot V_{FB\_OVP}}{V_a - V_{FB\_OVP}}$$

$$V_a = \frac{N_a}{N_s}(V_O + V_F)$$

V_{FB_OVP} is the FB pin OVP trip voltage level. V_a is the auxiliary winding voltage which reflects from the forward voltage V_F of Schottky diode and output voltage V_O. N_S is turns ration of secondary-side winding.

If V_{FB} overs the FB_OVP trip level, the internal counter starts counting 8 cycles, and then LD5763M1 goes to latch mode.

Over Temperature Protection on CS Pin (CS OTP) - Latch Mode

LD5763M1 is implemented over temperature protection on CS pin which senses voltage to determine NTC status during gate off region. As V_{CS} is greater than 0.85V and continues for 16 cycles, CS_OTP is triggered, than LD5763M1 is in latch mode.

Pull-Low Resistor on the Gate Pin of MOSFET

The LD5763M1 consists of an anti-floating resistor with OUT pin to protect the output from damage in abnormally operation or condition due to false triggering of MOSFET. Even so, we still recommend adding an external one at the MOSFET gate terminal to provide more protection in case of disconnection of gate resistor R_G during power-on.

In such single-fault condition, as shown in Fig. 18, the resistor R8 can provide a discharge path to avoid the MOSFET from being false-triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the MOSFET should be always pulled low and placed in the off-state as the gate resistor is disconnected or opened in any case.

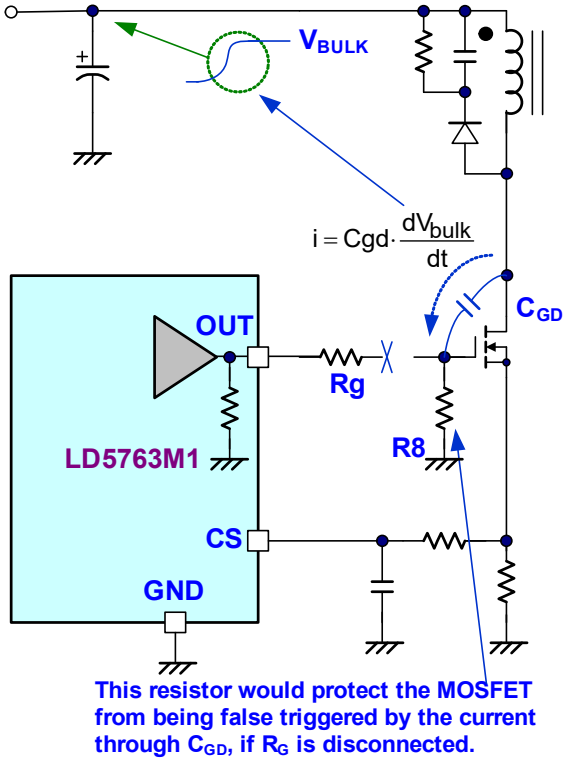


Fig. 18

Protection Resistor on the Hi-V Path

In some other Hi-V process and design, there may be a parasitic SCR caused around HV pin, VCC and GND. As shown in Fig. 19, a small negative spike on the HV pin may trigger this parasitic SCR and cause latch-up between VCC and GND. It may damage the chip because of the equivalent short-circuit induced by such latch-up behavior.

Leadtrend's proprietary of Hi-V technology will eliminate parasitic SCR in LD5763M1. Fig. 20 shows the equivalent Hi-V structure circuit of LD5763M1 so that LD5763M1 is more capable to sustain negative voltage than similar products. However, a 70KΩ resistor is recommended to add in the Hi-V path to play as a current limit resistor as a negative voltage is applied.

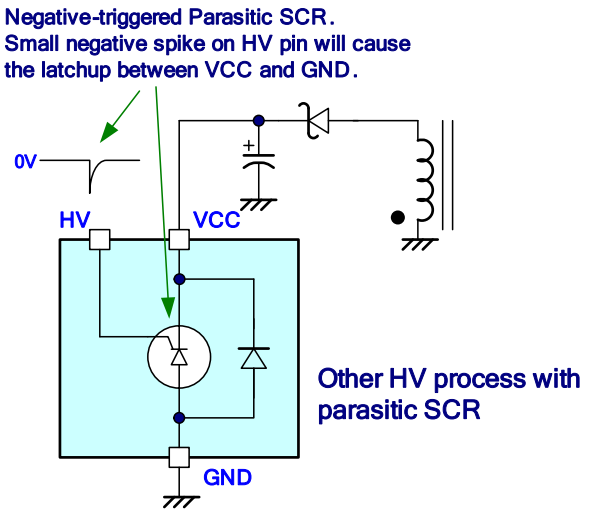


Fig. 19

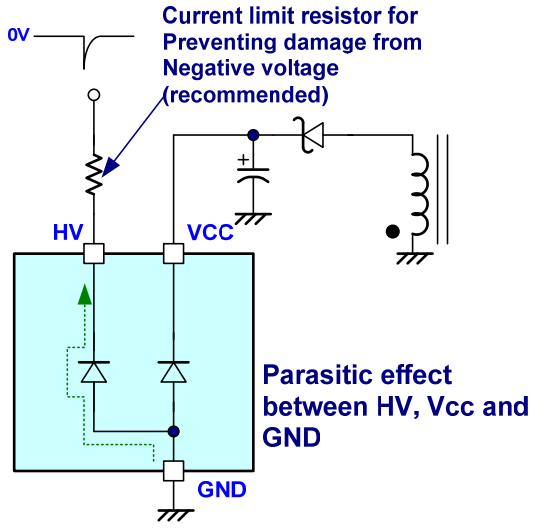


Fig. 20

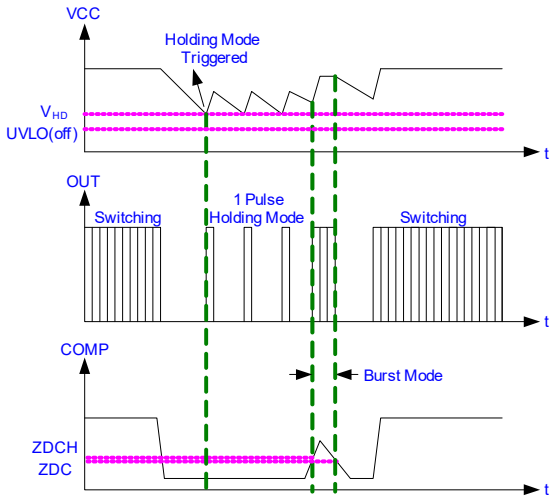


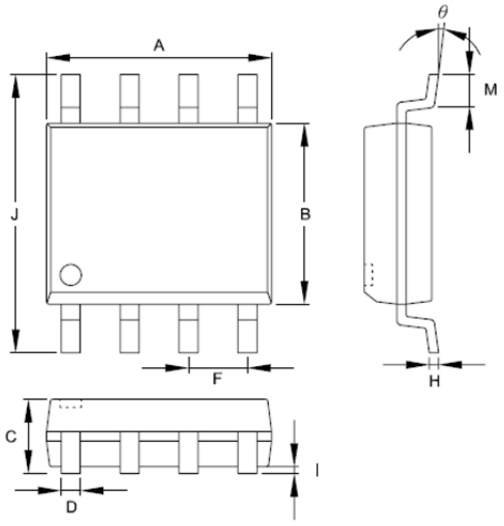
Fig. 21

V_{CC} Holding Mode

When the V_{CC} voltage is lower than the V_{HD} (9.5V, V_{CC} holding mode between 9.5V-10.2V), the gate will be forced to turn on and making V_{CC} voltage rise. V_{CC} holding mode avoids V_{CC} dropping to UVLO(off) in quick feedback system. See Fig. 21 for its operation.

Package Information

SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

REV.	Date	Change Notice
00	06/15/2021	Original Specification