

### DESCRIPTION

The LD6143 video filter driver is intended to replace passive LC filters and drivers with an integrated device. Three fourth-order filters provide improved image quality compared to typical 2nd or 3rd order passive solutions.

The LD6143 may be driven by a DC or an AC-coupled video signal. The outputs can drive AC or DC-coupled single ( 150Ω ) or dual ( 75Ω ) loads.

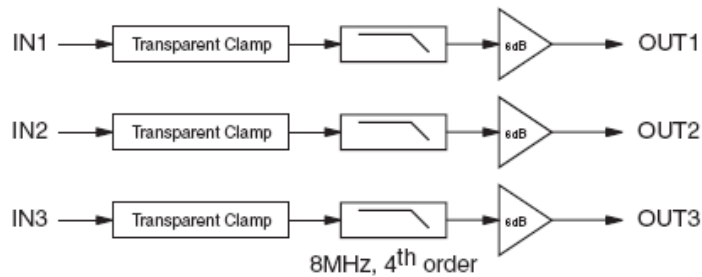
### FEATURE

- Three fourth-order 8MHz Standard Definition ( SD ) video filters
- Transparent input clamping
- Dual video load drive ( 2Vpp, 75Ω )
- AC or DC-coupled inputs
- AC or DC-coupled outputs
- 5V only
- SOIC-8 package

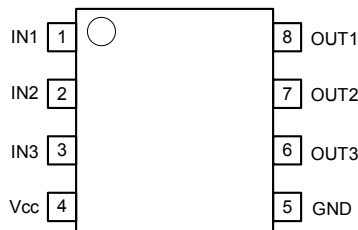
### APPLICATION

Use for the Cable set top boxes, Satellite set top boxes, DVD players, HDTV, Personal video recorders ( PVR ) or Video on demand ( VOD ) .

### FUNCTIONAL BLOCK DIAGRAM



### PIN CONFIGURATION



### PIN DESCRIPTION

PIN #	PIN	Description
1	IN1	Video input, Channel 1
2	IN2	Video input, Channel 2
3	IN3	Video input, Channel 3
4	V <sub>CC</sub>	+5V supply, do not float
5	GND	Ground, do not float
6	OUT3	Filtered output, Channel 3
7	OUT2	Filtered output, Channel 2
8	OUT1	Filtered output, Channel 1

### ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	$V_{CC}$	- 0.3	6	V
Analog and Digital input / output	I/O	- 0.3	$V_{CC} + 0.3$	V
Output Current ( Any One Channel )	$I_O$	--	50	mA
Storage Temperature	$T_S$	- 55	150	
Junction Temperature	$T_J$	--	150	
Lead Temperature ( Soldering, 10s )		--	300	

### RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage Range	$V_{CC}$	4.75	5.0	5.25	V
Video Input Voltage Range ( Referenced to GND if DC-coupled )	$V_{IN}$	--	1.4	--	$V_{PP}$
Operating Temperature Range	$T_A$	0	25	70	

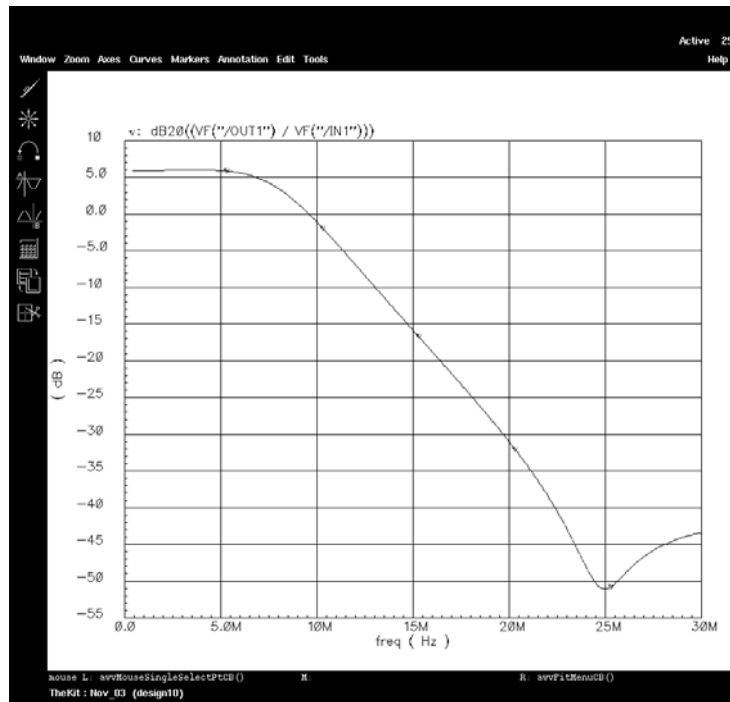
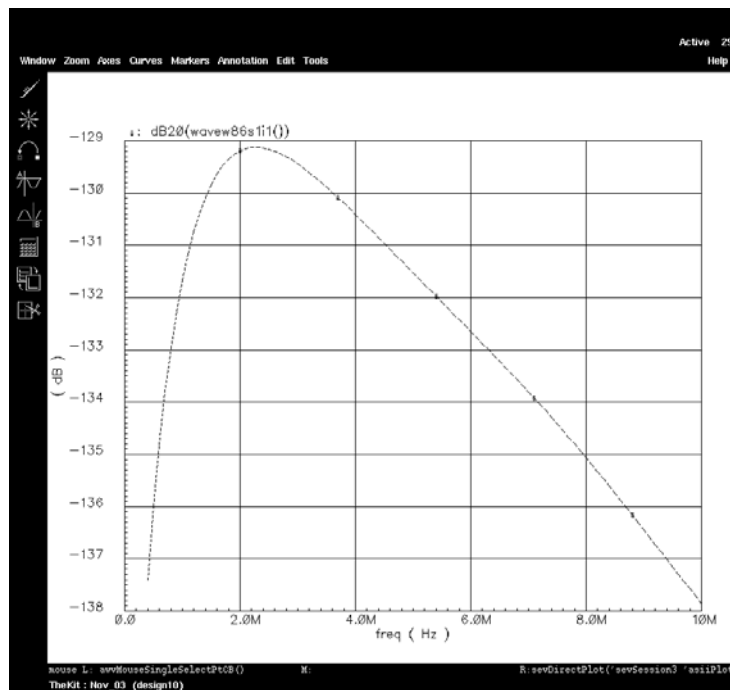
### ELECTRICAL CHARACTERISTIC

$V_{CC} = 5.0V$ ,  $V_{IN} = 1V_{pp}$ ,  $R_{source} = 37.5\Omega$ , all inputs AC coupled with  $0.1\mu F$ , all outputs AC coupled with  $220\mu F$  into  $150\Omega$  load,  $T_A = 0 \sim 70$  ; unless otherwise noted

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Current	$I_{CC}$	no input signal, no load	--	--	27	mA
Power Supply Rejection Ratio	PSRR	DC, All Channels	--	--	-40	dB
Channel Gain	AV	All Channels	5.5	6.0	6.6	dB
-1dB Bandwidth	$f_{1dB}$	All Channels	4.5	7.0	9.0	MHz
-3dB Bandwidth	$f_C$	All Channels	5.5	8.0	10.0	MHz
Stopband Attenuation	$f_{SB}$	All Channels, $f = 27MHz$	35	40	--	dB
Differential Gain	dG	All Channels	--	--	1.0	%
Differential Phase	d $\Phi$	All Channels	--	--	1.0	°
Output Distortion	THD	All Channels, $V_{OUT} = 1.8V_{PP}$ , 1MHz	--	0.4	0.9	%
Crosstalk	$X_{TALK}$	Channel-to-Channel, at 1MHz	--	--	-50	dB
Signal-to-Noise Ratio	SNR	All Channels, NTC-7 Weighting: 100kHz to 4.2MHz	55	--	--	dB
Propagation Delay	$t_{pd}$	Input-to-Output, 4.5MHz	--	--	100	ns

**TYPICAL PERFORMANCE CHARACTERISTIC**

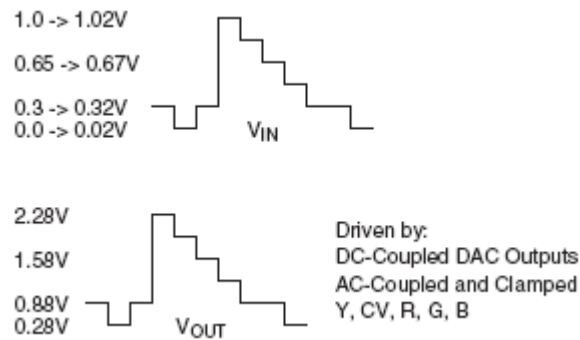
$V_{CC} = 5.0V$ ,  $V_{IN} = 1V_{pp}$ ,  $R_{source} = 37.5\Omega$ , all inputs AC coupled with  $0.1\mu F$ , all outputs AC coupled with  $220\mu F$  into  $150\Omega$  load,  $T_A = 25^\circ C$ ; unless otherwise noted


**Frequency Response**

**Noise vs. Frequency**

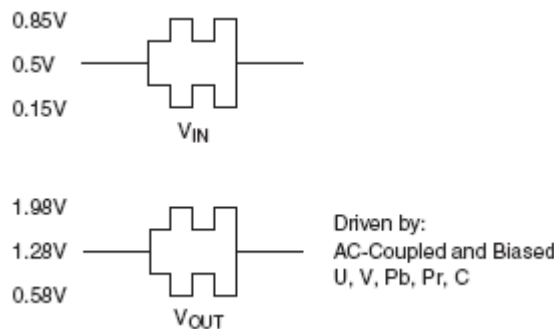
### APPLICATION INFORMATION

#### Application Circuit

The LD6143 Video Filter provides 6dB gain from input to output. In addition, the input will be slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in the Figure 1.



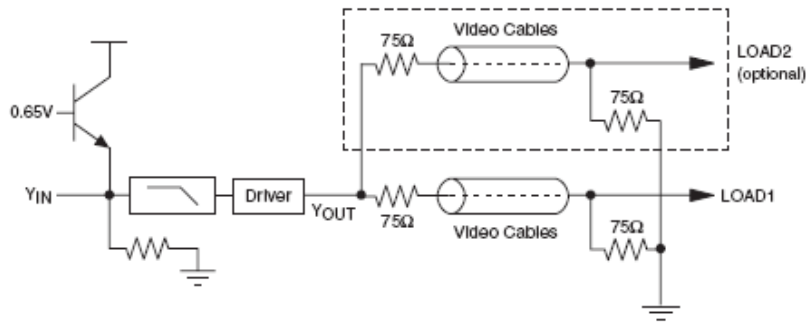
There will be a 280mV offset from the DC input level to the DC output level.  $V_{OUT} = 2V_{IN} + 280mV$



**Figure 1. Typical voltage level**

The LD6143 provides an internal diode clamp to support AC coupled input signals. If the input signal does not go below ground, the input clamp will not operate. This allows DAC outputs to directly drive the LD6143 without an AC coupling capacitor. When the input is AC-coupled, the diode clamp will set the sync tip (or lowest voltage) just below ground. The worstcase sync tip compression due to the clamp will not exceed 7mV. The input level set by the clamp combined with the internal DC offset will keep the output within its acceptable range.

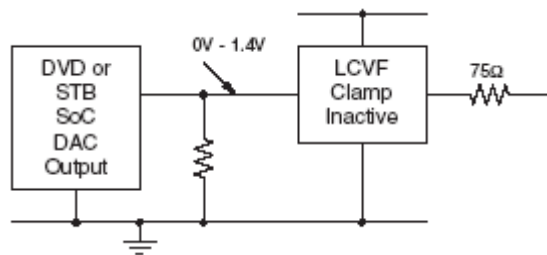
For symmetric signals like Chroma, U, V, Pb and Pr, the average DC bias is fairly constant and the inputs can be AC-coupled with the addition of a pull-up resistor to set the DC input voltage. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown Figure 2.



**Figure 2. Input clamp circuit**

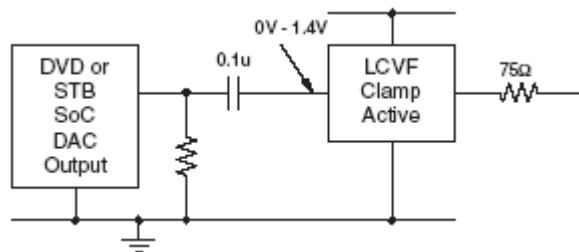
### I/O Configuration

For DC-coupled DAC drive with DC-coupled outputs, use this Figure 3 configuration.



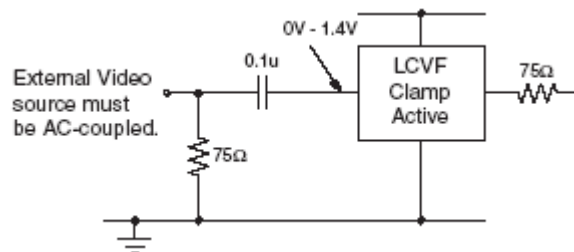
**Figure 3. DC-coupled input and output**

Alternatively, if the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC-coupled as follows Figure 4.



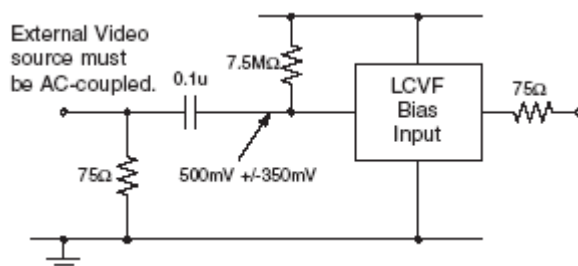
**Figure 4. AC-coupled input, DC-coupled output**

When the LD6143 is driven by an unknown external source or a SCART switch with its own clamping circuitry the inputs should be AC-coupled like this Figure 5.



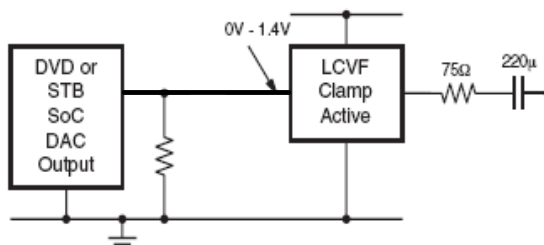
**Figure 5. SCART with DC-coupled output**

The same method can be used for biased signals with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is  $800k\Omega \pm 20\%$  so the external resistance should be  $7.5M\Omega$  to set the DC level to  $500mV$ , as follows Figure 6.

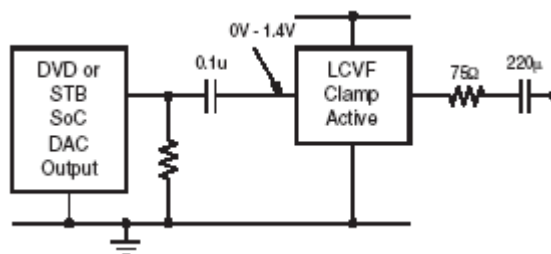


**Figure 6. Biased SCART with DC-coupled output**

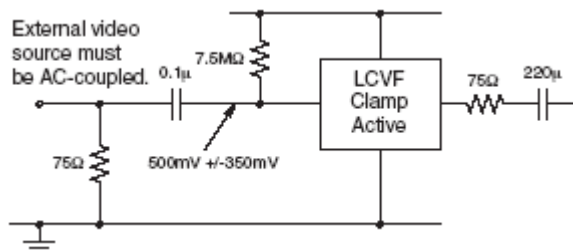
The same circuits can be used with AC-coupled outputs if desired. As follows Figure 7, Figure 8 and Figure 9.



**Figure 7. DC-coupled inputs, AC-coupled output**



**Figure 8. AC-coupled input and output**



**Figure 9. Biased SCART with AC-coupled output**

NOTE: The video tilt or line time distortion will be dominated by the AC-coupling capacitor. The value may need to be increased beyond  $220\mu F$  in order to obtain satisfactory operation in some applications.

### Power Dissipation

The LD6143 output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the LD6143's power dissipation and internal temperature rise.

$$T_J = T_A + P_d \times \theta_{JA}$$

where:  $T_A$  = Environment Temperature,  $\theta_{JA}$  = Thermal Resistance

$$P_d = P_{CH1} + P_{CH2} + P_{CH3} \text{ and } P_{CHX} = V_{CC} \times I_{CH} - (V_{OUT}^2 / R_L)$$

where:  $V_{OUT} = 2V_{IN} + 0.280V$

$$I_{CH} = (I_{CC} / 3) + (V_{OUT} / R_L)$$

$V_{IN}$  = RMS value of input signal

$I_{CC}$  = Supply Current

$V_{CC}$  = Supply Voltage

$R_L$  = Channel load resistance

Board layout can also affect thermal characteristics. Refer to the Layout Considerations section for more information.

The LD6143 is specified to operate with output currents typically less than 50mA, more than sufficient for a dual (75Ω) video load. Internal amplifiers are current limited to a maximum of 100mA and should withstand brief duration short circuit conditions, however this capability is not guaranteed.

### Layout Consideration

General layout and supply bypassing play major roles in high frequency performance and thermal characteristics. Following this layout configuration will provide the optimum performance and thermal characteristics. For optimum results, follow the steps below as a basis for high frequency layout:

- Include 1μF and 0.1μF ceramic bypass capacitors
- Place the 1μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- For multi-layer boards, use a large ground plane to help dissipate heat
- For 2 layer boards, use a ground plane that extends beyond the device by at least 0.5"
- Minimize all trace lengths to reduce series inductances

### TYPICAL APPLICATION

As follows Figure 10, circuit may be used for direct DC-coupled drive by DACs with an output voltage range of 0V to 1.4V. AC-coupled or DC-coupled outputs may be used with AC-coupled outputs offering slightly lower power dissipation.

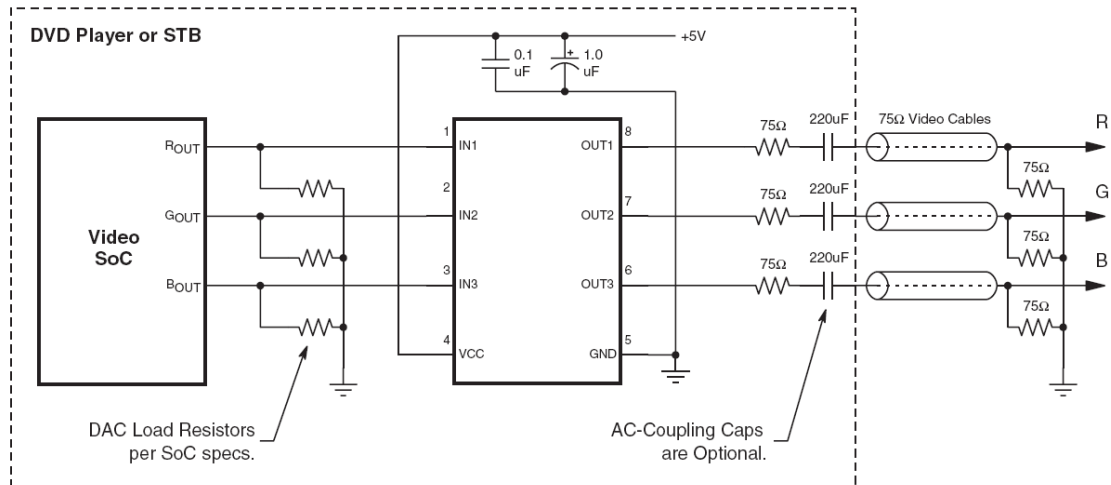
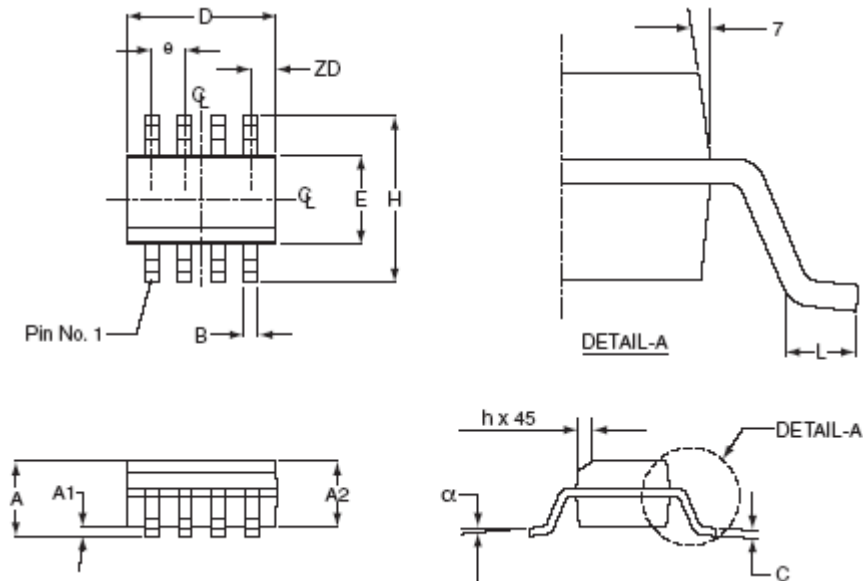


Figure 10. Typical application diagram



### PACKAGE DIMENSION

SOIC 8-Lead Small Outline Package



SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
	0°	8°
ZD	0.53 ref	
A2	1.37	1.57

NOTE: All dimensions are in millimeters.

### TAKE CARE!

This is ESD sensitive device, observe the same precautions that you would use with other ESD sensitive devices.