LD6835 series

Low-dropout regulator, high PSRR, 300 mA

Rev. 2 — 20 September 2013 Product data sheet

1. Product profile

1.1 General description

The LD6835 series is a small-size Low-DropOut (LDO) regulator family with a high-Power Supply Rejection Ratio (PSRR) of 75 dB and a voltage drop of 240 mV at 300 mA current rating. Operating voltages range from 1.75 V to 5.5 V. The products are available with fixed nominal output voltages $V_{O(nom)}$ between 1.2 V and 3.6 V.

The LD6835 series products are available in a DFN1010C-4 (SOT1194-1) plastic package with a size of 1 mm × 1 mm × 0.55 mm. The devices are ideal for use in portable applications requiring component miniaturization.

1.2 Features and benefits

- High PSRR
- Low quiescent current
- Soft start with optimized start-up time
- Temperature watchdog
- Current limiter with foldback circuit
- Low standby current in shutdown mode (typical 0.1 μA)
- Auto discharge or high-ohmic mode for the output state when disabled
- DFN1010C-4 (SOT1194-1) plastic package with a size of 1 mm × 1 mm × 0.55 mm
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant, free of halogen and antimony (Dark Green compliant)

1.3 Applications

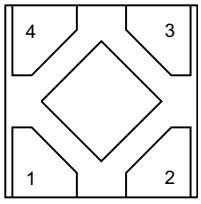
- Smartphones
- Mobile handsets
- Digital still cameras
- Tablet PCs
- Mobile internet devices
- Portable media players

1.4 Quick reference data

- I_O = 300 mA
- PSRR = 75 dB at 1 kHz
- RMS noise $V_{n(o)(RMS)}$ = 60 μV at 10 Hz to 100 kHz
- $t_{startup(reg)}$ = 150 μs
- V_I = 1.75 V to 5.5 V
- V_O = 1.2 V to 3.6 V
- Dropout voltage V_{do} = 240 mV at I_O = 300 mA
- Quiescent current I_q = 35 μA at I_O = 0 mA

2. Pinning information

2.1 Pinning



Transparent top view

Fig 1. Pin configuration for DFN1010C-4 (SOT1194-1)

2.2 Pin description

Table 1. Pin description for LD6835 series in DFN1010C-4 (SOT1194-1)

Symbol	Pin	Description
OUT	1	regulator output voltage
GND	2	supply ground
EN	3	device enable input; active HIGH
IN	4	regulator input voltage
i.c.	TAB	internally connected[1]

[1] The TAB is GND level (It is placed on the reverse side of the IC). It is recommended to connect the TAB to GND for a good thermal performance. Leaving it unconnected is also allowed.

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
LD6835K	DFN1010C-4 (HXSON4)	plastic thermal enhanced ultra thin small outline package; no leads; 4 terminals; body 1 × 1 × 0.55 mm	SOT1194-1

3.1 Ordering options

Further information on output voltage is available on request; see Section 19 “Contact information”

Table 3. Type number extension of high-ohmic output

Type number	Nominal output voltage $V_{O(nom)}$	Type number	Nominal output voltage $V_{O(nom)}$
LD6835K/12H	1.2 V	LD6835K/28H	2.8 V
LD6835K/15H	1.5 V	LD6835K/29H	2.9 V
LD6835K/18H	1.8 V	LD6835K/30H	3.0 V
LD6835K/22H	2.2 V	LD6835K/31H	3.1 V
LD6835K/25H	2.5 V	LD6835K/33H	3.3 V

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Table 4. Type number extension of pull-down output

Type number	Nominal output voltage $V_{O(nom)}$	Type number	Nominal output voltage $V_{O(nom)}$
LD6835K/12P	1.2 V	LD6835K/285P	2.85 V
LD6835K/15P	1.5 V	LD6835K/29P	2.9 V
LD6835K/18P	1.8 V	LD6835K/30P	3.0 V
LD6835K/22P	2.2 V	LD6835K/31P	3.1 V
LD6835K/25P	2.5 V	LD6835K/33P	3.3 V
LD6835K/28P	2.8 V	-	-

4. Block diagram

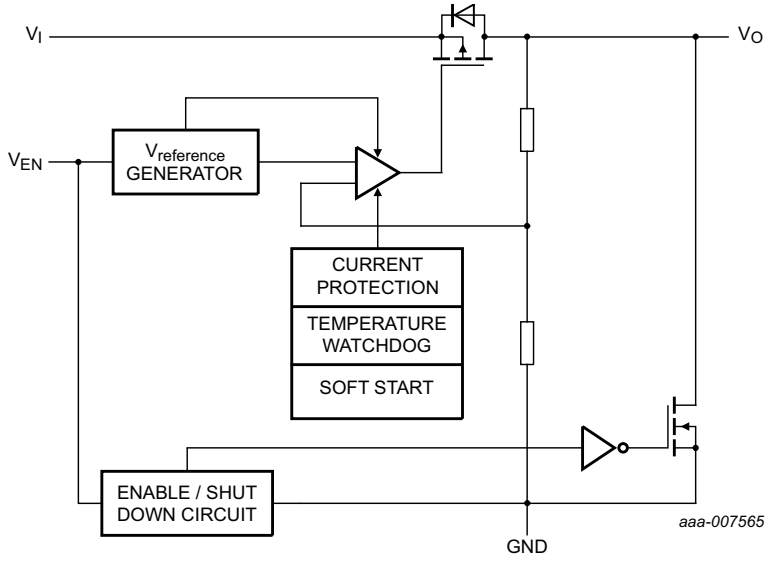

Fig 2. Block diagram of LD6835K/xxP (auto discharge function)

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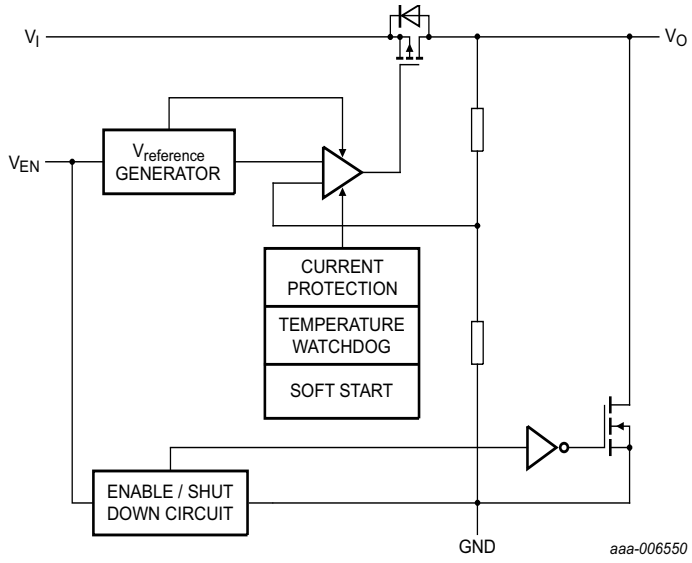

Fig 3. Block diagram of LD6835K/xxH (high-ohmic function)

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	4 ms transient		−0.5	+6.0	V
V_O	output voltage	4 ms transient		−0.5	+6.0	V
V_{EN}	voltage on pin EN	4 ms transient		−0.5	+6.0	V
P_{tot}	total power dissipation		[1]	-	400	mW
T_{stg}	storage temperature			−55	+150	°C
T_j	junction temperature			−40	+125	°C
T_{amb}	ambient temperature			−40	+85	°C
V_{ESD}	electrostatic discharge voltage	human body mode	[2]	-	±2	kV
		machine model	[3]	-	±200	V

[1] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 25 °C and the use of a two-layer Printed-Circuit Board (PCB).

[2] According to JESD22-A114F.

[3] According to JESD22-A115C.

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6. Recommended operating conditions

Table 6. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	125	°C
Pin IN					
V_I	input voltage		1.75	5.5	V
$C_{ext(IN)}$	external capacitance on pin IN		1	-	µF
Pin EN					
V_{EN}	voltage on pin EN		–0.5	+5.5	V
Pin OUT					
V_O	output voltage		–0.5	V_I + 0.3	V
$C_{L(ext)}$	external load capacitance	[1]	1	-	µF

[1] See Section 10.1 “Capacitor values”.

7. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1][2]	250	K/W

[1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all pins must have a solid connection to large Cu layer areas for example to the power and ground layer. In multilayer PCB applications, the second layer should be used to create a large heat spreader area directly below the LDO. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Avoid the use of solder-stop varnish under the chip.

[2] Use the measurement data given for a rough estimation of the $R_{th(j-a)}$ in your application. The actual $R_{th(j-a)}$ value can vary in applications using different layer stacks and layouts.

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8. Characteristics

Table 8. Electrical characteristics

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); $V_I = V_{O(nom)}$ + 1.0 V; output capacitor $C_{L(ext)}$ = 1 µF; input capacitor $C_{ext(IN)}$ = 1 µF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output voltage							
V_{do}	dropout voltage	I_O = 300 mA; $V_I = V_{O(nom)} - 0.1$ V	[1]	-	240	-	mV
ΔV_O	output voltage variation	$V_O \geq 1.8$ V; I_O = 1 mA					
		T_{amb} = +25 °C		−2	±0.5	+2	%
		−40 °C ≤ T_{amb} ≤ +85 °C	[1]	−3	-	+3	%
		V_O < 1.8 V; I_O = 1 mA					
		T_{amb} = +25 °C		−3	±0.5	+3	%
		−40 °C ≤ T_{amb} ≤ +85 °C	[1]	−4	-	+4	%
Line regulation error							
$\Delta V_O/(V_O \times \Delta V_I)$	relative output voltage variation with input voltage	$V_I = (V_{O(nom)} + 0.5\text{ V})$ to 5.0 V; I_O = 1 mA	[1]	−0.1	-	+0.1	%/V
Load regulation error							
$\Delta V_O/(V_O \times \Delta I_O)$	relative output voltage variation with output current	1 mA ≤ I_O ≤ 300 mA	[1]	−0.01	±0.0025	+0.01	%/mA
Output current							
I_O	output current			300	-	-	mA
$I_{act(fold)}$	foldback activation current	$V_O = 0.9 \times V_{O(nom)}$	[1]	-	500	-	mA
I_{sc}	short-circuit current	V_O = 0 V	[1]	-	60	-	mA
Regulator quiescent current							
I_q	quiescent current	V_{EN} = 1.1 V; I_O = 0 mA		-	35	75	µA
		V_{EN} = 1.1 V; I_O = 300 mA	[1]	-	450	-	µA
		$V_{EN} \leq 0.4$ V		-	0.1	1	µA
Ripple rejection and output noise							
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; I_O = 30 mA	[1]	-	75	-	dB
$V_{n(o)(RMS)}$	RMS output noise voltage	f_{ripple} = 10 Hz to 100 kHz; I_O = 10 mA	[1]	-	60	-	µV
Enable input and timing							
V_{IL}	LOW-level input voltage	pin EN		0	-	0.4	V
V_{IH}	HIGH-level input voltage	pin EN		1.1	-	5.5	V
I_{en}	enable current	pin EN		-	400	-	nA
$t_{startup(reg)}$	regulator start-up time	$V_O = 0.95 \times V_{O(nom)}$; I_O = 300 mA	[2]	-	150	-	µs
LD6835K/xxP auto discharge function							
$t_{sd(reg)}$	regulator shutdown time	$V_O = 0.05 \times V_{O(nom)}$		-	300	-	µs
R_{pd}	pull-down resistance			-	100	-	Ω
Thermal protection							
T_{sd}	shutdown temperature		[3]	-	160	-	°C
$T_{sd(hys)}$	shutdown temperature hysteresis		[3]	-	20	-	K

[1] Parameter is checked, verified and guaranteed by design.

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[2] $V_{O(nom)}$ = nominal output voltage (devices specific).

[3] If the device reaches the shutdown temperature, the LDO is disabled. The LDO will restart after the device temperature is decreased to the shutdown temperature minus the shutdown temperature hysteresis.

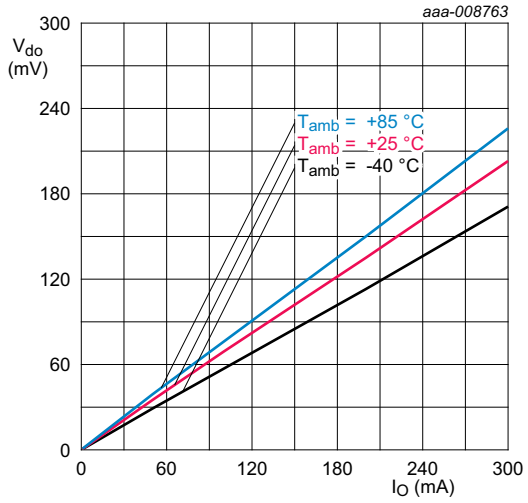
9. Dynamic behavior

All results described in this section are based on measurements of types LD6835K/xxx from the LD6835 product series.

9.1 Dropout

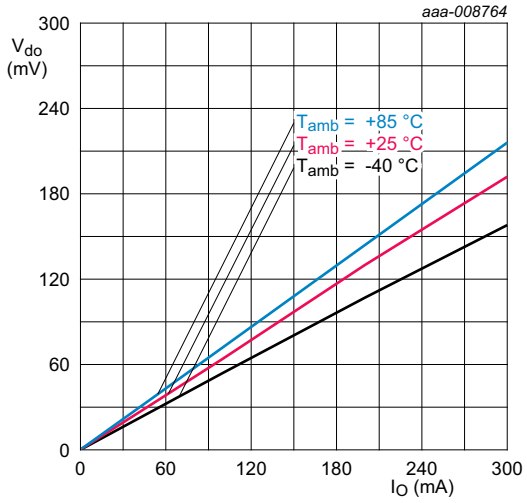
The dropout voltage is defined as the smallest input-to-output voltage difference at a specified load current when the regulator operates within its linear region with the pass transistor functioning simply as a resistor. This means that the input voltage is below the nominal output voltage value.

A small dropout voltage guarantees lower power consumption and maximizes efficiency.



V_I = 2.9 V; $V_{O(nom)}$ = 3.0 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 4. Dropout voltage as a function of output current for LD6835K/30x



V_I = 3.2 V; $V_{O(nom)}$ = 3.3 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 5. Dropout voltage as a function of output current for LD6835K/33x

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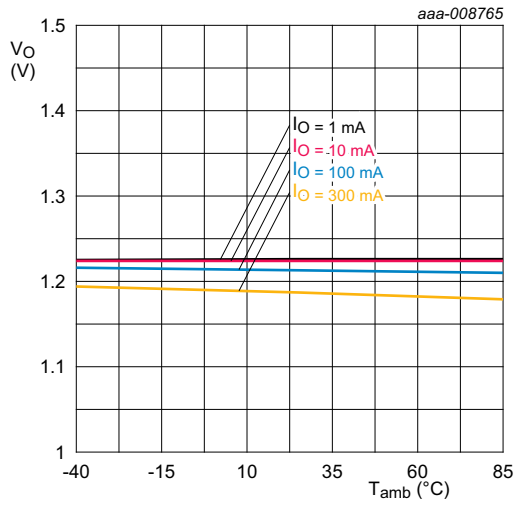
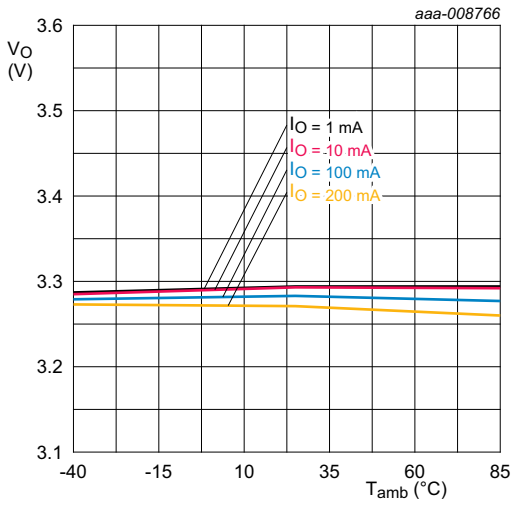
9.2 Temperature dependency



V_I = 2.3 V; $V_{O(nom)}$ = 1.2 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 6. Temperature dependency of LD6835K/12x

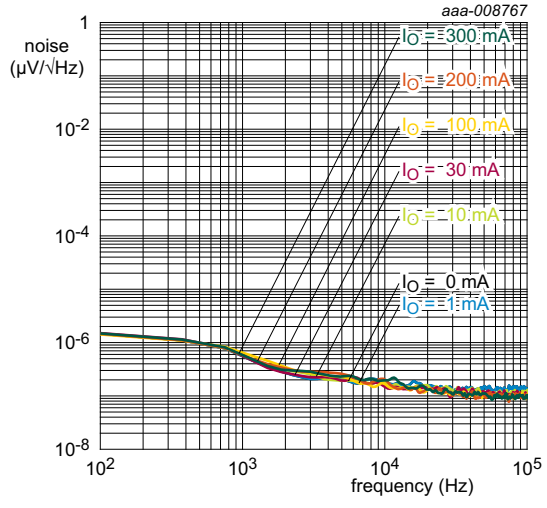


V_I = 4.5 V; $V_{O(nom)}$ = 3.3 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 7. Temperature dependency of LD6835K/33x

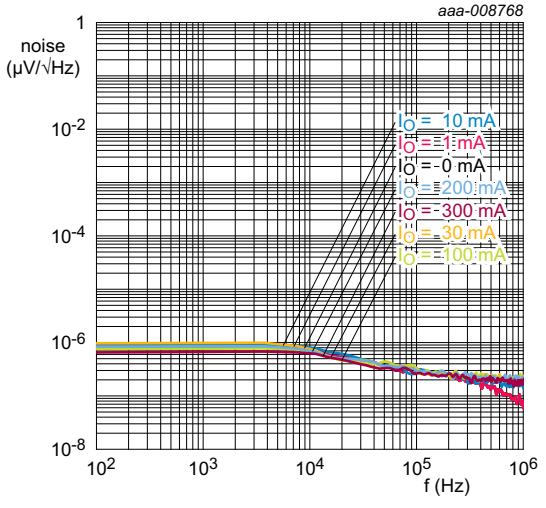
9.3 Noise

Output noise voltage of an LDO circuit is given as noise density or RMS output noise voltage over a defined range of frequencies (10 Hz to 100 kHz). Permanent conditions are a constant output current and a ripple-free input voltage. The output noise voltage is generated by the LDO regulator.



V_I = 4.5 V; $V_{O(nom)}$ = 1.2 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 8. Noise density for LD6835K/12x



V_I = 4.5 V; $V_{O(nom)}$ = 3.3 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 9. Noise density for LD6835K/33x

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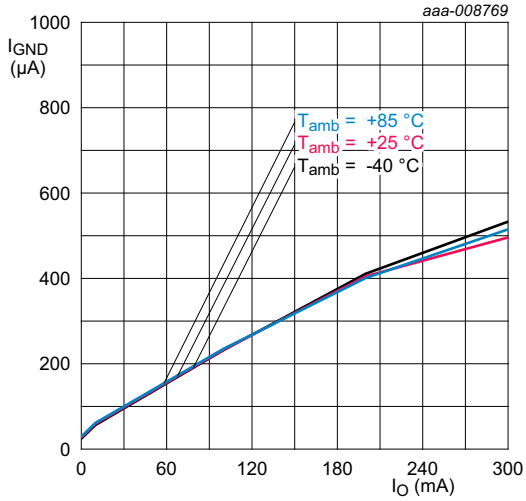
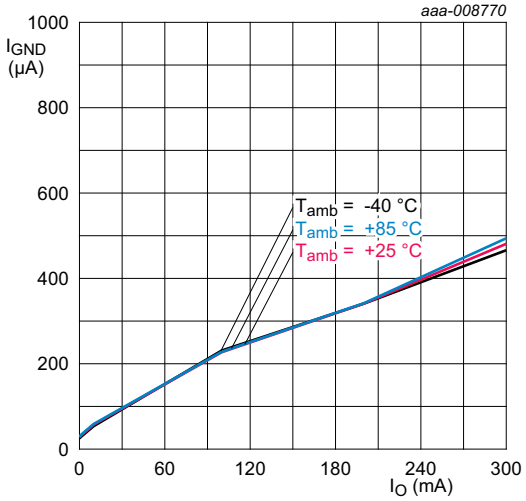
9.4 Quiescent current

Quiescent or ground current is the difference between the input and the output current of the regulator.



V_I = 2.3 V; $V_{O(nom)}$ = 1.2 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 10. Quiescent current for LD6835K/12x



V_I = 4.5 V; $V_{O(nom)}$ = 3.3 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 11. Quiescent current for LD6835K/33x

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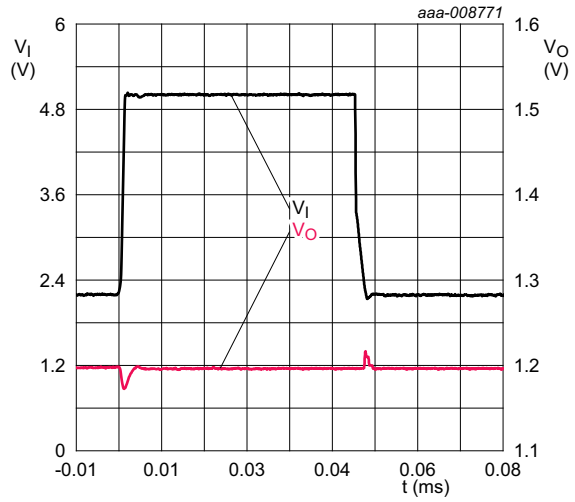
9.5 Line regulation

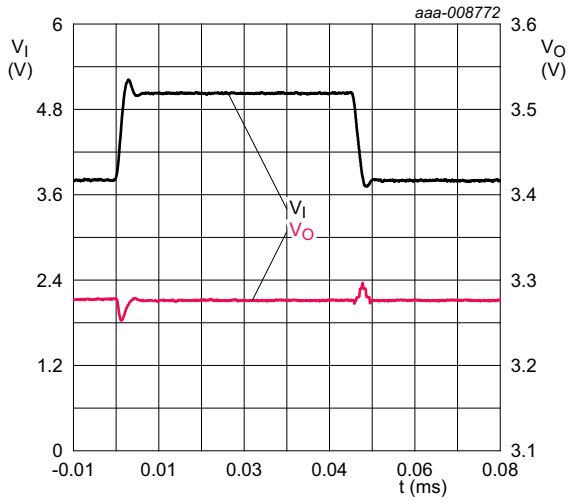
Line regulation response is the capability of the circuit to maintain the nominal output voltage while varying the input voltage.

$$Line\ regulation\ (\%/V) = \frac{\Delta V_O}{\Delta V_I} \times \frac{100}{V_O} \quad (1)$$



$V_{O(nom)}$ = 1.2 V; I_O = 300 mA; $t_r = t_f$ = 2 µs; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 12. Line regulation for LD6835K/12x



$V_{O(nom)}$ = 3.3 V; I_O = 300 mA; $t_r = t_f$ = 2 µs; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 13. Line regulation for LD6835K/33x

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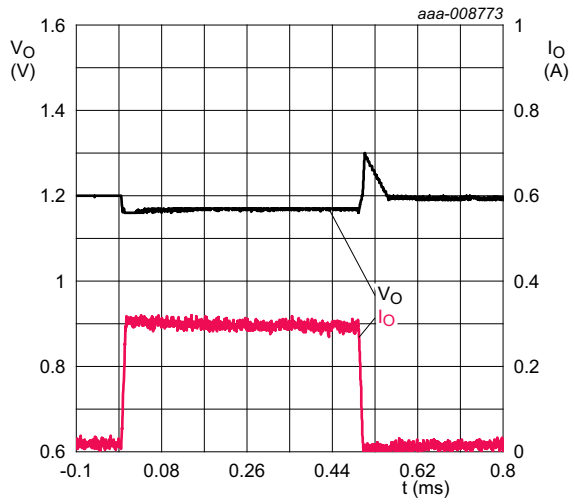
9.6 Load regulation

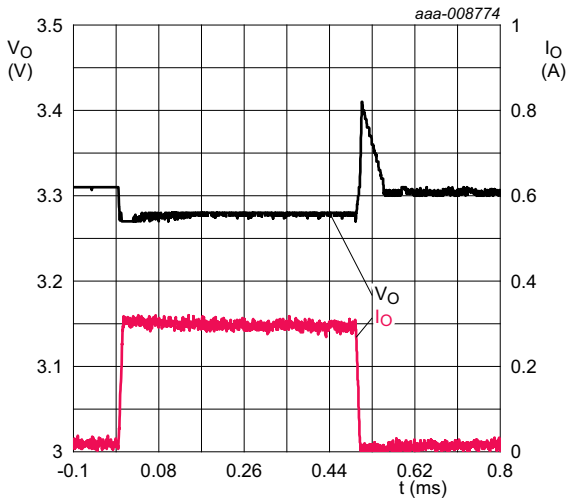
Load regulation is the capability of the circuit to maintain the nominal output voltage while varying the output load current.

$$Load\ regulation\ (\%/mA) = \frac{\frac{\Delta V_O}{V_{O(nom)}} \times 100}{\Delta I_O} \quad (2)$$



$V_{O(nom)}$ = 1.2 V; I_O = 1 mA to 300 mA; $t_r = t_f$ = 2 µs; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 14. Load regulation for LD6835K/12x



$V_{O(nom)}$ = 3.3 V; I_O = 1 mA to 300 mA; $t_r = t_f$ = 2 µs; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 15. Load regulation for LD6835K/33x

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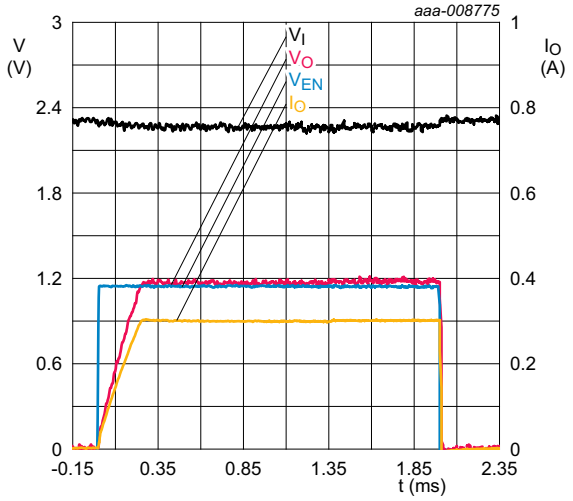
9.7 Start-up, inrush current

Start-up time defines the time needed for the LDO to achieve 95 % of its typical output voltage level after activation via the enable pin.



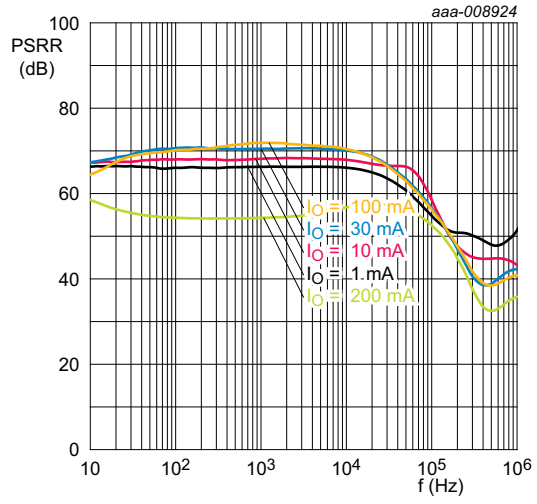
$V_{O(nom)}$ = 3.3 V; I_O = 300 mA; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 16. Start-up and inrush current for LD6835K/12P

9.8 Power Supply Rejection Ratio (PSRR)

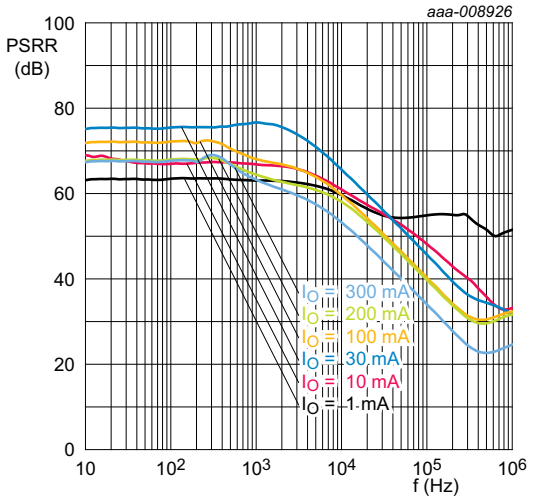
PSRR stands for the capability of the regulator to suppress unwanted signals on the input voltage like noise or ripples.

$$PSRR\ (dB) = (-20)log\frac{V_{O(ripple)}}{V_{I(ripple)}}$$ for all frequencies.



$V_{O(nom)}$ = 1.8 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 17. PSRR for LD6835K/18x



$V_{O(nom)}$ = 3.3 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 18. PSRR for LD6835K/33x

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10. Application information

10.1 Capacitor values

The LD6835 series requires external capacitors at the output to guarantee a stable regulator behavior. Also an input capacitor is recommended to keep the input voltage stable. These capacitors should not violate the specified minimum Equivalent Series Resistance (ESR).

The absolute value of the total capacitance attached to the output pin OUT influences the regulator shutdown time ($t_{sd(reg)}$) of the LD6835 series.

Table 9. External load capacitor

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{ext(IN)}$	external capacitance on pin IN		[1]	0.7	1.0	-	µF
$C_{L(ext)}$	external load capacitance		[1]	0.7	1.0	-	µF
ESR	equivalent series resistance			5	-	500	mΩ

[1] The minimum value of capacitance for stability and correct operation is 0.7 µF. The capacitor tolerance should be ±30 % (over the temperature range). The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure that this minimum capacitance specification is met. The recommended capacitor type is X7R to meet the full temperature specification of –40 °C to +125 °C.

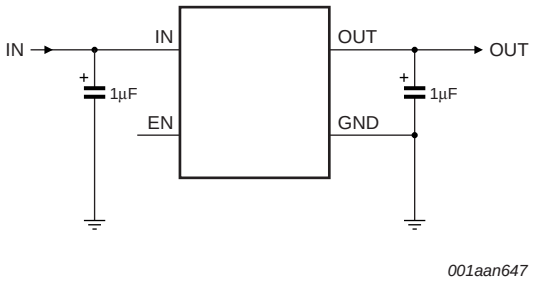

Fig 19. Application diagram

11. Test information

11.1 Quality information

This product has been qualified in accordance with *NX1-00023 NXP Semiconductors Quality and Reliability Specification* and is suitable for use in consumer applications.

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12. Marking

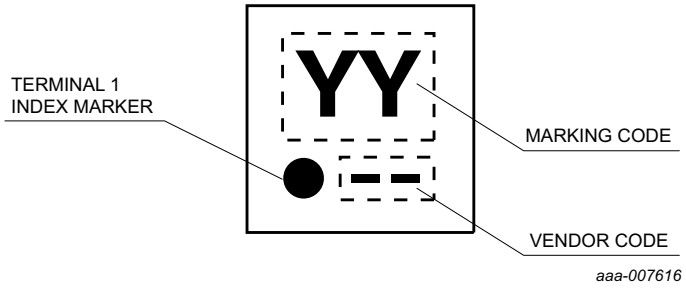

Fig 20. Marking DFN1010C-4 (SOT1194-1)

Table 10. Marking of high-ohmic output

Type number	Nominal output voltage $V_{O(nom)}$	Marking code	Type number	Nominal output voltage $V_{O(nom)}$	Marking code
LD6835K/12H	1.2 V	AA	LD6835K/28H	2.8 V	QA
LD6835K/15H	1.5 V	DA	LD6835K/29H	2.9 V	RA
LD6835K/18H	1.8 V	GA	LD6835K/30H	3.0 V	SA
LD6835K/22H	2.2 V	KA	LD6835K/31H	3.1 V	TA
LD6835K/25H	2.5 V	NA	LD6835K/33H	3.3 V	VA

Table 11. Marking of pull-down output

Type number	Nominal output voltage $V_{O(nom)}$	Marking code	Type number	Nominal output voltage $V_{O(nom)}$	Marking code
LD6835K/12P	1.2 V	AB	LD6835K/285P	2.85 V	ZB
LD6835K/15P	1.5 V	DB	LD6835K/29P	2.9 V	RB
LD6835K/18P	1.8 V	GB	LD6835K/30P	3.0 V	SB
LD6835K/22P	2.2 V	KB	LD6835K/31P	3.1 V	TB
LD6835K/25P	2.5 V	NB	LD6835K/33P	3.3 V	VB
LD6835K/28P	2.8 V	QB	-	-	-

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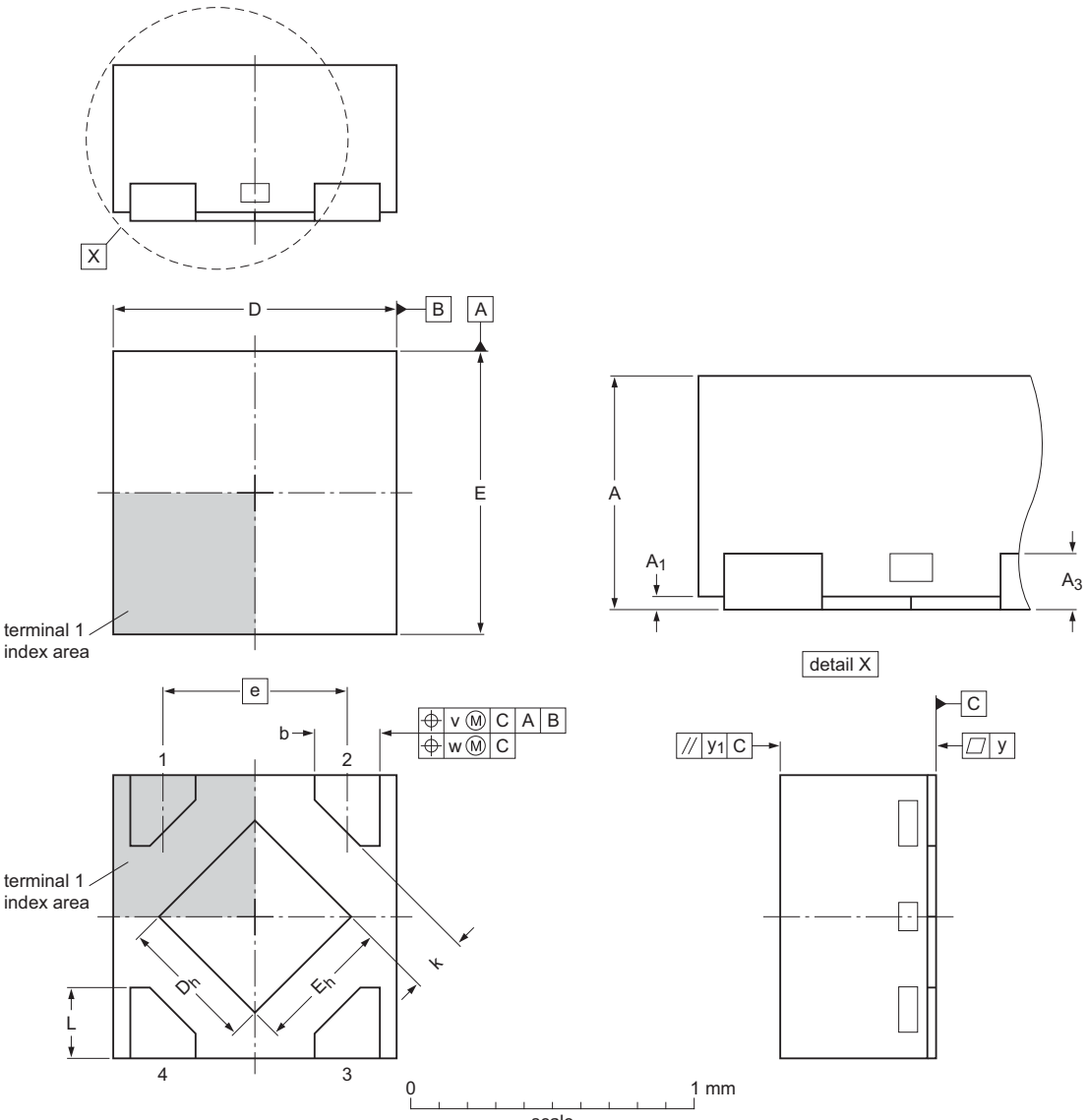
13. Package outline

Plastic thermal enhanced ultra thin small outline package; no leads; 4 terminals; body 1 x 1 x 0.55 mm **SOT1194-1**



Dimensions

Unit(1)		A	A_1	A_3	b	D	D_h	E	E_h	e	k	L	v	w	y	y_1
mm	max	0.55	0.05	0.152	0.30	1.05	0.53	1.05	0.53			0.30				
	nom				0.25	1.00	0.48	1.00	0.48	0.65		0.25	0.1	0.05	0.05	0.05
	min		0.00	0.05	0.20	0.95	0.43	0.95	0.43		0.2	0.20				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1194-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1194-1	---	---	---			~~11-05-30~~ 12-05-22

Fig 21. Package outline DFN1010C-4 (SOT1194-1)

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14. Packing information

14.1 Packing methods

Table 12. Packing methods

Type number	Package	Description	Orientation [1]	12NC ending	Packing quantity
LD6835K	DFN1010C-4 (SOT1194-1)	2 mm pitch, 8 mm tape and reel	Q1	115	10000

[1] For further information about orientation, see Section 14.2.

14.2 Carrier tape information

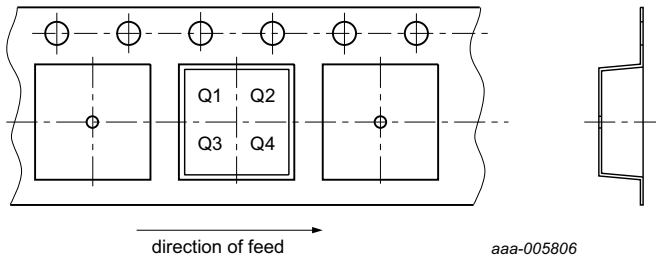

Fig 22. Carrier tape

Table 13. Orientations

Orientation	Meaning	Pin 1 location
Q1	quadrant 1	upper left
Q2	quadrant 2	upper right
Q3	quadrant 3	lower left
Q4	quadrant 4	lower right

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15. Soldering

Footprint information for reflow soldering of HXSON4 package **SOT1194-1**

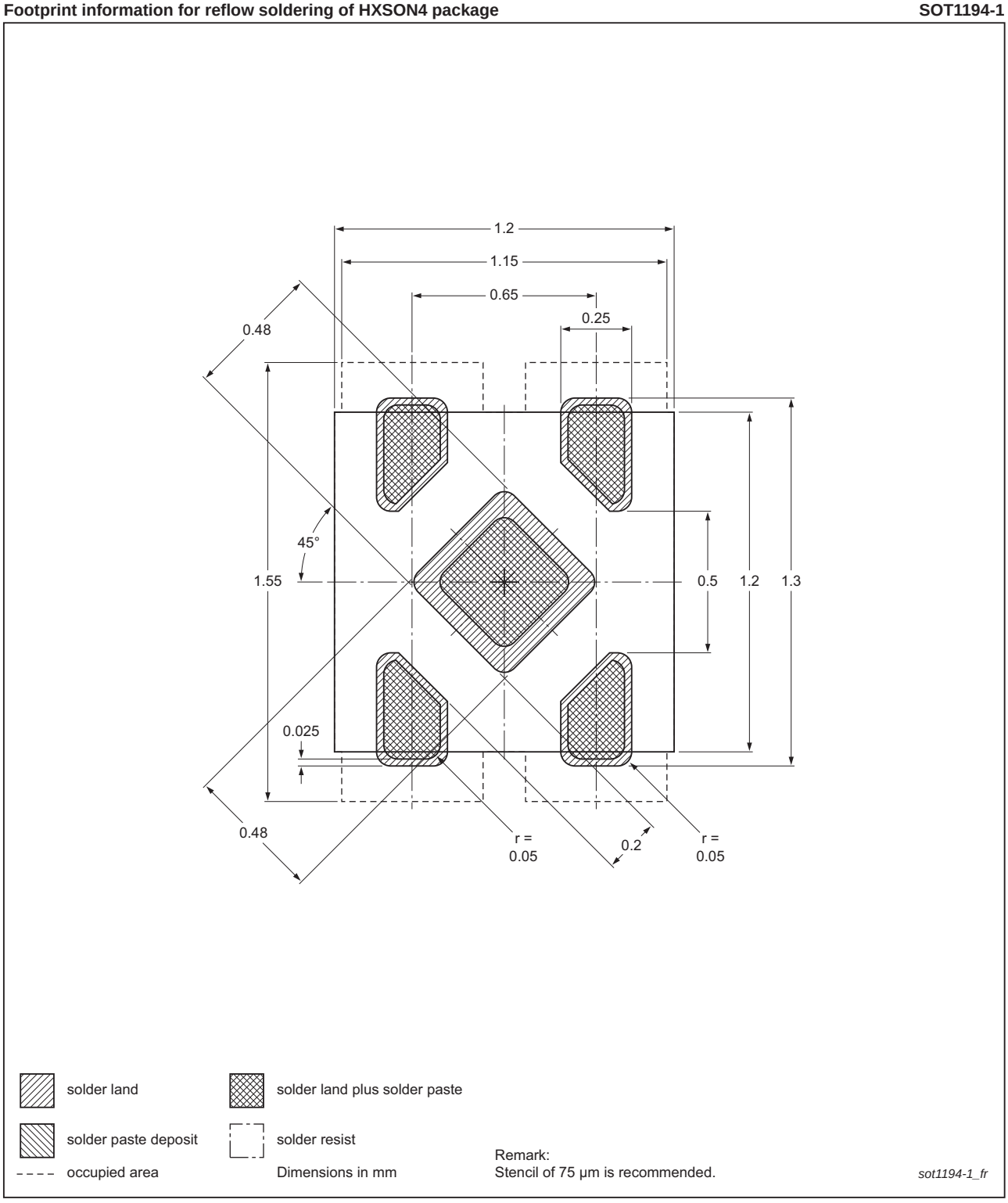

Fig 23. Soldering footprint DFN1010C-4 (SOT1194-1)

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16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 24) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14 and 15

Table 14. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 24.

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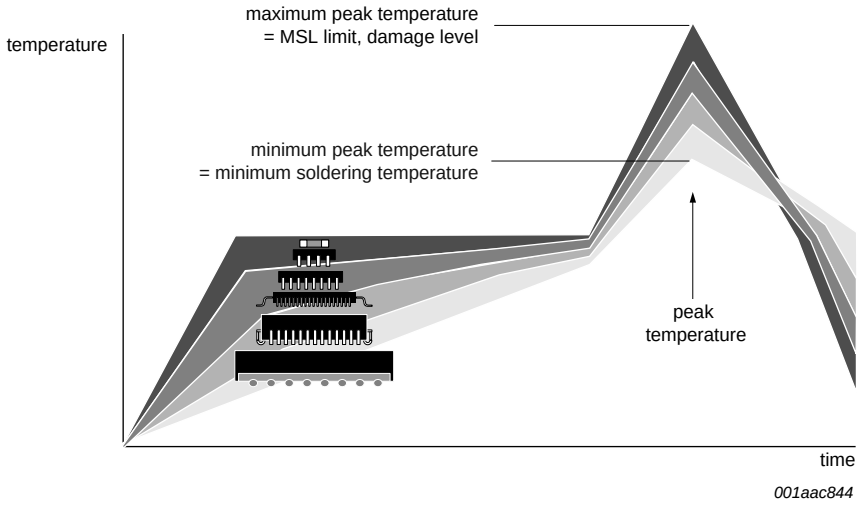

MSL: Moisture Sensitivity Level

Fig 24. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LD6835_SER v.2	20130920	Product data sheet	-	LD6835_SER v.1
Modifications:	• Data sheet status changed			
LD6835_SER v.1	20130704	Preliminary data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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