90mA, Ultra Low Quiescent Current CMOS LDO Regulator with Voltage Detector Circuit

REV:01b

General Description

The LD6991/A is an ultra low quiescent micropower linear regulator with voltage detector circuit. For regulator circuit, the precision of feedback reference voltage is within ±2% and output current is up to 90mA. As well, it can be stable with 1uF output capacitor which reduces the board space and cost. For voltage detector circuit, the reset threshold voltage accuracy is within ±2% and the reset time period is adjustable by an external capacitor.

LD6991/A is available in a space saving SC70-6 package.

+patent pending

Features

REGULATOR CIRCUIT

- Low Dropout: 350mV @50mA
- Ultra Low Quiescent Current: 5μA(typ)
- Thermal Shutdown and Current Limiting Protection
- Stable with 1μF Capacitor
- Output Voltage: 1.5V to 3.3V (step 0.1V)

VOLTAGE DETECTOR CIRCUIT

- Reset Threshold Voltage 1.2V to 3.3V (step 0.1V)
- Low Supply Current:3μA (typ)
- Capacitor-Adjustable Reset Timeout Period
- Reset Output Options
  Active-Low Open Drain (LD6991)
  Active-High Open Drain (LD6991A)

Applications

- Battery-Powered Equipment
- Hand-Held Instruments

Typical Application

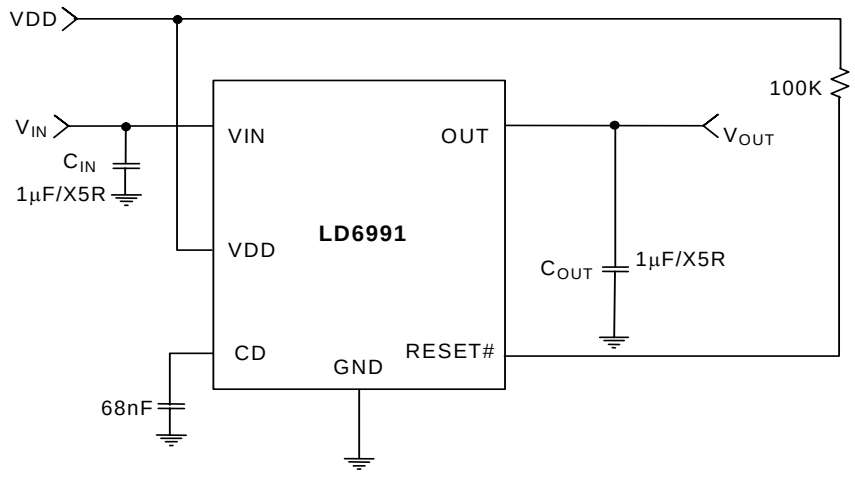
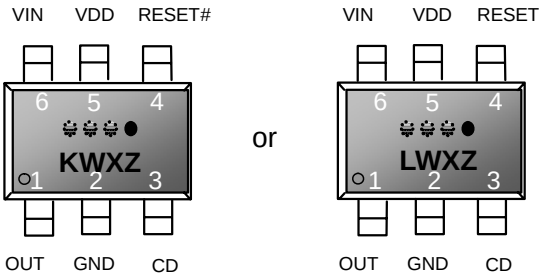


Fig.1 Typical Application Circuit

Pin Configuration

SC-70-6 (Top view)



K: Product code: LD6991
L: Product code: LD6991A
●●●● : Year code (Binary, ●●●● = 2007, ●●●○ =2008)
W: Week code
X: Regulator Output Voltage (H~Z: 1.5V~3.3V)
Z: Voltage Detector Output Voltage (E~Z:1.2~3.3V)

Ordering Information

Part number	Package	TOP MARK	Shipping
LD6991 GU-XXZZ	SC70-6	KWXZ	3000 /tape & reel
LD6991A GU-XXZZ	SC70-6	LWXZ	3000 /tape & reel

Note 1: The LD6991/A is Green Packaged/ ROHS compliant.

Note 2: -XX suffix for Regulator Output, from 1.5V~3.3V in 0.1V increment.

-ZZ suffix for Reset Threshold Voltage, from 1.2V~3.3V in 0.1V increment.

Ex: LD6991GU-3019 is with 3.0V of Regulator Output and 1.9V of Reset Threshold Voltage.

Pin Descriptions

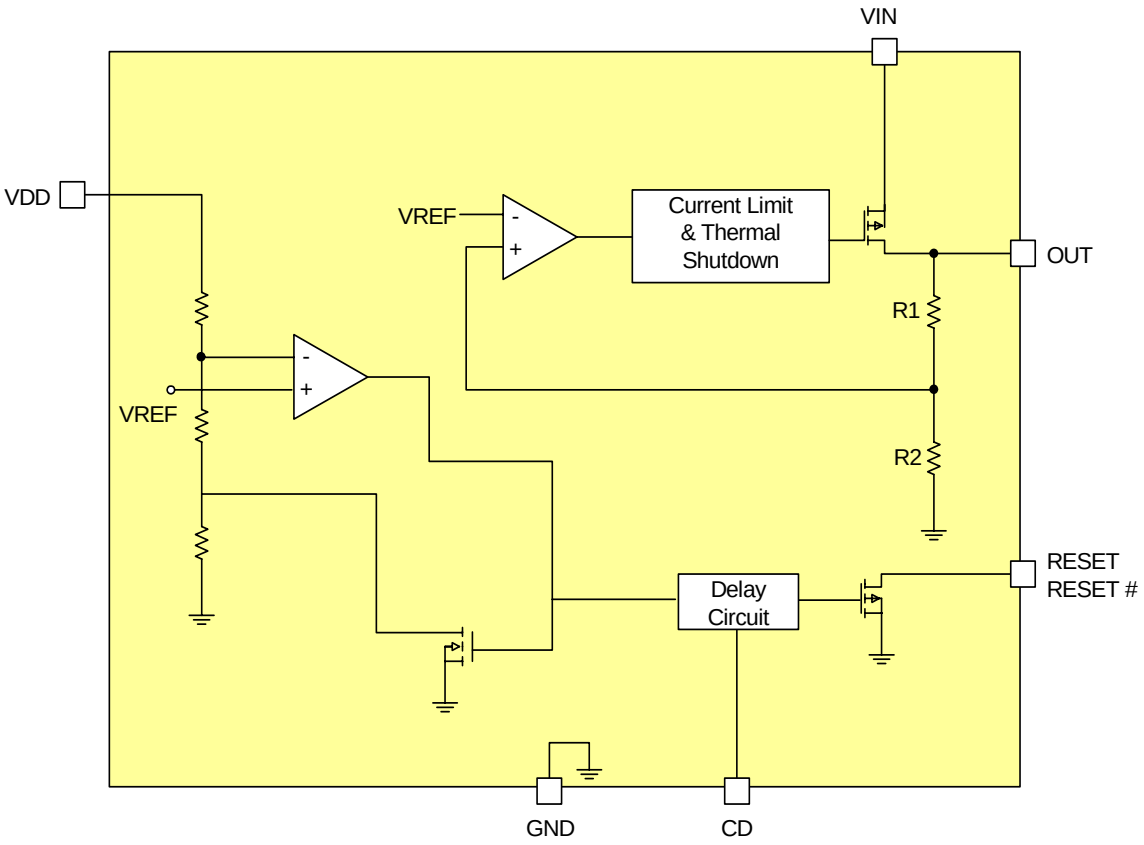
LD6991

PIN	NAME	FUNCTION
1	OUT	Regulator output
2	GND	IC GND
3	CD	Connect a capacitor between CD Pin and GND to set the timeout period.
4	RESET#	Active Low Open Drain Reset Output. RESET# changes from high to low whenever VDD drops below the selected reset threshold voltage (VTH). RESET# remains low for the reset time out period after all reset conditions are removed and then goes high.
5	VDD	Supply and Input for Voltage Detector Circuit
6	VIN	Input voltage for regulator circuit

LD6991A

PIN	NAME	FUNCTION
1	OUT	Regulator output
2	GND	IC GND
3	CD	Connect a capacitor between CD Pin and GND to set the timeout period.
4	RESET	Active High Open Drain Reset Output. RESET changes from low to high whenever VDD drops below the selected reset threshold voltage (VTH). RESET remains high for the reset time out period after all reset conditions are removed and then goes low.
5	VDD	Supply and Input for Voltage Detector Circuit
6	VIN	Input voltage for regulator circuit

Block Diagram



Absolute Maximum Ratings

VIN,VDD,OUT Pin	-0.3V~6.5V
CD, RESET, RESET # Pin	-0.3V~(VDD+0.3)V
Power dissipation SC70-6@Ta=25°C	300mW
Operating Temperature Range	-30°C to 85°C
Package Thermal Resistance SC70-6	333°C/W
Storage Temperature Range	-55°C to 125°C
Junction Temperature	150°C
Lead temperature (Soldering, 10sec)	260°C
ESD Level (Human Body Model)	2KV
ESD Level (Machine Model)	200V

Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{IN}=V_{OUT}+1.5V, C_{IN}=C_{OUT}=1μF, VDD=3.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REGULATOR CIRCUIT					
VIN Input Voltage		2.0	-	6	V
VIN Quiescent current	V_{IN}=5V, I_{OUT}=0mA		5	8	μA
Dropt Voltage	I_{OUT}=1mA, V_{IN}>3.6V		10	25	mV
	I_{OUT}=50mA, V_{IN}>3.6V		350	550	mV
Output Current Limit		90	150	-	mA
Output Voltage Accuracy	I_{OUT}=1mA	-2		+2	%
Line Regulation	V_{IN}=V_{OUT}+1V, to 5.5V, I_{OUT}=1mA	-	0.1	0.2	%/V
Load Regulation	1mA<I_{OUT}<50mA	-	0.02	0.04	%/mA
Ripple Rejection	F=1KHz, EIN=1Vrms, I_{OUT}=10mA	-	40	-	dB
Thermal Shutdown	V_{OUT} short to GND		130		°C
Hysteresis			20		°C
VOLATGE DETECTOR CIRCUIT					
VDD Operating Voltage Range		0.9	-	6	V
VDD Supply Current	V_{DD}<4.5V, CD=0nF		3	6.5	μA
	V_{DD}<3.3V, CD=0nF		2.5	5.5	
	V_{DD}<2.0V, CD=0nF		2	5	
Reset Threshold Voltage		1.2	-	3.3	V
Reset Threshold Voltage Accuracy		-2	-	2	%
Threshold Voltage Hysteresis Width		0.03VTH	0.05VTH	0.08VTH	V
Reset timeout Period	CD=68nF	33	50	75	mS
	CD=0nF		25		μS
Open Drain Leakage Current	VDD=3V, RESET / RESET#=5V			1	μA
Reset Output Voltage Low (Note)	V_{DD}=3V<V_{TH}, I_{SHINK}=3.5mA			0.6	V

Note: The voltage V_{OL} can be calculated by V_{OL}=V_{DD}-Ir*R. where R is the pull-up resistor and Ir is the current flowing through the pull-up resistor. For typical application (R=100KΩ), V_{OL} is less than 0.2V.

Typical Performance Characteristics

LDO Regulator (C_{IN}=I_{OUT}=1μF, V_{OUT}=3.0V, V_{IN}=V_{OUT}+1V, LD6991)

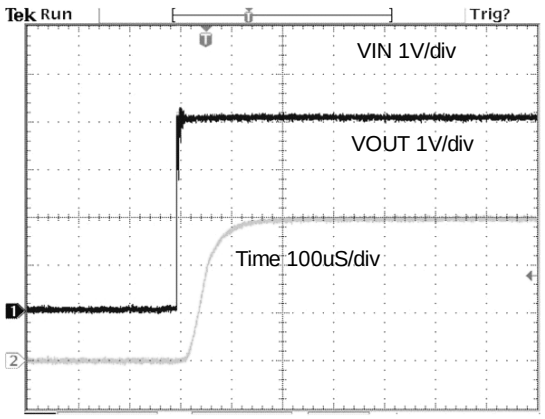


Fig. 2 Start Up Response

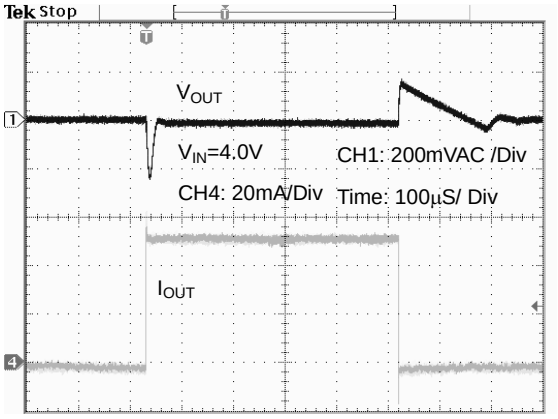


Fig. 3 Load Transient Response

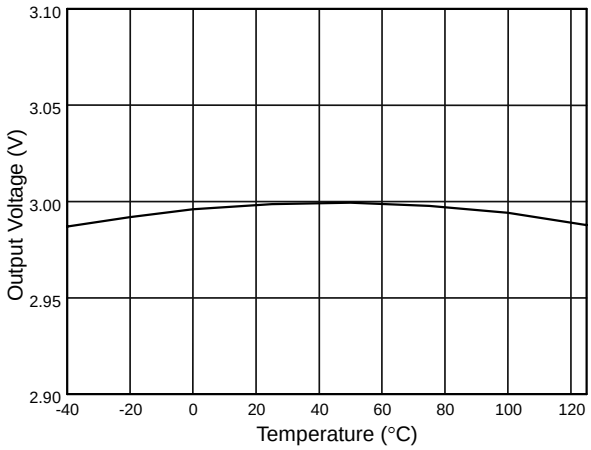


Fig. 4 Output Voltage vs. Temperature

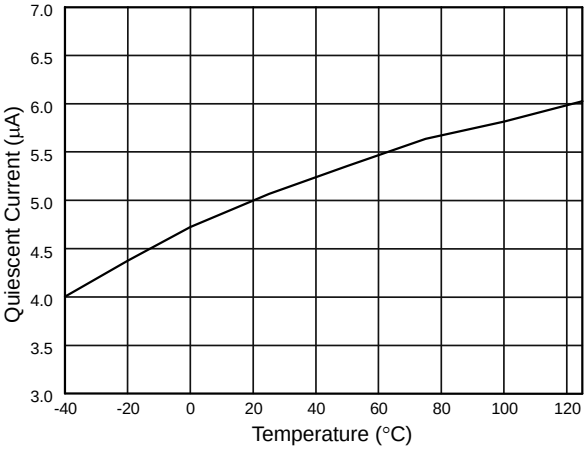


Fig. 5 Quiescent Current vs. Temperature

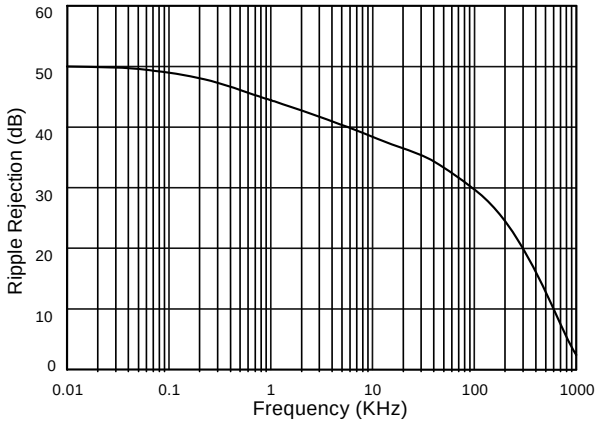


Fig. 6 Ripple Rejection vs. Frequency

Voltage Detector (Reset Voltage=1.8V, R=100KΩ, LD6991)

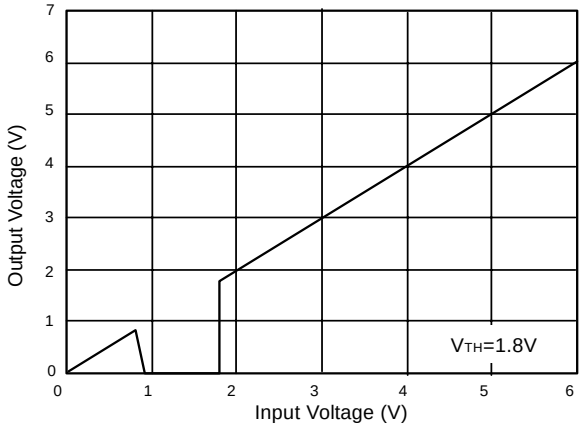


Fig. 7 Output Voltage vs. Input Voltage

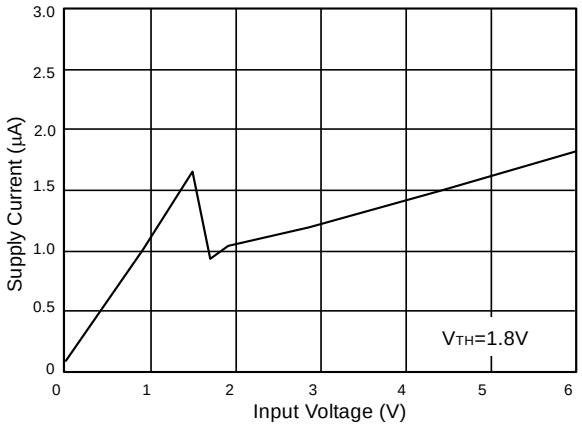


Fig. 8 Supply Current vs. Input Voltage

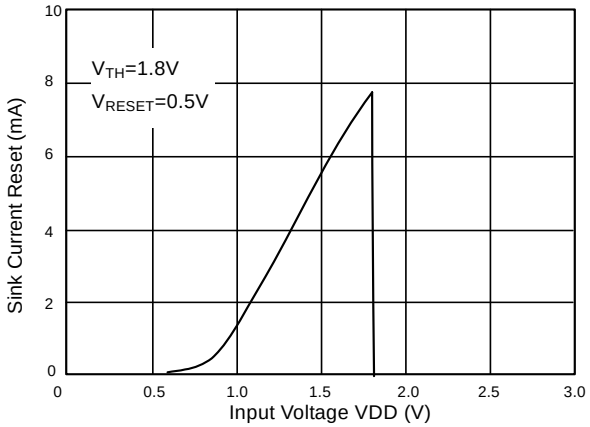


Fig. 9 N-Ch Driver Sink Current vs. Input Voltage

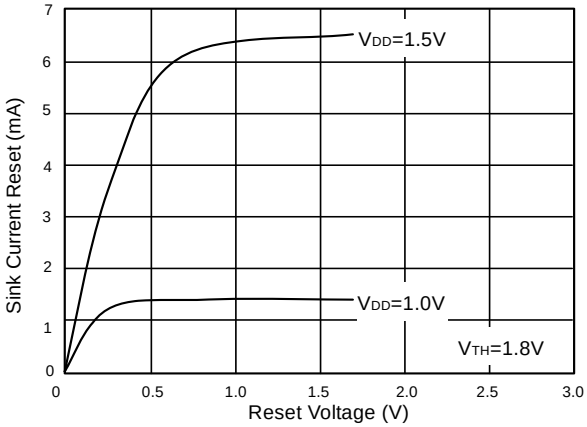


Fig. 10 N-Ch Driver Sink Current vs. RESET Voltage

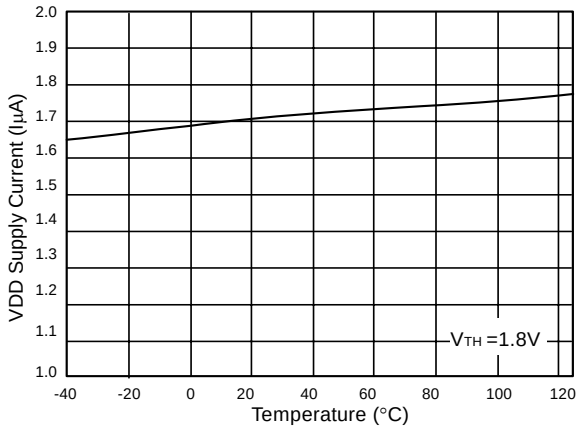


Fig. 11 VDD Supply Current vs. Temperature

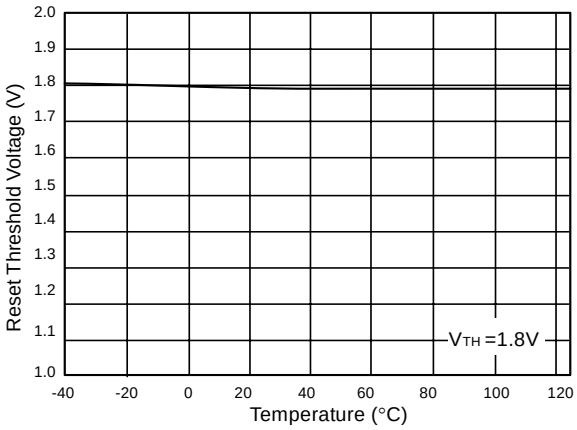


Fig. 12 Reset Threshold Voltage vs. Temperature

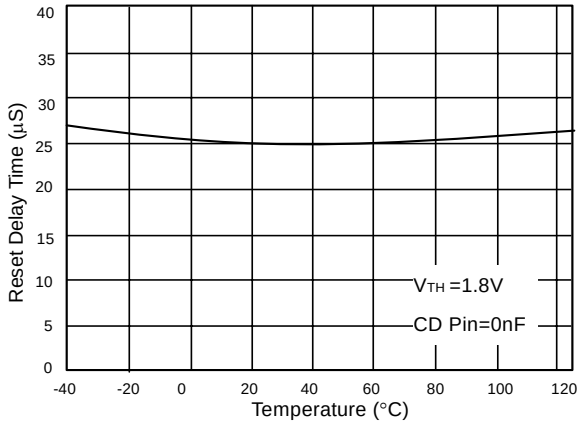


Fig. 13 Reset Delay Time vs. Temperature

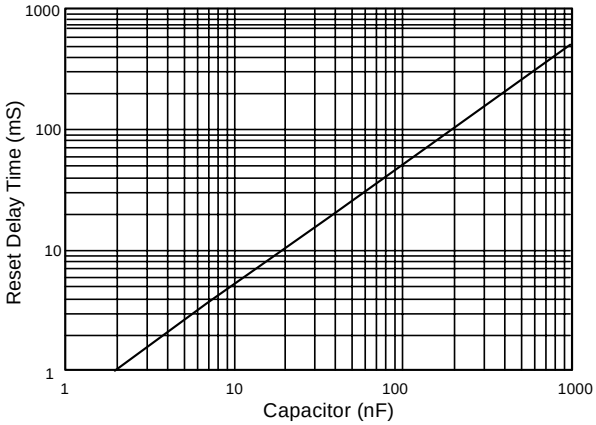


Fig. 14 Reset Delay Time vs. Capacitor

Application Information

Regulator Circuit

An input capacitor is required to place between the input and GND to stabilize V_{IN}. The input capacitor should be at least of 1μF to obtain beneficial effect. Besides, the input capacitor should be located in the distance within 5 mm from the VIN pin.

For stable operation, the output capacitor should be in the range of 1μF to 10μF with ESR >25 mΩ. The figure 1 shows the curves of the allowable ESR range as a function of load current for C_{OUT}=1μF.

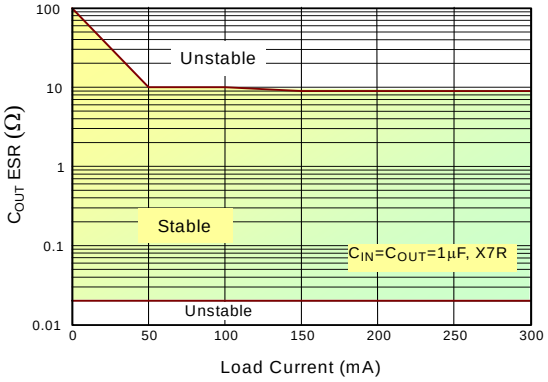


Fig. 15 Region of Stable C_{OUT} ESR vs. Load Current

The output capacitor should be located in the distance within 5mm from the OUT pin.

X5R or X7R types of capacitors are recommended for the input and output capacitors.

Current Limit

Output current is limited to 150mA (typical). When current limit engages, the output voltage scales back linearly until the over-current condition come to an end. Take care not to exceed the power dispassion ratings of the package.

Thermal Consideration

The thermal sensor would disable the pass transistor as soon as it detects the junction temperature over the limit of 130°C. It remains disable until it's cooled down to about 20°C (typ.). For continuous operation, it's not recommended to operate while the maximum junction temperature is above 125°C. The maximum power dissipation is determined according to following equation.

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

θ_{JA}: Package Thermal Resistance

The maximum power dispassion at Ta=25°C can be obtained by above formula.

P_{DMAX}=(125°C-25°C)/333=300mW

……..(SC70-6 package)

Voltage Detector Circuit

The LD6991/A performs supervisory by sending out a reset signal whenever the VDD voltage falls below a preset threshold level. This reset-signal will continue in the whole period unless VDD recovers. Once the VDD recovered up-crossing the threshold level, the reset signal will be released after a certain delay time. The LD6991 features an active-low, open drain reset output, and LD6991A features an active-high, open drain reset output.

Selecting a Reset Capacitor

The reset delay time is set by an external capacitor. The reset timeout period can be determined by following equations.

$$T_D = 0.735C_D + 0.025 \quad (mS)$$

Where T_D is in mS, ands C_D in nF.

Ex: C_D =68nF→ T_D~=50mS

C_D must be a low-leakage (<10nA) type capacitor, ceramic capacitor is recommended.

Timing Chart

Fig. 16 shows the timing chart of LD6991. Note that the VDD must be larger than 0.9V, otherwise the reset signal will not operate correctly.

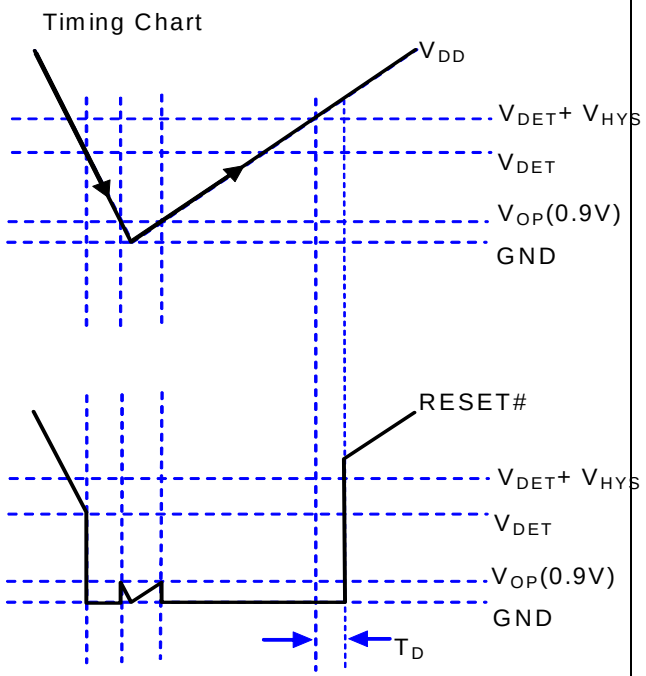
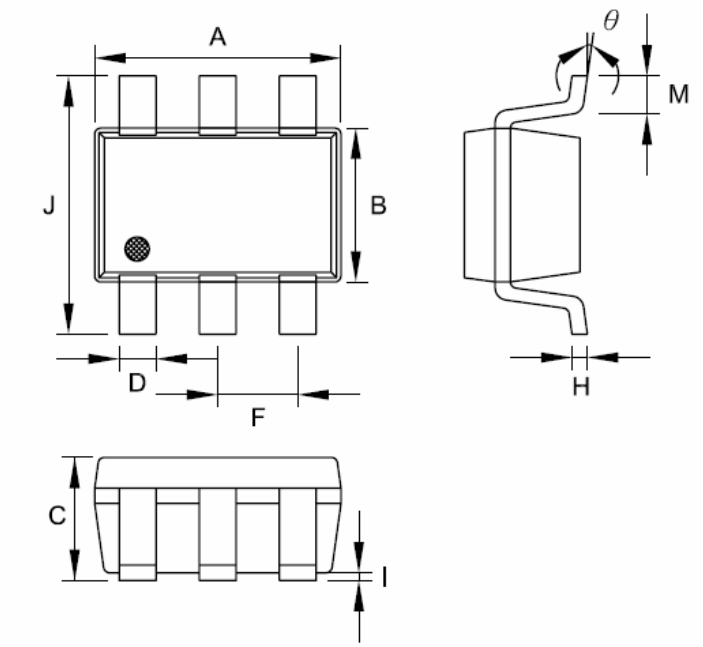


Fig.16 Timing chart of LD6991

Package Information

SC70-6



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.80	2.20	0.071	0.087
B	1.15	1.35	0.045	0.053
C	0.80	1.10	0.031	0.043
D	0.15	0.40	0.006	0.016
F	0.65 TYP.		0.026 TYP.	
H	0.08	0.25	0.003	0.010
I	0.00	0.10	0.000	0.004
J	1.80	2.40	0.071	0.094
M	0.10	0.46	0.004	0.018
θ	0°	12°	0°	12°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	9/20/2007	Original Specification.
01	10/17/2007	Modify typical application circuit
01a	11/13/2007	Marking system revision
01b	4/11/2008	Reset Output Voltage Low (Note): 0.6V Max