5-Channel DC-DC Converter with 1 Channel Shutter Driver

REV :00

General Description

The LD7241 includes 5-channel PWM DC/DC controller IC and a Shutter controller. It can operate at 1MHz frequency and built in ON/OFF control, soft-start, power on/off sequence and output overload protection.

Four channels have been integrated with MOSFETs and can achieve higher efficiency up to 90%~95% (CH1, CH2, CH3 and CH4). CH5 is a current source, ideally for 1WLED driver application. The LD7241 is also built with constant-current shutter driver. It optimizes overall efficiency and cost, and also reduces the board size.

The LD7241 is available in a space-saving 5mm*5mm 40-pin QFN package.

+ Patented

Features

- 1.5V to 5V Battery Input Range
- All Power Switches Integrated
- All channels built with internal compensation
- Synchronous step-down Converter
  - Efficiency up to 95%
  - Duty Cycle up to 100%
- Synchronous Step-up Converter
  - Efficiency up to 95%
  - Output Overvoltage Protection
  - Truly disconnected from output during shutdown
- 1 WLED Driver application
  -1KHz~50KHz PWM dimming
- CH2 Buck or Boost Configuration Selection
- Built-in Charge pump to enhance CH3/CH4 PMOS gate driving capacity
- Built-in Constant Current Shutter Driver
- Fixed 1MHz Operating Frequency
- Shutdown current :2.5μA (typ)

Applications

- Digital Video Camera, Digital Still Camera

Typical Application

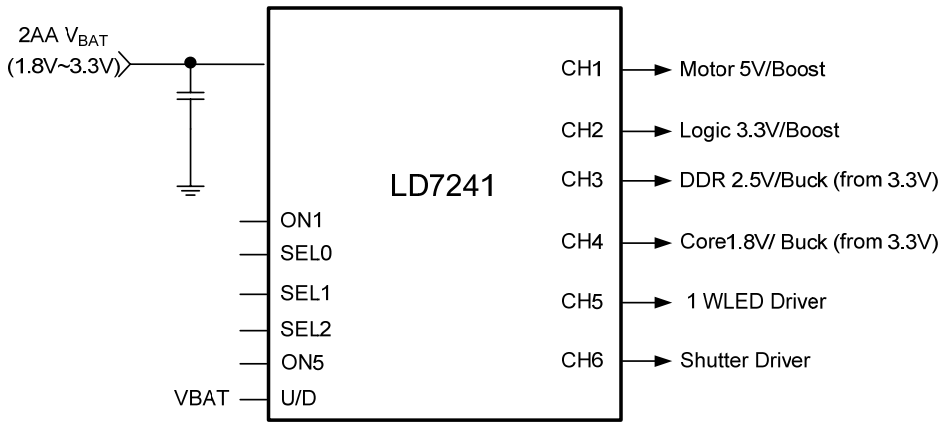


Fig.1

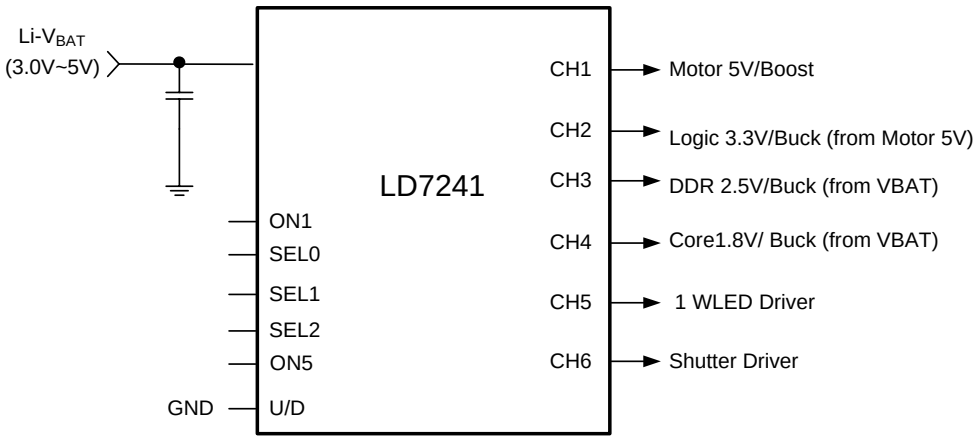


Fig.2

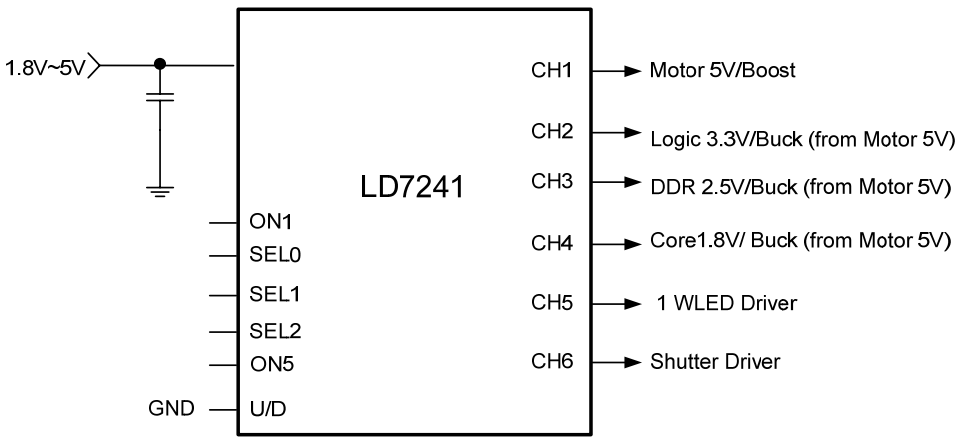
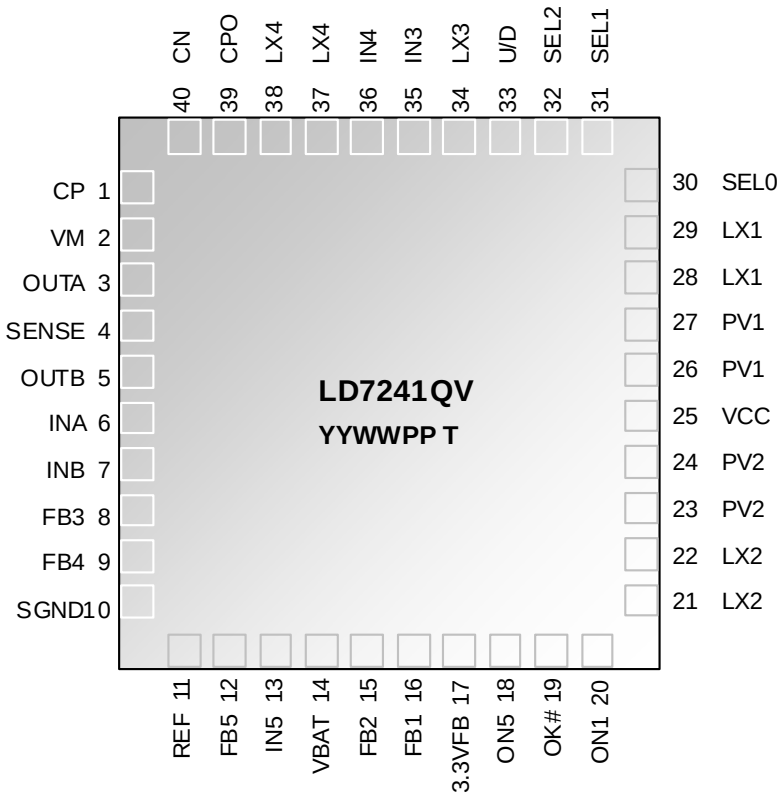


Fig.3

Pin Configuration



YY: Year code
WW: Week code
PP: Production code
T: Thickness
V: 0.85~0.9mm
W: 0.75mm (normal)
U: 0.55mm
X: 0.4mm

Ordering Information

Part number	Package		TOP MARK	Shipping
LD7241 GQVW	QFN -40	Green Package	LD7241QV(W)	2500/Tape & Reel

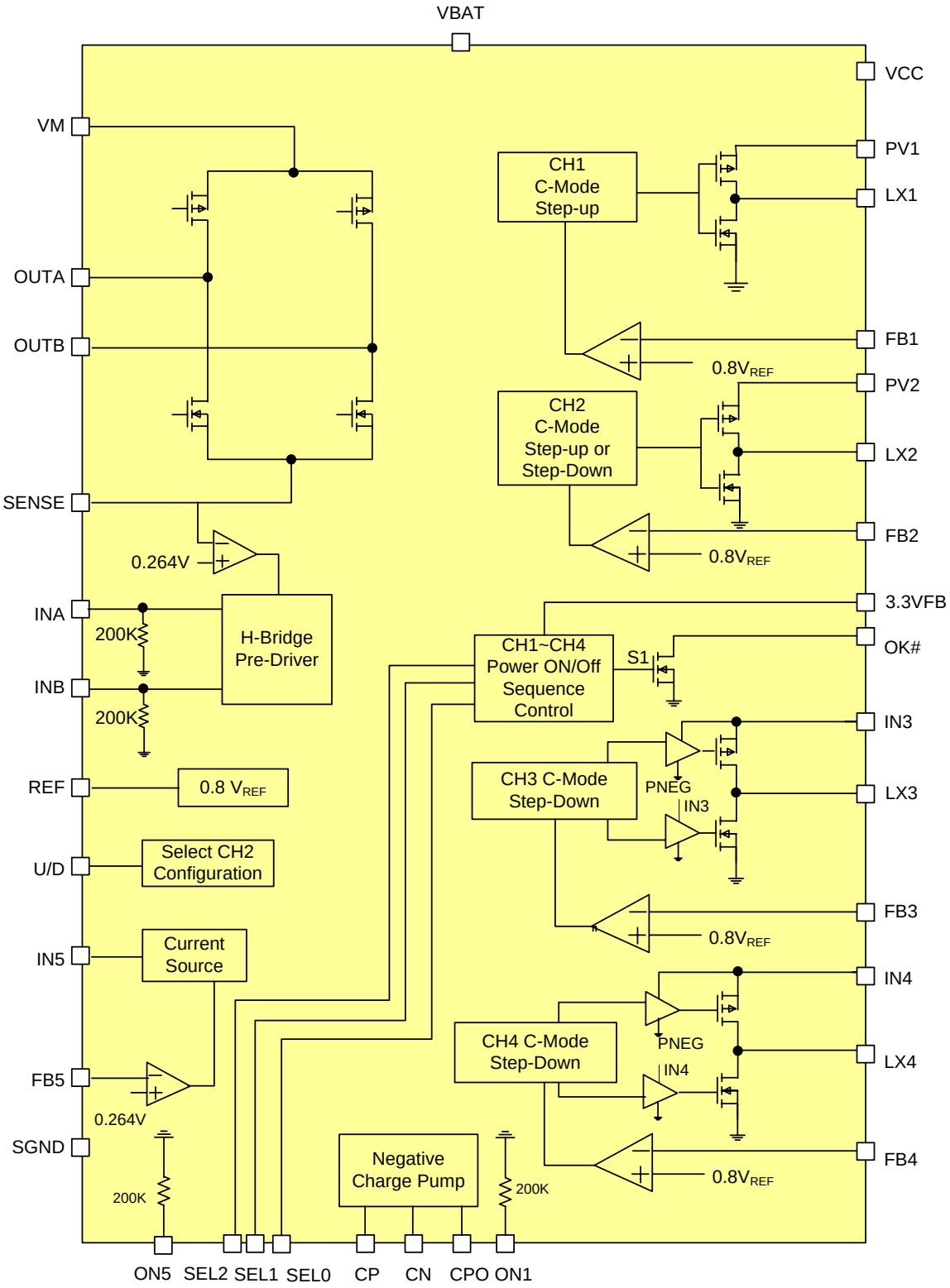
The LD7241 is ROHS compliant.

Pin Descriptions

PIN	NAME	FUNCTION
1	CP	Charge Pump external driver pin
2	VM	Power supply for driver
3	OUTA	H-Bridge output terminal A of the driver
4	SENSE	Current detection terminal for the shutter driver
5	OUTB	H-Bridge output terminal B of the driver
6	INA	It cooperates with INB to determine the state of shutter driver INA and INB pins are locked out until CH1 output reaches its determined value
7	INB	It cooperates with INA to determine the state of shutter driver INA and INB pins are locked out until CH1 output reaches its determined value
8	FB3	CH3 inverting input of error amplifier
9	FB4	CH4 inverting input of error amplifier
10	SGND	Signal GND. Connect PGND and SGND together at a single point on the PC board.
11	REF	0.8V reference. Bypass to SGND with 0.1μF ceramic capacitor.
12	FB5	CH5 inverting input of error amplifier
13	IN5	CH5 Converter input.
14	VBAT	VBAT pin. Bypass to power GND with at least 2*22μF ceramic capacitors.
15	FB2	CH2 inverting input of error amplifier
16	FB1	CH1 inverting input of error amplifier
17	3.3VFB	Sense Pin of CH2 output. High Impedance in shutdown
18	ON5	CH5 On/Off control. ON5 pin is locked out until the CH1 output reaches its determined value.
19	OK#	Open drain, active low signal. The status of OK# signal is acting according to SEL1and SEL2. Please refer to power on/off sequence section.
20	ON1	CH1 On/Off control. ON5, INA and INB pins are locked out until the CH1 output reaches its determined value.
21	LX2	CH2 Converter Switching Node. Pin 21 and 22 should be connected together.
22	LX2	CH2 Converter Switching Node. Pin 21 and 22 should be connected together.
23	PV2	CH2 is configured as a step-up converter and PV2 is the output. (U/D= VBAT) CH2 is configured as a step-down converter and PV2 is the input. (U/D= GND), Bypass to PGND with a 1μF ceramic capacitor.

PIN	NAME	FUNCTION
24	PV2	CH2 is configured as a step-up converter and PV2 is the output. (U/D=VBAT) CH2 is configured as a step-down converter and PV2 is the input. (U/D=GND), Bypass to PGND with a 1μF ceramic capacitor.
25	VCC	Input power of IC. Bypass to SGND with at least a 1μF ceramic capacitor. Connect PV1 with VCC together.
26	PV1	CH1 Converter Output.
27	PV1	CH1 Converter Output.
28	LX1	CH1 Converter Switching Node. Pin 28 and 29 should be connected together.
29	LX1	CH1 Converter Switching Node. Pin 28 and 29 should be connected together.
30	SEL0	Combine with SEL1 and SEL2 to determine the power sequence mode or debug mode of CH1, CH2, CH3 and CH4. Logic state isn't changeable during operation
31	SEL1	Combine with SEL0 and SEL2 to determine the power sequence mode or debug mode of CH1, CH2, CH3 and CH4. Logic state isn't changeable during operation
32	SEL2	Combine with SEL0 and SEL1 to determine the power sequence mode or debug mode of CH1, CH2, CH3 and CH4. Logic state isn't changeable during operation.
33	U/D	Configure CH2 as a Step-up or Step-down Converter. Logic state isn't changeable during operation. If U/D is connected to VBAT, CH2 is configured as step up and PV2 as the converter output. If U/D is connected to GND, CH2 is configured as step down and PV2 as the converter input.
34	LX3	CH3 Converter Switching Node
35	IN3	CH3 Converter Input. Bypass to PGND with a 1μF ceramic capacitor.
36	IN4	CH4 Converter Input. Bypass to PGND with a 1μF ceramic capacitor.
37	LX4	LX4 Converter Switching Node. Pin 37 and 38 should be connected together.
38	LX4	LX4 Converter Switching Node. Pin 37 and 38 should be connected together.
39	CPO	Negative Output pin of charge pump
40	CN	Charge pump external driver pin
EP	PGND	Power GND (Exposed Metal Pad). Exposed pad should be soldered to PCB board with a larger area and connected to SGND by a single point.

Block Diagram



Absolute Maximum Ratings

VBAT, LX1, U/D, SEL1 and SEL2	-0.3V ~8V (Note)
ON_, VCC,VM, IN5, LX2, LX3 and LX4	-0.3V ~ 6.5V
(IN4+IPNEGI)	-0.3V ~ 6.5V
Other Pins	-0.3V ~(VCC+0.3V)
LX1 Current	5.0A
LX2 Current	4.0A
LX3 Current	2.6A
LX4, Current	2.6A
OUTA, OUTB Current	350mA
Package Thermal Resistance	51°C/W
Power Dispassion	1270mW
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10sec)	+260°C
ESD Level (Human Body Model)	2KV
ESD Level (Machine Model)	200V

Note: If IC is in OFF-state, those pins rating will reach up to 8V.

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(T_A = +25°C, V_{BAT}=PV2=IN3=IN4=3.6V, Vcc=PV1=VM=5V, EP=SGND=0V, C_{REF}=0.1μF unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
General					
Input Battery Voltage Range	(Note1)	1.5		5.5	V
Minimum Start-up Battery Voltage	CH1: I_{LOAD}<1mA,		1.5	1.6	V
Shutdown Supply Current into VCC and VABT	ON1=ON5=SEL0=SEL1=SEL2=0 VCC=V_{BAT}=3.3V		2.5	10	μA
ON/OFF Control					
ON_, SEL_,INA,INB	Enable, 1.6V<PV1=V_{CC}=V_{BAT}<5V	1.2			V
	Disable, 1.6V<PV1=V_{CC}=V_{BAT}<5V			0.5	V
ON_, INA, INB Impedance to GND			200		KΩ
Reference					
Reference Output Voltage	I_{REF}=0mA	0.788	0.8	0.812	V
Oscillator					
OSC Frequency		0.9	1	1.1	MHz
CH1 DC-DC Converter (Boost)					
CH1 Voltage Adjust Range		3.3		5	V
FB1 Regulation Voltage		0.788	0.8	0.812	V
Soft Start Interval			4		mS
PV1 leakage current	LX1=0V, PV1=3.6V		0.1	5	μA
LX1 leakage current	LX1=3.6V		0.1	5	μA
CH1 Maximum Duty Cycle			90		%
Switch On-Resistance	NMOS		100		mΩ
	PMOS		150		mΩ
N-Channel Current limit			3.75		A
P-Channel Turn-off Current			20		mA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CH2 DC-DC Converter (Boost, U/D=VBAT)					
CH2 Voltage Adjust Range		3.3		5	V
FB2 Regulation Voltage		0.788	0.8	0.812	V
Soft Start Interval			4		mS
PV2 leakage current	LX2=0V, PV2=3.6V		0.1	5	μA
LX2 leakage current	LX2=3.6V		0.1	5	μA
CH2 Maximum Duty Cycle			90		%
Switch On-Resistance	NMOS		100		mΩ
	PMOS		150		mΩ
N-Channel Current limit			2.6		A
P-Channel Turn-off Current			20		mA
CH2 DC-DC Converter (Buck, U/D=GND)					
Maximum Duty Cycle				100	%
Soft Start Interval			4		mS
PV2 Leakage Current	LX2 =0V, PV2= 3.6V		0.1	5	μA
LX2 Leakage Current	LX2 = 3.6V		0.1	5	μA
FB2 Regulation Voltage		0.788	0.8	0.812	V
Switch On-Resistance	NMOS		100		mΩ
	PMOS		150		mΩ
P-Channel Current limit			2.6		A
N-Channel Turn-off Current			20		mA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CH 3 DC-DC Converter (Buck)					
Maximum Duty Cycle				100	%
Soft Start Interval			2		mS
IN3 Leakage Current	LX3=0V, IN3= 3.6V		0.1	5	μA
LX3 Leakage Current	LX3 =3.6V		0.1	5	μA
Switch On-Resistance	NMOS		200		mΩ
	PMOS		200		mΩ
P-Channel Current limit			1.2		A
N-Channel Turn-off Current			20		mA
FB3 Regulation Voltage		0.788	0.8	0.812	V
CH4 DC-DC Converter (Buck)					
Maximum Duty Cycle				100	%
Soft Start Interval			2		mS
IN4 Leakage Current	LX4 =0V, IN4= 3.6V		0.1	5	μA
LX4 Leakage Current	LX4 =3.6V		0.1	5	μA
FB4 Regulation Voltage		0.788	0.8	0.812	V
Switch On-Resistance	NMOS		150		mΩ
	PMOS		200		mΩ
P-Channel Current limit			1.2		A
N-Channel Turn-off Current			20		mA
Negative Charge Pump					
IN4 Low Threshold to Start Charge Pump			3.6		V
(IN4+IPNEGI) Clamped Voltage			4.3		V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CH 5 WLED Driver					
Input Voltage			-	5.5	V
Feedback Reference		0.25	0.264	0.278	V
Dropout Voltage	I_{LOAD} =20mA@Vgs=3.6V	-	0.1	0.15	V
Output Current Limit		40	70		mA
PWM Dimming Frequency		1		50	KHz
CH 6 Shutter Driver					
VM power supply		2.5		5.5	V
VM supply current at stand by	INA=INB=0, No load, VM=3.6V		0.5	2	μA
Output On resistance	Io=200mA, Sum of Resistance@ Vcc=3.3V		1.5		Ω
SENSE pin voltage			0.264		V
Output current	R_{SENSE}=1.2Ω, V_{SENSE}=0.264V	209	220	231	mA
Protection					
PV1and PV2 overvoltage protection		6.0	6.2	6.5	V
VBAT Pin overvoltage protection		6.0	6.2	6.5	V
VBAT Pin overvoltage detection blanking time			2		mS
Thermal Shutdown			150		°C

Note 1: The IC is powered from VCC pin.

Typical Performance Characteristics (Reference are Application Circuits)

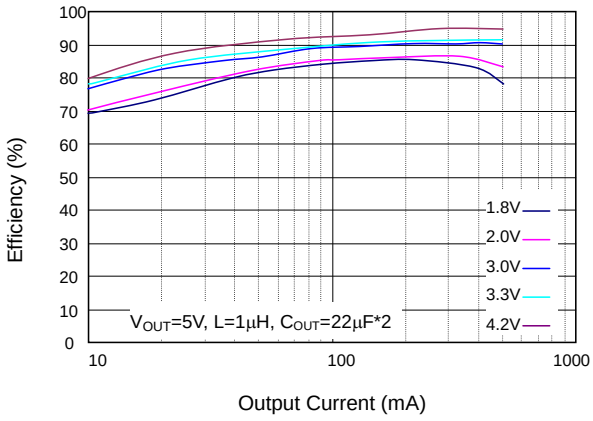


Fig. 4 CH1 Boost Efficiency vs. Output Current

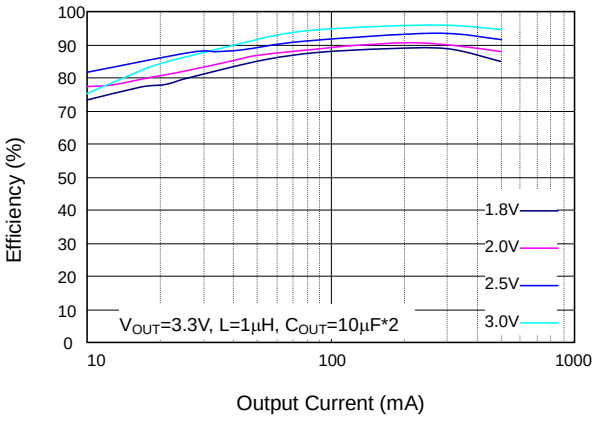


Fig. 5 CH2 Boost Efficiency vs. Output Current

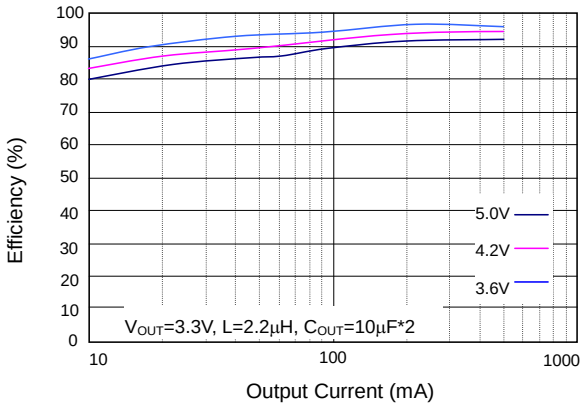


Fig. 6 CH2 Buck Efficiency vs. Output Current

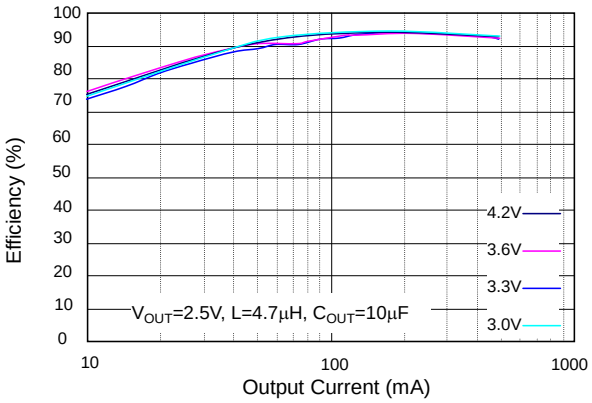


Fig. 7 CH3 Buck Efficiency vs. Output Current

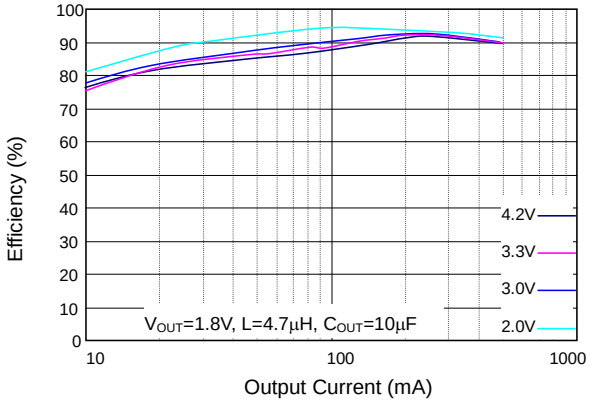


Fig. 8 CH4 Buck Efficiency vs. Output Current

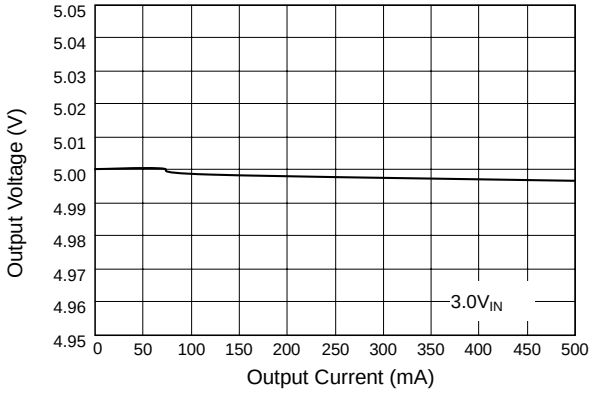


Fig. 9 CH1 Boost Output Voltage vs. Output Current

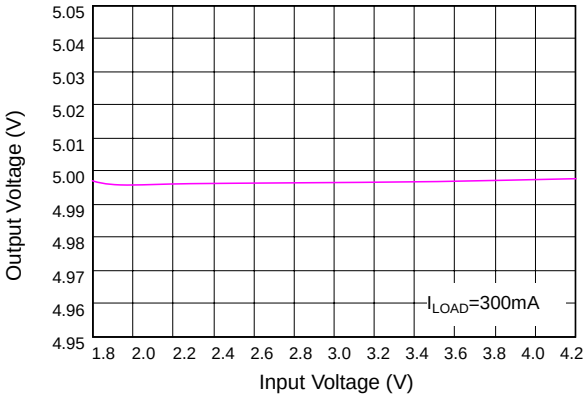


Fig. 10 CH1 Boost Input Voltage vs. Output Voltage

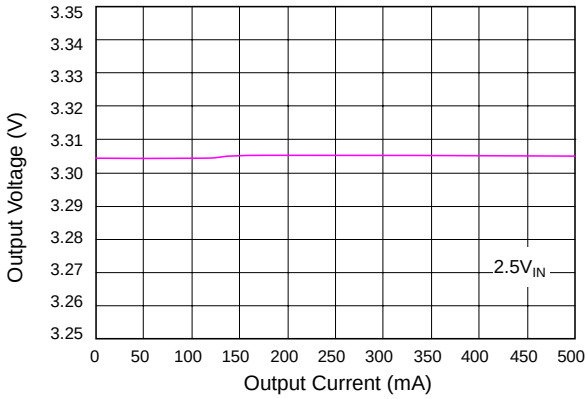


Fig. 11 CH2 Boost Output Voltage vs. Output Current

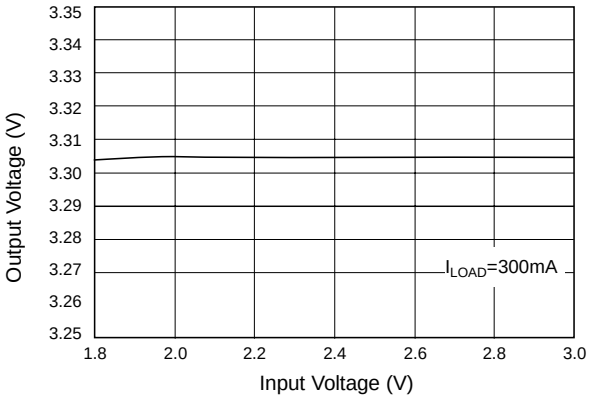


Fig. 12 CH2 Boost Input Voltage v.s Output Voltage

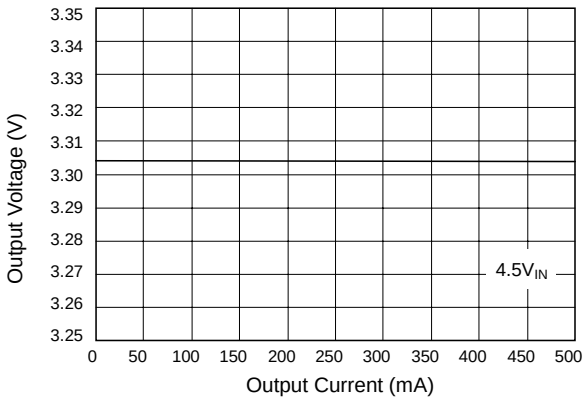


Fig. 13 CH2 Buck Output Voltage vs. Output Current

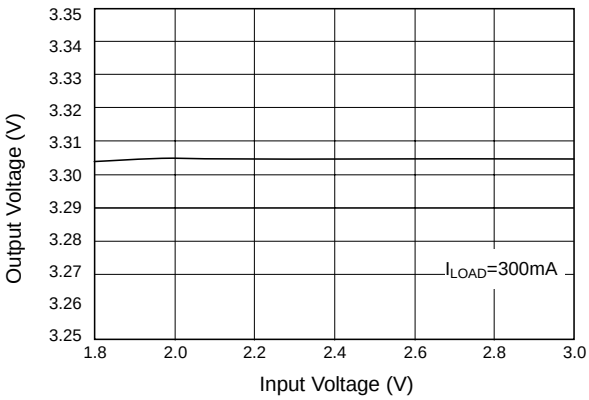


Fig. 14 CH2 Buck Input Voltage vs. Output Voltage

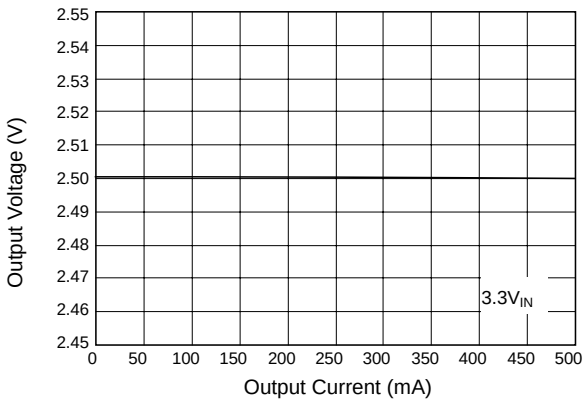


Fig. 15 CH3 Buck Output Voltage vs. Output Current

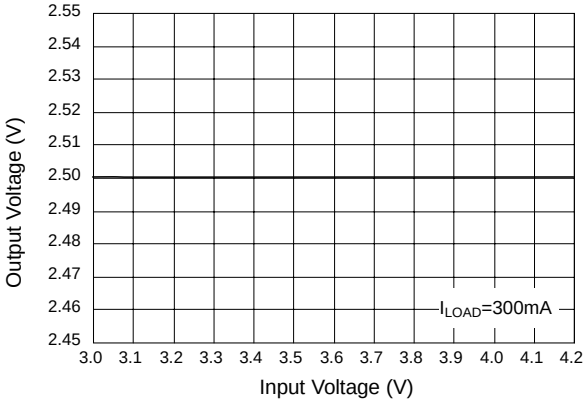


Fig. 16 CH3 Buck Input Voltage v.s Output Voltage

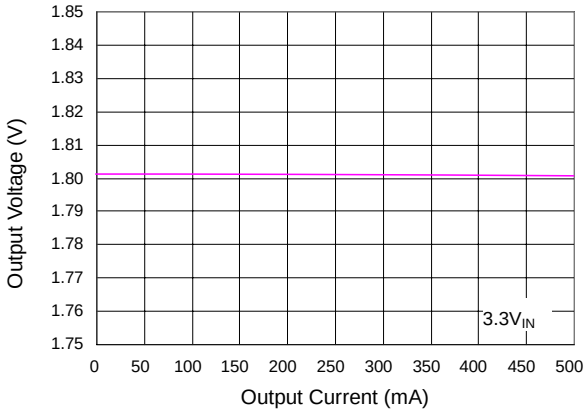


Fig. 17 CH4 Buck Output Voltage vs. Output Current

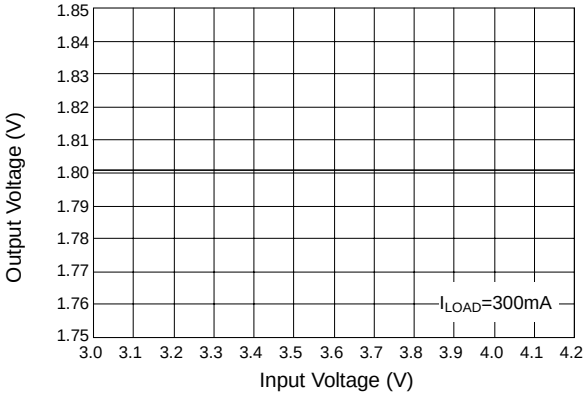


Fig. 16 CH4 Buck Input Voltage vs. Output Voltage

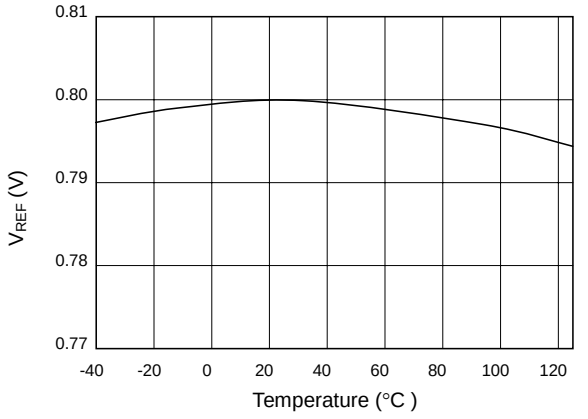


Fig. 19 T_C of V_{REF}

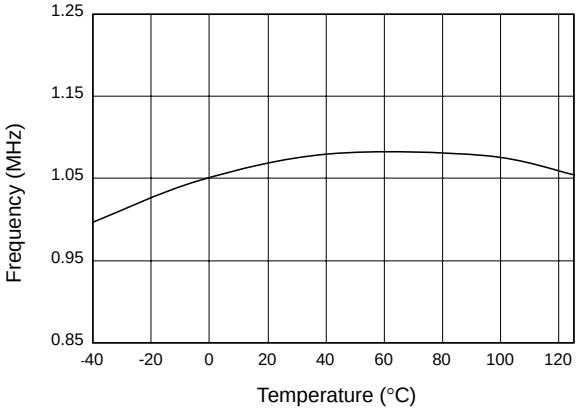


Fig. 20 Tc of Frequency

Typical Application Schematic

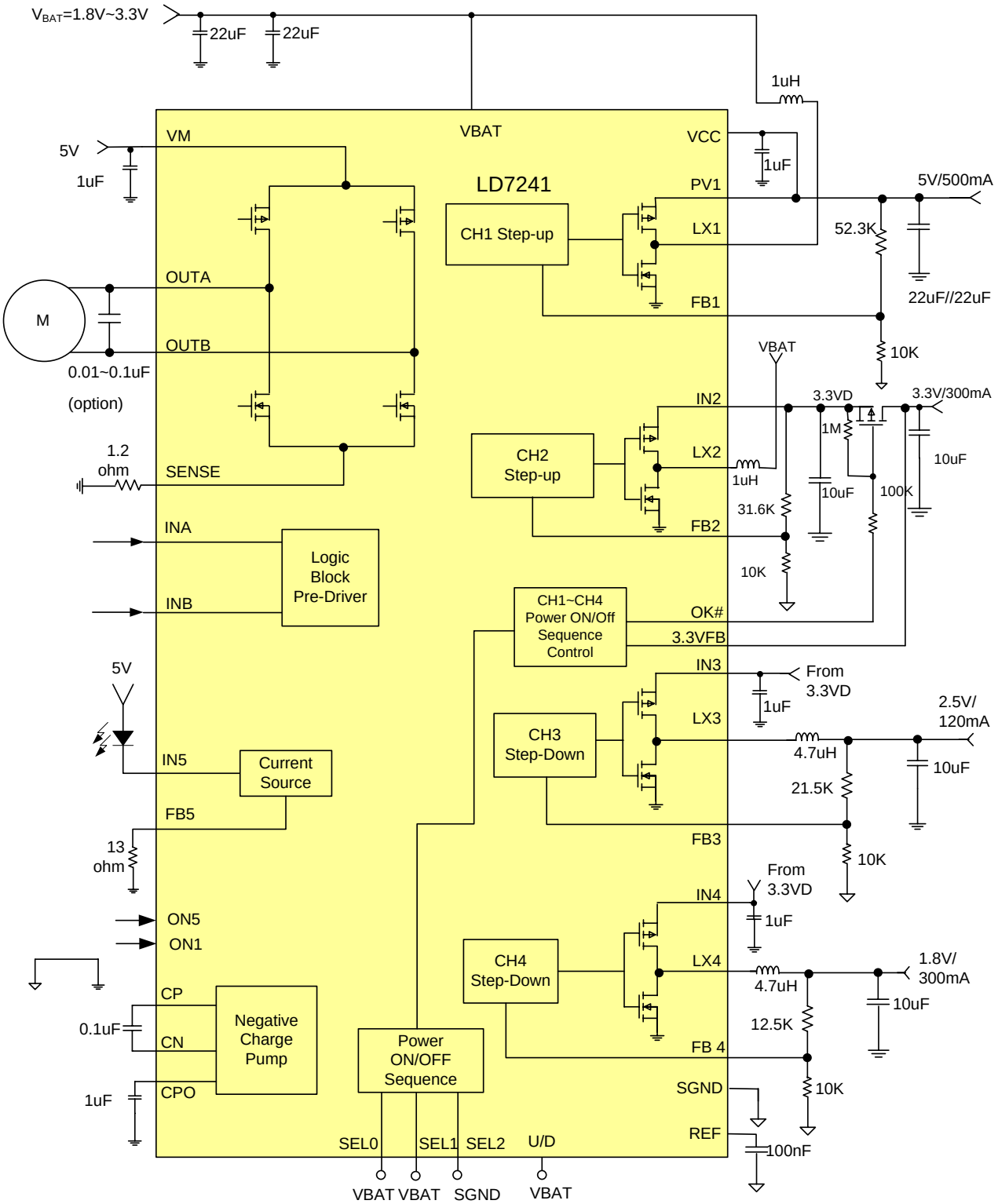


Fig.21 The Application for 2AA Battery

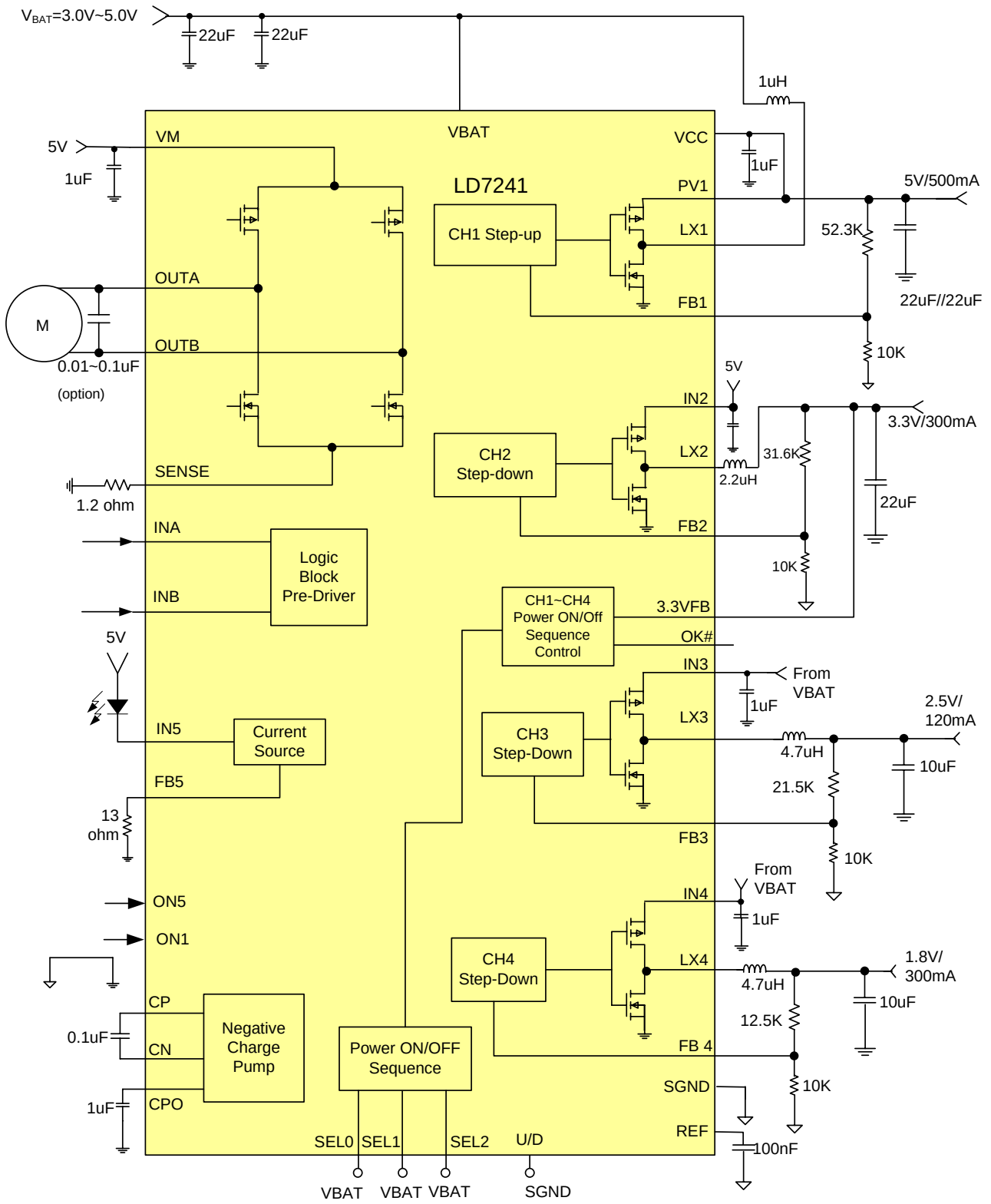


Fig.22 The Application for Li Battery

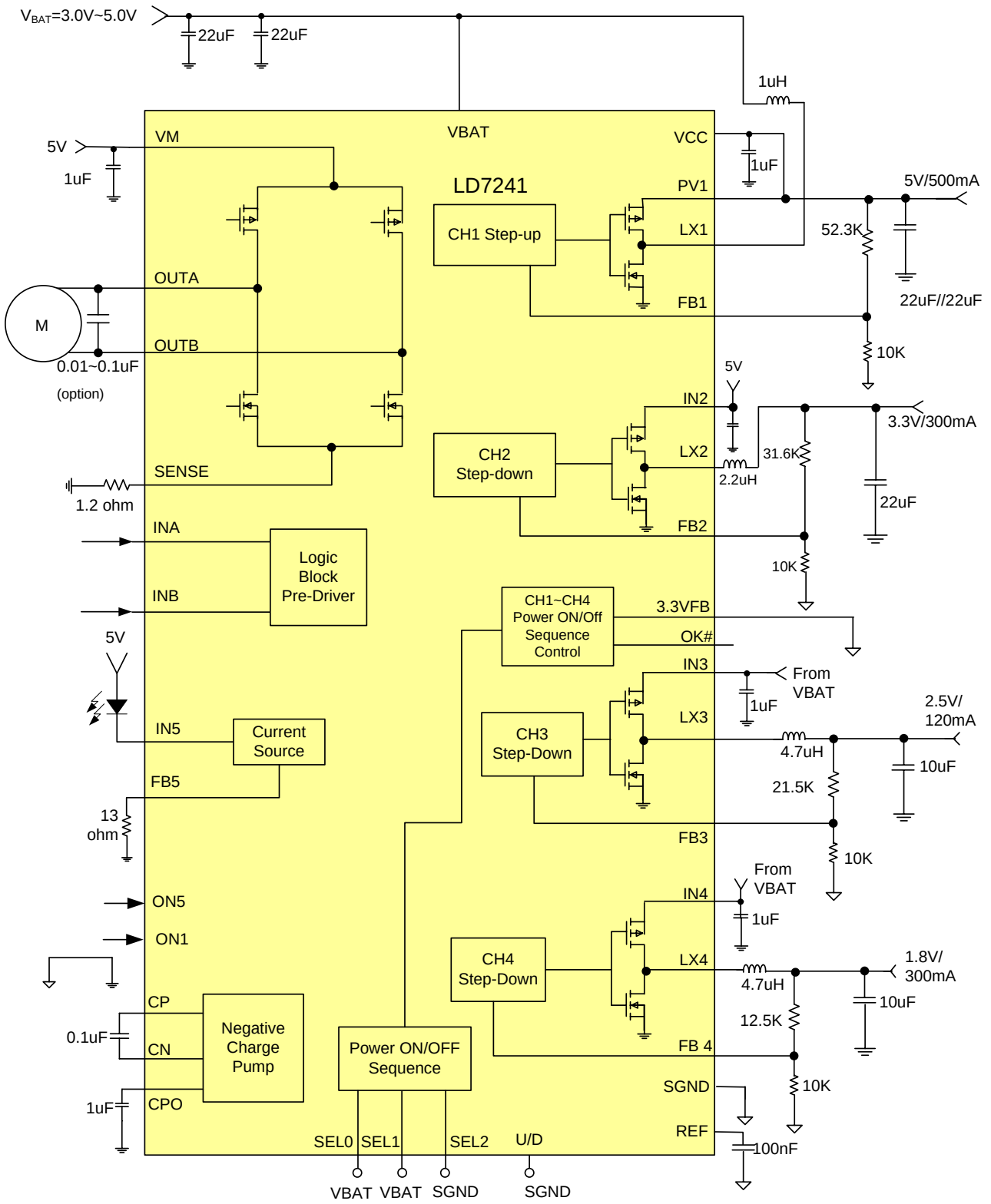


Fig.23 The Application for Li Battery

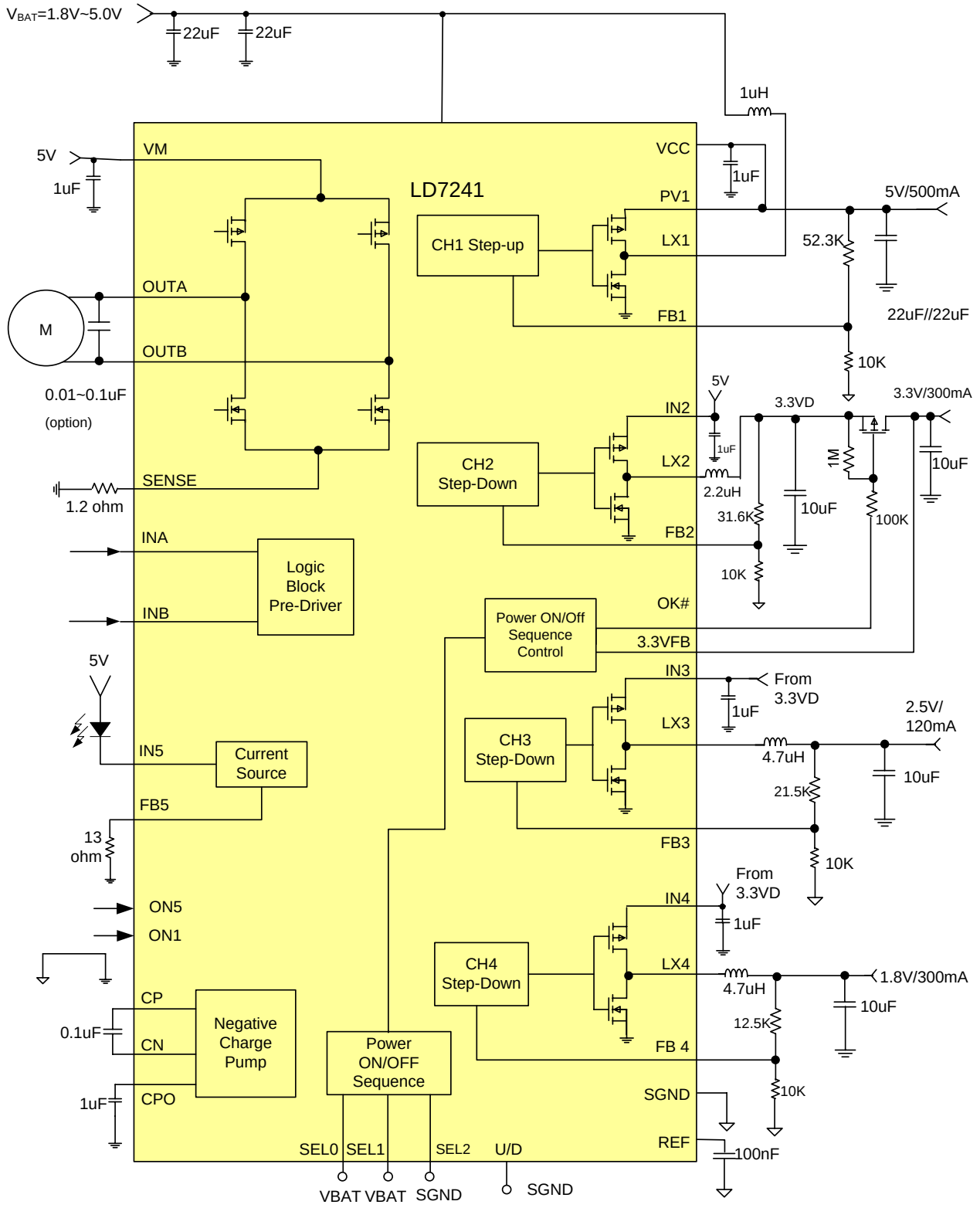


Fig.24 The Application for VBAT=1.8V~5V

Application Information

Operation Overview

The LD7241 provides a complete power supply solution for Digital Video camera application. The LD7241 includes 5 Channel DC-DC converters and a constant current driver for shutter control.

For 1-cell Li-ion battery application (U/D=GND):

CH1: Step-up DC-DC Converter with on-chip MOSFET – It typically supplies 5V for Motor voltage.

CH2: Step-down DC-DC Converter with on-chip MOSFET –It typically supplies 3.3V for logic power.

CH3: Step-Down DC-DC Converter with on-chip MOSFET–It typically supplies 2.5V for DDR power.

CH4: Step-Down DC-DC Converter with on-chip MOSFET –It typically supplies 1.8V for core power.

CH5: Current Source Controller –It is typically used for 1 WLED Driver.

CH6: Constant current driver for Shutter control

For 1-cell 2AA batteries application (U/D=VBAT)

CH1: Step-up DC-DC Converter with on-chip – It typically supplies 5V for Motor driver.

CH2: Step up DC-DC Converter with on-chip – It typically supplies 3.3V for logic power.

CH3: Step-Down DC-DC Convert with on-chip MOSFET –It typically supplies 2.5V for DDR power.

CH4: Step-Down DC-DC Converter with on-chip MOSFET –It typically supplies 1.8V for core power.

CH5: Current Source Controller –It is typically used for 1 WLED Driver.

CH6: Constant current driver for Shutter control

CH1 Step-Up DC-DC Converter

CH1 operates as a Boost-type configuration.

Connect VCC to PV1. Once the VCC pin voltage exceeds 2.7V, the IC would be powered from VCC other than VBAT. All other outputs would be therefore locked out until CH1 reaches its regulation voltage.

CH2 Step- Up DC-DC Converter (U/D=VBAT)

The Step-Up DC-DC converter channel is optimized for generating output voltages up to 5V. An internal switch and synchronous rectifier enable it to achieve conversion efficiency up to 90%. Such design reduces both circuit size and the number of external components.

CH2 Step down DC-DC Converter (U/D=GND)

The Step-Down DC-DC converter channel is optimized for generating output voltages down to 0.8V. An internal switch and synchronous rectifier allow conversion efficiency up to 95% while reducing both circuit size and the number of external components. The maximum duty cycle could be up to 100%.

CH3 Step- Down DC-DC Converter

The Step-Down DC-DC converter channel is optimized for generating output voltages down to 0.8V. An internal switch and synchronous rectifier enable it to achieve efficiency up to 95%. Such design reduces both circuit size and the number of external components. The maximum duty cycle could be up to 100%.

CH4 Step-Down DC-DC Converter

The Step-Down DC-DC converter channel is optimized for generating output voltages down to 0.8V. An internal switch and synchronous rectifier enable it to achieve conversion efficiency up to 95%. Such design reduces both circuit size and the number of external components. The maximum duty cycle could be up to 100%.

Negative Charge Pump

The negative charge pump is enabled when ON1 is active high. The charge pump circuit provides negative drive voltage for CH3 and CH4. This enhances PMOS gate driver capacity of CH3 and CH4. The negative voltage is clamped by (IN4+IPNEGI) <4.3V. **Note that the voltage of PNEG is determined by IN4, thus user should further check the IN3 voltage to keep (IN3+IPNEGI) <6V in all applications.**

CH5 Current Source Driver

The CH5 is a current source topology with feedback thresholds of 0.264V. Fig. 25 shows the 1WLED driver applications. ON5 input can also be driven by a logic-level PWM brightness control signal. The acceptable PWM dimming frequency is from 1 KHz to 50KHz.

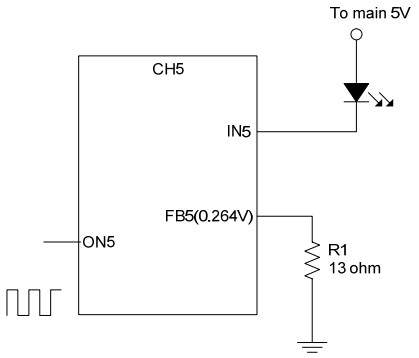


Fig. 25 1 WLED driver application

CH6 H-Bridge Shutter Driver

The driver current is adjustable by an external resistor connected at SENSE pin.

$I_o = 0.264V/R_{SENSE}$

Input-Output Logic Table：CH6 Constant Current Control for Shutter

Input		Output		Mode
INA	INB	OUTA	OUTB	MODE
L	L	Hi-Z	Hi-Z	Standby
H	L	H	L	Forward
L	H	L	H	Reverse
H	H	L	L	Brake

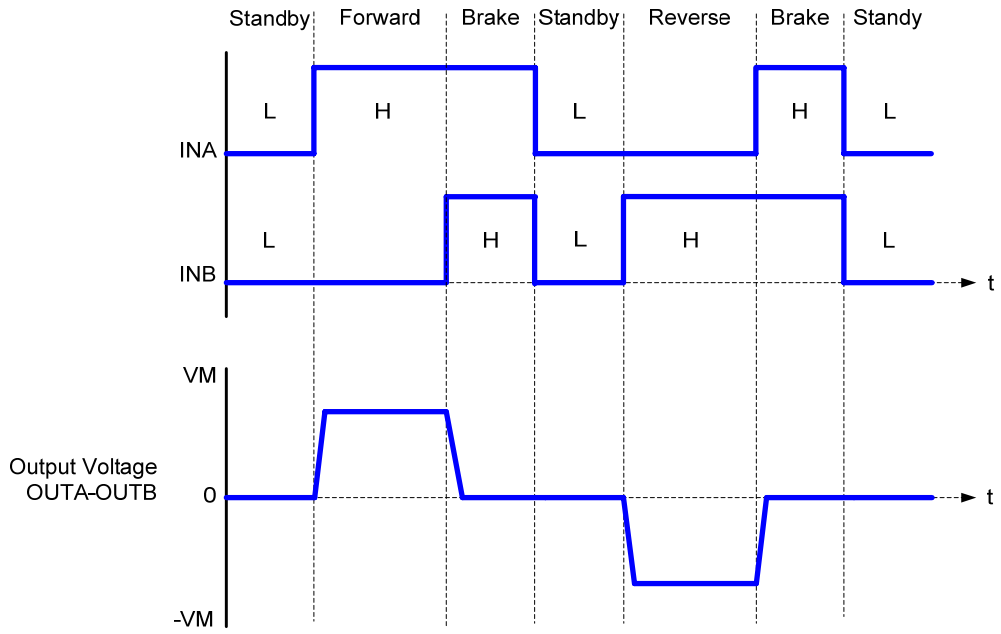


Fig. 26 Input-Output Waveform

CH1, CH2, CH3 and CH4 Power on/off Sequence Selection table

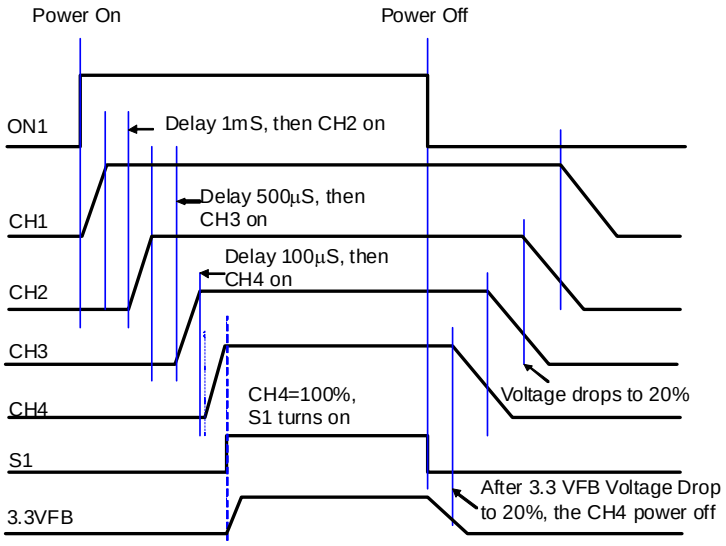
The LD7241 has a built-in power on/off sequence according to SEL0, SEL1 and SEL2 pins. Table 1-1 and Table 1-2 show the power on/off sequence selection table for the most applications. Please note that the SEL0, SEL1 and SEL 2 logic states are not changeable during operation.

SEL0	SEL1	SEL2	Power on sequence
1	1	0	CH1->CH2->CH3->CH4->S1
1	0	1	CH1->CH2->CH4->CH3->S1
0	1	1	CH1->CH2->CH3-> S1>CH4
1	1	1	CH1->CH3->CH4/S1->CH2

Table1-1

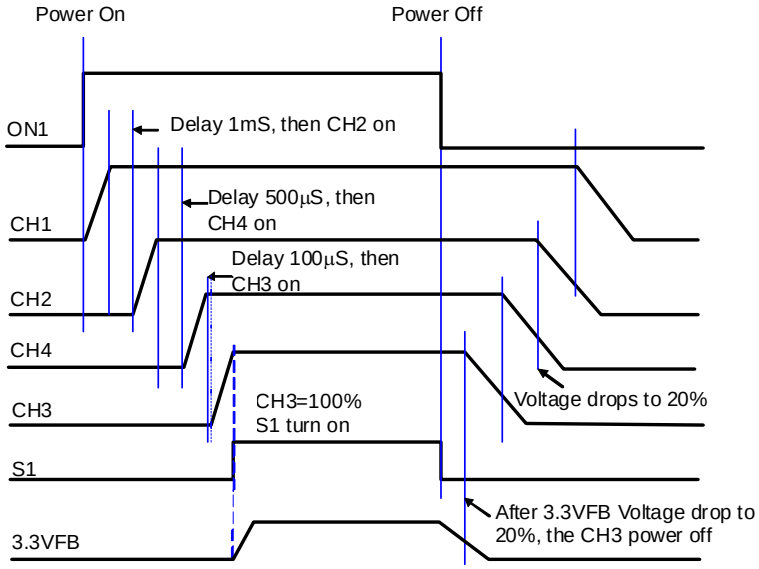
SEL0	SEL1	SEL2	Power off sequence
1	1	0	S1->CH4->CH3->CH2->CH1
1	0	1	S1->CH3->CH4->CH2->CH1
0	1	1	S1->CH4->CH3->CH2->CH1
1	1	1	S1->CH2->CH4->CH3->CH1

Table 1-2



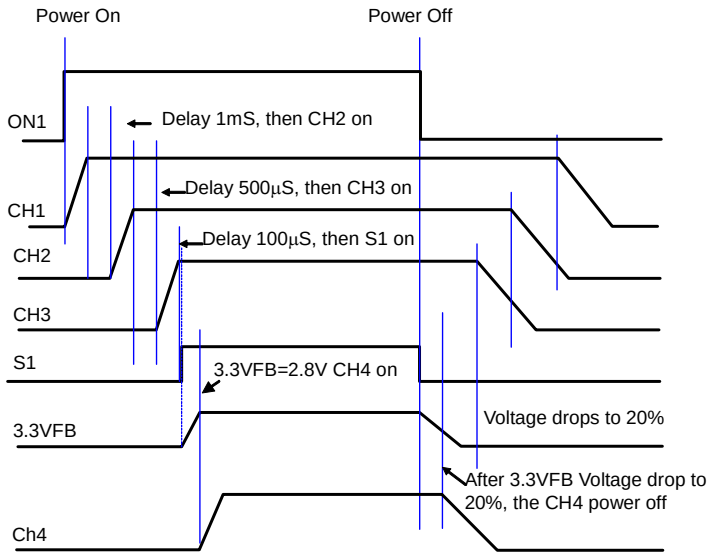
SEL0	SEL1	SEL2	
1	1	0	CH1->CH2->CH3->CH4->S1
			S1->CH4->CH3->CH2->CH1

Fig. 27 Power On/Off Sequence (SEL0=1, SEL1=1, SEL2=0)



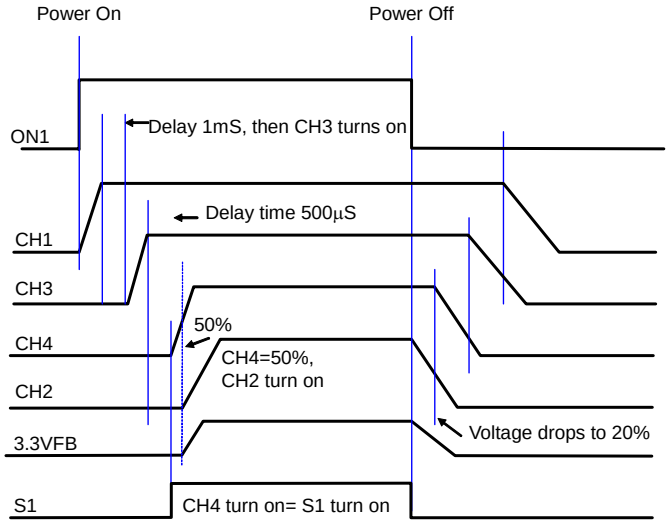
SEL0	SEL1	SEL2	
1	0	1	CH1->CH2->CH4->CH3->S1
			S1->CH3->CH4->CH2->CH1

Fig. 28 Power On/Off Sequence (SEL0=1, SEL1=0, SEL2=1)



SEL0	SEL1	SEL2	
0	1	1	CH1->CH2->CH3-> S1>CH4
			S1->CH4->CH3->CH2->CH1

Fig. 29 Power On/Off Sequence (SEL0=0, SEL1=1, SEL2=1)



SEL0	SEL1	SEL2	
1	1	1	CH1->CH3->CH4 / S1->CH2
			S1->CH2->CH4->CH3->CH1

Fig. 30 Power On/Off Sequence (SEL0=1, SEL1=1, SEL2=1)

Debug Mode

Table 1-3 shows the debug modes according to SEL0, SEL1 and SEL2 pins. Please note that the SEL0, SEL1 and SEL2 logic state are not changeable during operation

SEL0	SEL1	SEL2	CH2	CH3	CH4
0	0	0	OFF	OFF	OFF
1	0	0	ON	OFF	OFF
0	1	0	OFF	ON	OFF
0	0	1	OFF	OFF	ON

Table 1-3

Fault Protection

If any channel trips the level of over-current protection or short-circuit protection, all outputs will be latched off until CH1 is reset by the ON1 pin, or by cycling of input power. The fault detection circuit for each channel is disabled during its initial turn-on soft-start sequence.

Protection Summary

	Protection type	Threshold	Protection Methods	Reset Method
Thermal	OTP	T>150°C	All channels shut down	Reset by the ON1 pin, or by cycling of input power
VBAT	OVP	VBAT>6.2V	All channels shut down	Latch, until remove and plug in Battery again
VCC	UVLO	PV1<2.5V	All channels shut down	Reset by the ON1 pin, or by cycling of input power
CH1 Boost	Current Limit	NMOS current >3.75A	--	Reset at next cycle
	OVP	PV1>6.4V	NMOS and PMOS latched off, and all channels shut down	Reset by the ON1 pin, or by cycling of input power
CH2 Boost (U/D=GND)	Current Limit	NMOS current >2.6A	--	Reset at next cycle
	OVP	PV2>6.4V	NMOS and PMOS latched off, and all channels shut down	Reset by the ON1 pin, or by cycling of input power
CH2 Buck (U/D=VBAT)	Current Limit	PMOS Current >2.6A	--	Reset at next cycle
	SCP	FB2<0.4V	NMOS and PMOS latch off All channels shutdown	Reset by the ON1 pin, or by cycling of input power
CH3 Buck	Current limit	PMOS Current >1.2A	---	Reset at next cycle
	SCP	FB3<0.4V	NMOS and PMOS latch off All channels shutdown	Reset by the ON1 pin, or by cycling of input power
CH4 Buck	Current limit	PMOS Current >1.2A	---	Reset at next cycle
	SCP	FB4<0.4V	NMOS and PMOS latch off All channels shutdown	Reset by the ON1 pin, or by cycling of input power.

Soft-Start

The LD7241's channels feature the soft-start function that limits inrush current and prevents excessive battery loading during startup by ramping output voltage to the regulation voltage. This is achieved by increasing the internal reference inputs to the controller trans-conductance amplifiers from 0V to 0.8V reference voltage for over 4mS when initial power is applied or when a channel is enabled.

Reference

The LD7241 has an internal 0.8V reference. Please connect a 0.1μF ceramic bypass capacitor between REF and GND. REF can source up to 100μA, and it will be enabled when ON1 is high and PV1 is above 2.7V. During shutdown, REF is pulled to GND internally.

Inductor Selection

CH1, CH2, CH3 and CH4 are incorporated with internal loop compensation. For stable operation, please choose the inductance as shown in Table 2. Note that the peak current should be less than the saturation current of the inductor.

Channel	Inductance
CH1	1μH
CH2	1μH for Boost 2.2μH for Buck
CH3	4.7μH
CH4	4.7μH

Table2

Output Capacitor Selection

CH1, CH2, CH3 and CH4 are incorporated with internal loop compensation. For stable operation, please choose the minimum C_{OUT} as Table 3.

Channel	Minimum Output Capacitance
CH1	22μF//22uF
CH2	22μF
CH3	10μF
CH4	10μF

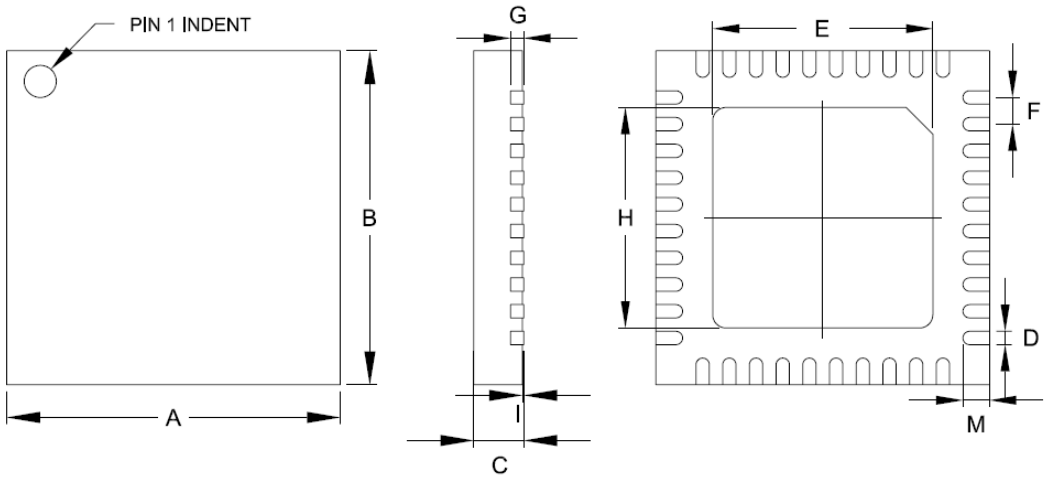
Table3

Layout Consideration

1. Keep the bypass capacitor 1μF very close to IC. (<5mm)
2. Keep the bypass capacitor 0.1μF very close to REF pin.
3. Keep output voltage feed back network very close to the IC.
4. Signal ground plane of FB pin and REF pin (small signal components) should be connected to the PGND (EP) plane with only one point to minimize the effect of power ground currents.
5. Switching nodes should be kept as small as possible and routed away from FB pin and REF pin.
6. The PCB traces carrying discontinuous currents and any high current path should be made as short and board as possible.
7. If possible, a multi-layer PCB is recommended. Please refer to the EV kit of LD7241 for a PCB layout example.

Package Information

QFN-40 (5mm x 5mm)



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	4.900	5.100	0.193	0.201
B	4.900	5.100	0.193	0.201
C	0.700	0.800	0.028	0.031
D	0.150	0.250	0.006	0.012
E	3.250	3.350	0.128	0.142
F	0.40 TYP.		0.016 TYP.	
G	0.20 REF.		0.008 TYP.	
H	3.250	3.350	0.128	0.142
I	0.000	0.050	0.000	0.002
M	0.350	0.450	0.013	0.018

Important Notice

Leadtrend Technology Inc. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	2008/10/20	Original Specification