# Smart Photoflash Capacitor Charger with Integrated MOS

***REV:01***

## General Description

The LD7265A is an ideal charge control IC for flash units with internal soft start, adjustable charging current and output voltage. It provides a proprietary charging algorithm to speed up the charging with more efficiency. The LD7265A operates in the constant peak current mode, while the peak current limit can be adjusted to eight different levels between 0.54A to 1.8A, by clocking the CHARGE Pin. As well, LD7265A separates the source and sink pin of IGBT driver, which enables the users to easily meet the requirement of any different IGBT application.

The LD7265A is available in a space-saving DFN10 package and is ideal for DSC flash unit.

† Patented

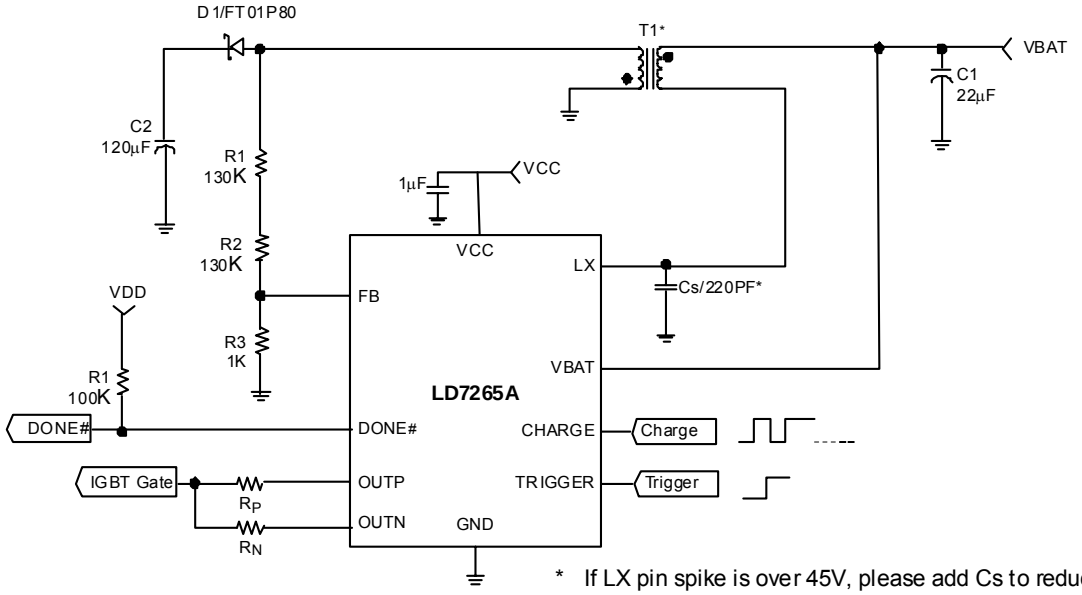
## Features

- Adjustable Output Voltage
- 1.8V~6V Battery Voltage Range
- Tiny Transformer
- Integrated 45V Power Switch
- Programmable eight-level Current Limit
- Separate Source and Sink Pin of IGBT Driver
- Output Voltage Overcharge Protection
- Lower Charging Current Drop Compensation

## Applications

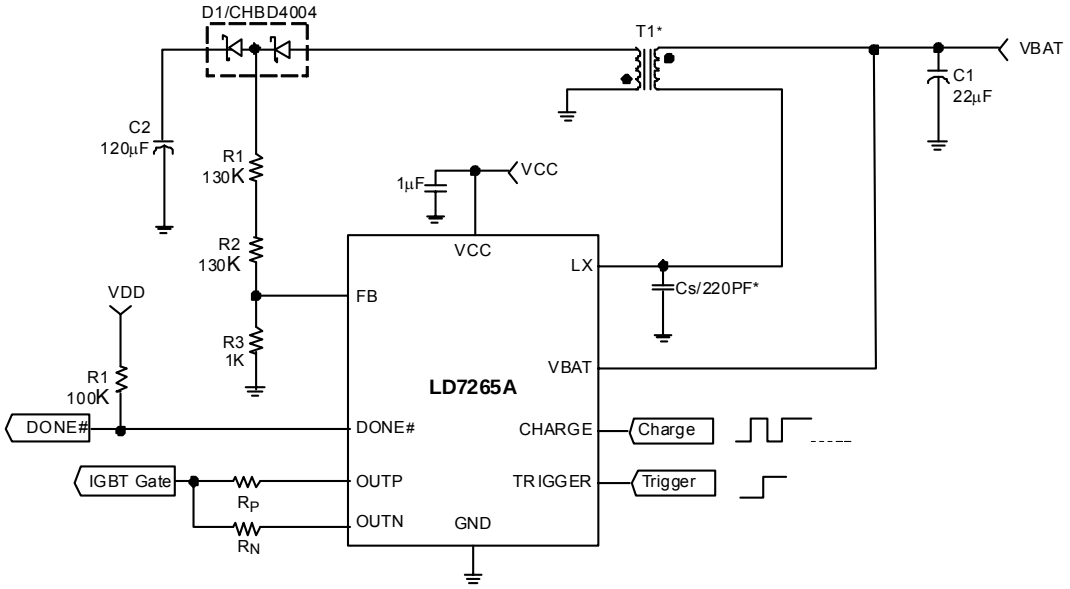
- DSC Flash Unit
- Cell Phone with Camera

## Typical Application



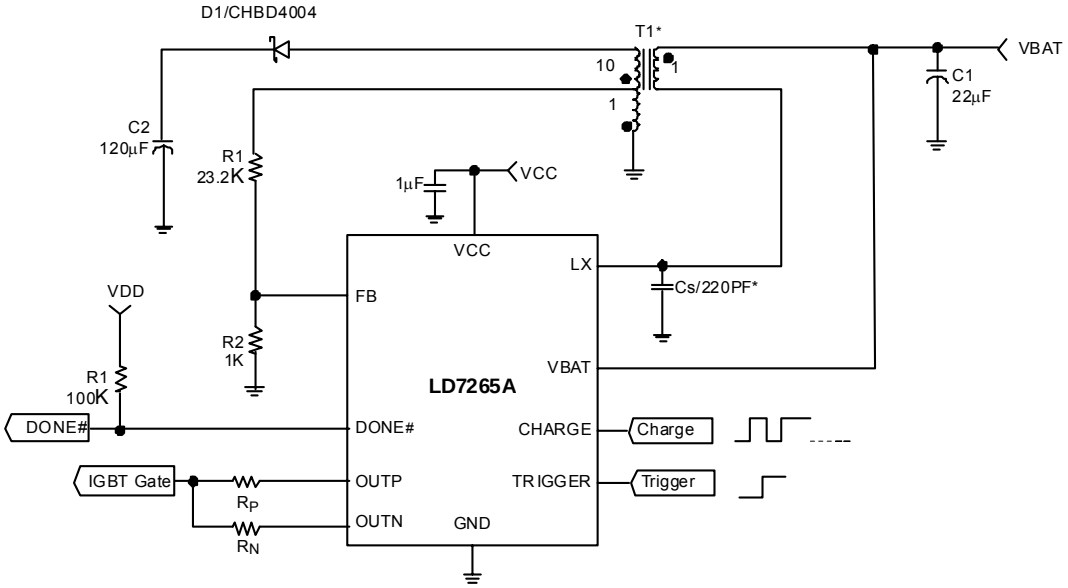

* If LX pin spike is over 45V, please add Cs to reduce spike. Cs< 220pF is recommended.

Fig.1




* If LX pin spike is over 45V, please add Cs to reduce spike.
Cs< 220pF is recommended.

Fig.2




* If LX pin spike is over 45V, please add Cs to reduce spike.
Cs< 220pF is recommended.

Fig.3

## Pin Configuration

DFN-10 (3mm x 3mm, W type)


YY: Year code
WW: Week code
PP: Production code
T: Thickness
V: 0.85~0.9mm
W: 0.75mm (normal)
U: 0.55mm
X: 0.4mm

## Ordering Information

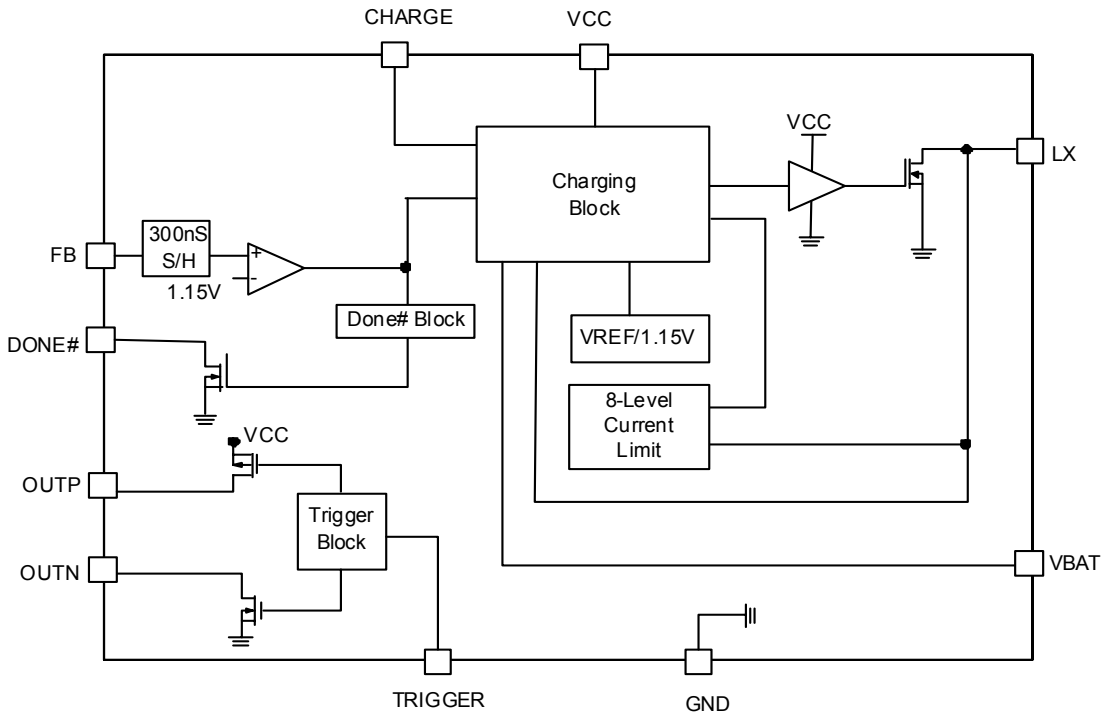
| Part number | Package | | Top Mark | Shipping |
|---|---|---|---|---|
| LD7265AGDHW | DFN-10 | Green Package | 7265AGDH(W) | 2500 /tape & reel |

Note: The LD7265A is ROHS compliant.

## Pin Descriptions

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | FB | Output voltage feedback |
| 2 | DONE# | Charge Done Indicator. DONE# is an open drain output that pulls low when CHARGE is high and the circuit has finished charging the output capacitor. |
| 3 | OUTP | IGBT driver source output Pin. |
| 4 | OUTN | IGBT driver sink output Pin. |
| 5 | GND | IC GND. |
| 6 | LX | NMOS drain pin. Connect to transformer primary as shown in Fig.1 |
| 7 | VCC | Input power of IC. Bypass with a 1μF ceramic capacitor close to IC GND. |
| 8 | VBAT | Battery Voltage Input |
| 9 | CHARGE | Charging on/off control and primary side peak current setting. |
| 10 | TRIGGER | Trigger on/off control. |
| - | EP | Exposed Metal Pad. Exposed pad should be soldered to PCB board and connected to power ground plane to achieve better thermal dissipation. |

## Block Diagram




## Absolute Maximum Ratings

| | |
|---|---|
| VCC and VBAT Pin | -0.3V~6.5V |
| FB pin | -0.45V~6.5V |
| Charge, Trigger, DONE#, OUTP and OUTN pin | -0.3V~6.5V |
| LX pin<200nS | -0.3V~45V |
| DC | -0.3V~40V |
| LX Current | 3.3A |
| Operating Temperature Range | -30°C to 85°C |
| Storage Temperature Range | -55°C to 125°C |
| Junction Temperature | 125°C |
| Lead Temperature (Soldering, 10sec) | 260°C |
| ESD Level (Human Body Model) | 2KV |
| ESD Level (Machine Model) | 200V |

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## Electrical Characteristics

($T_A$ = +25°C unless otherwise stated, $V_{CC}$=3.3V)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Input Power** | | | | | |
| Operating Voltage $V_{CC}$ | | 2.8 | | 5.5 | V |
| Shutdown Current $I_{CC}$ | Charge=Off, Trigger=Off | | | 1.5 | μA |
| Nominal Supply Current | $V_{CC}$=3.3V, D=50% | | 1 | | mA |
| **FB** | | | | | |
| Reference Voltage | | | 1.15 | | V |
| Reference Voltage Tolerance | | -1.5 | | +1.5 | % |
| Sample time of FB detection | | 270 | 300 | 330 | nS |
| **LX pin** | | | | | |
| Primary Side Current Limit- $I_{LIM1}$ | | 0.486 | 0.54 | 0.595 | A |
| Primary Side Current Limit- $I_{LIM2}$ | | | 0.72 | | A |
| Primary Side Current Limit- $I_{LIM3}$ | | | 0.90 | | A |
| Primary Side Current Limit- $I_{LIM4}$ | | | 1.08 | | A |
| Primary Side Current Limit- $I_{LIM5}$ | | | 1.26 | | A |
| Primary Side Current Limit- $I_{LIM6}$ | | | 1.44 | | A |
| Primary Side Current Limit- $I_{LIM7}$ | | | 1.62 | | A |
| Primary Side Current Limit- $I_{IM8}$ | Note | 1.62 | 1.80 | 1.98 | A |
| On resistance | $V_{cc}$=5V, $I_{LX}$=0.54A | | 270 | | mΩ |
| LX leakage current | $V_{LX}$=40V | | | 5 | μA |
| **IGBT Driver** | | | | | |
| OUTP Resistance | $V_{CC}$=3.3V | | 6 | 9 | Ω |
| OUTN Resistance | $V_{CC}$=3.3V | | 11 | 17 | Ω |
| Rising Time | $V_{CC}$=3.3V, $C_L$=3.9nF | | 90 | | nS |
| Falling Time | $V_{CC}$=3.3V, $C_L$=3.9nF | | 165 | | nS |
| **ON/OFF** | | | | | |
| Trigger On/Off | Enabled | 1.4 | | | V |
| | Disabled | | | 0.6 | V |
| Charge On/Off | Enabled | 1.4 | | | V |
| | Disabled | | | 0.6 | V |
| $I_{LIM}$ Clock High time at Charge Pin | Initial Pulse | 36 | | | μS |
| | Subsequent Pulses | 5 | | | μS |
| $I_{LIM}$ Clock Low time at Charge Pin | | 5 | | | μS |

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Total MAX clock pulse setup time | | | | 500 | μS |
| **Impedance to GND** | | | | | |
| Charge Pin to GND | | | 100K | | Ω |
| Trigger Pin to GND | | | 100K | | Ω |
| OUTP Pin to GND | | | 20K | | Ω |
| OUTN Pin to GND | | | 20K | | Ω |
| **Others** | | | | | |
| Thermal Shutdown | | | 150 | | °C |
| Max ON Time | | | 32 | | μS |
| Propagation Delay | (Trigger=High) delay to OUTP and OUTN | | 60 | | nS |

*Note: Current limit of level 8 is guaranteed by design.

## Typical Performance Characteristics

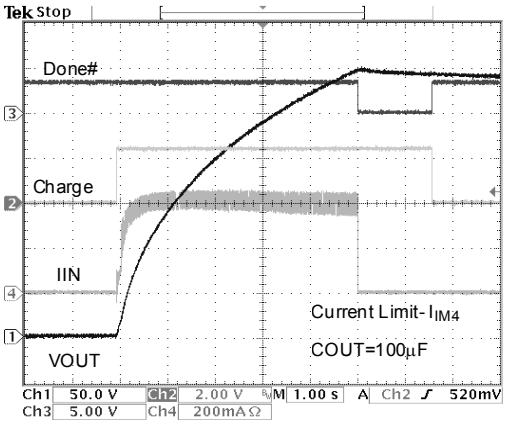



Fig.4 Charge Waveform $V_{BAT}$=3V

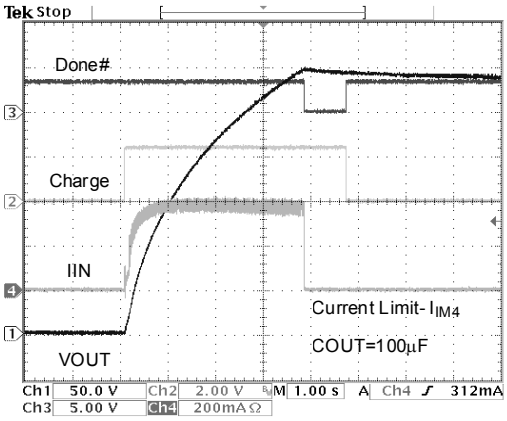



Fig.5 Charge Waveform $V_{BAT}$=4.2V

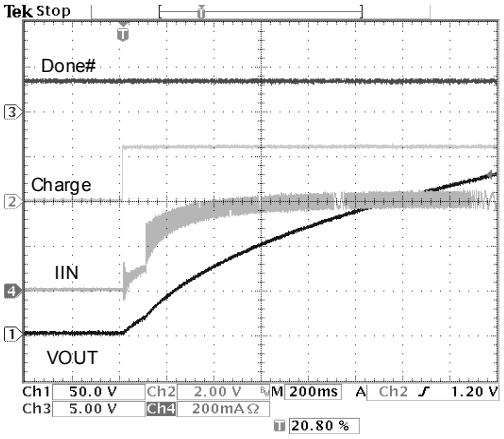



Fig.6 Soft Start Function

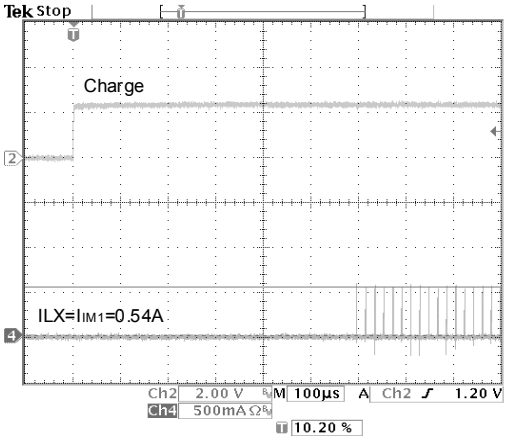



Fig.7 Primary Side Current Limit-$I_{IM1}$

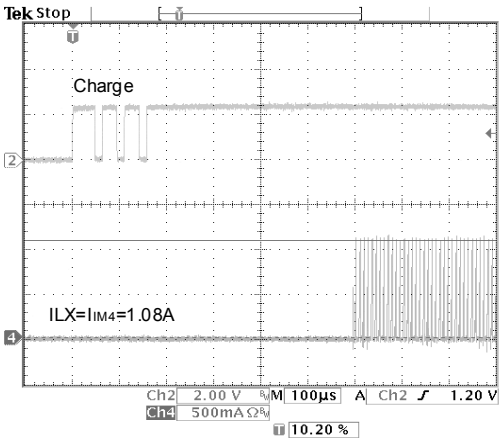



Fig.8 Primary Side Current Limit-$I_{IM4}$

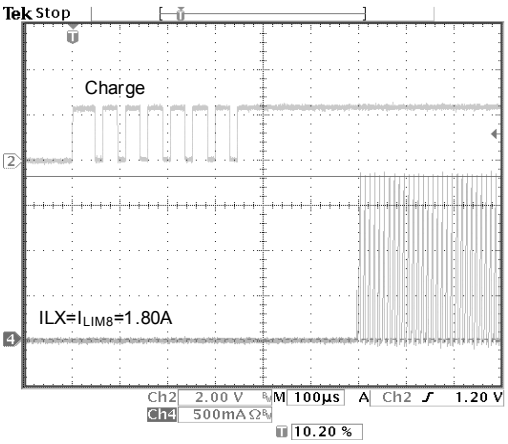



Fig.9 Primary Side Current Limit-$I_{IM8}$

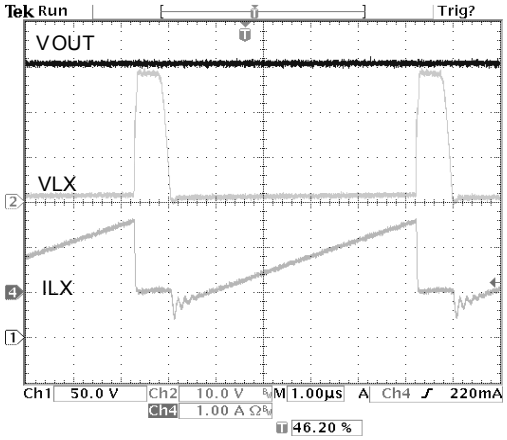



Fig.10 Typical Switching Waveform

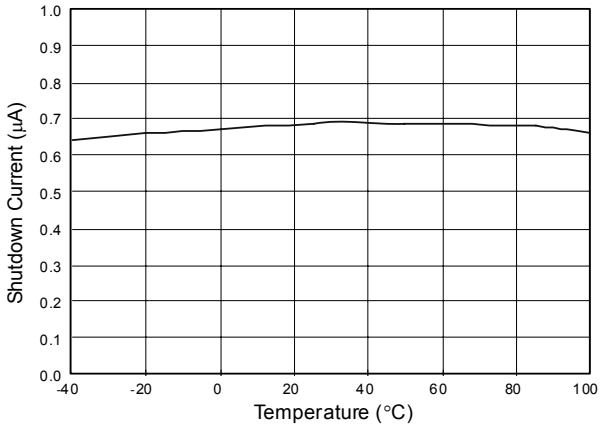



Fig.11 Shut Down Current vs. Temperature

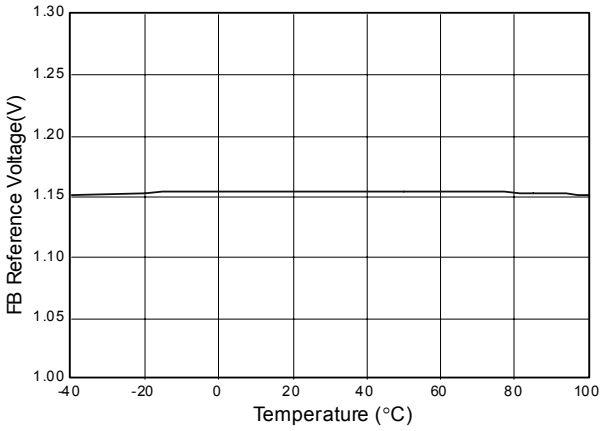



Fig.12 FB Reference Voltage vs. Temperature

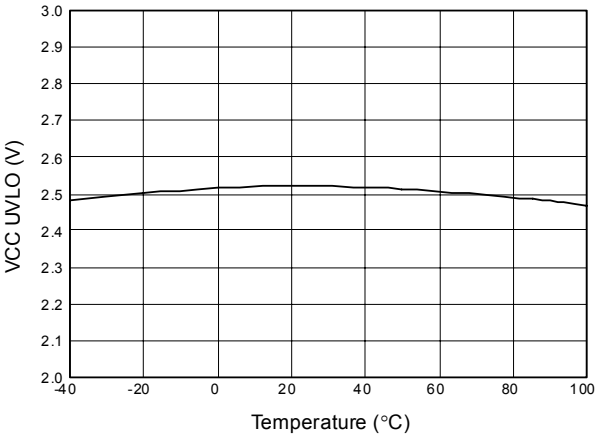



Fig.13 VCC UVLO vs. Temperature

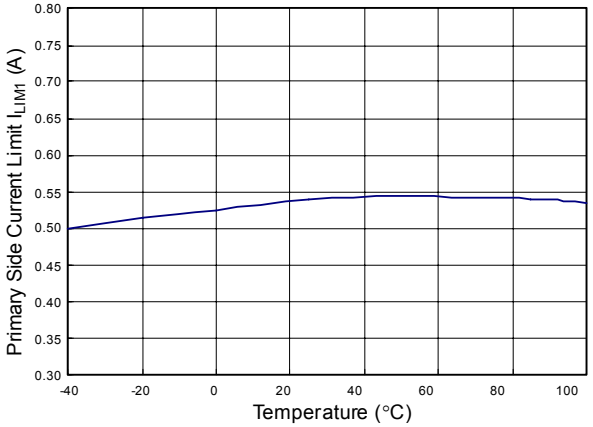



Fig.14 Primary Side Current Limit $I_{LIM1}$ vs. Temperature

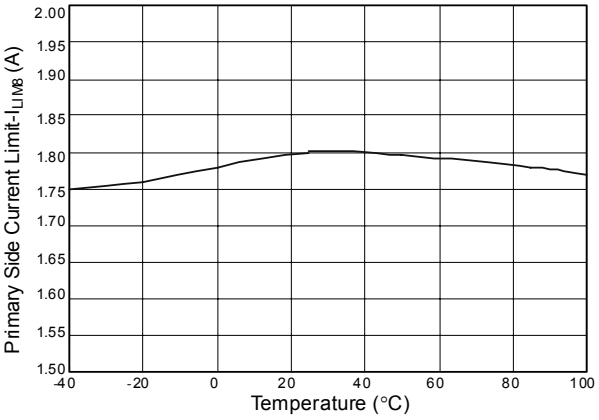



Fig.15 Primary Side Current Limit-Lim8 vs. Temperature

# Function Description

## Adjust Charging Current

The peak current can be adjusted to eight different levels, from 0.54A to 1.8A, by clocking the CHARGE Pin. The flexible scheme allows the users to design the flash circuit according to various input voltages. The battery life can be extended effectively by setting a lower current limit at low battery.

Fig.16 shows the $I_{LIM}$ clock timing protocol. The total $I_{LIM}$ setup time, $T_{ILIM(SU)}$, denotes the time required for the decoder circuit to receive CHARGE Pin clock inputs and to set $I_{LIM}$. The last low-to-high edge must arrive within 500μS from the first edge.

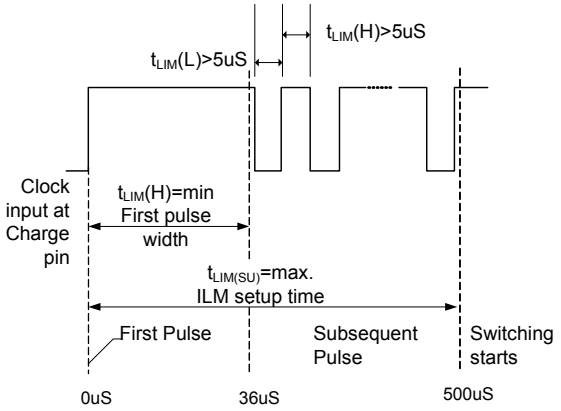



Fig. 16 $I_{LIM}$ Clock Timing Definition

The first rising edge starts the ILIM counter, and then up to 8 rising edges counted to set the ILIM level. The initial clock pulse must stay for at least 36μS, the subsequent pulses at least 5μS and the last low-to-high edge must arrive before 500μS from the first edge. If the high time or low time of clock pulse is not larger than the minimum value of spec., then the clock pulse may be ignored. The $I_{LIM}$ setting will remain effective as long as the CHARGE pin is high. To reset the ILIM counter, pull the CHARGE pin low before clocking the new setting. Fig.17 shows the example for setting at $I_{LIM4}$.

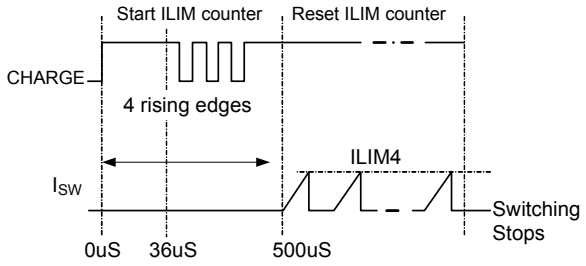



Fig. 17 Current Limiting Waveforms

Example for setting at $I_{LIM4}$

## Transformer Turn Ration

A carefully chosen transformer could result in best performance of the LD7265A. Also, the turning ratio of the transformer should be taken into consideration. The maximum voltage rating of the internal NMOS of the LD7265A is 45V. Thus, the turn ration is obtained by:

$$N \geq \frac{V_{OUT} + V_{D1}}{45 - V_{BATMAX} - V_{SPIKE}}$$

N: turn ration of transformer

$V_{OUT}$: target output voltage

$V_{D1}$: the forward voltage of D1.

If $V_{OUTMAX}$=320V, $V_{BATMAX}$=6V and $V_{SPIKE}$=0V, the turn ration N should be higher than 9. Usually, a transformer of N=10~15 is recommended for most of the applications while using the LD7265A.

## Minimum Primary Inductance

To ensure accurate operation for the LD7265A, the acceptable primary inductance, Lp (H), should meet the following formula:

$$L_P \geq \left(\frac{330 \times 10^{-9} \times V_{OUT}}{N \times I_{LIM(MIN)}}\right)$$

$I_{LIM(MIN)}$: the selected min primary current limit value during charging period

$V_{OUT}$: target output voltage

Ex1: N=15, $V_{OUT}$=300V, selected min primary current limit value during operation, $I_{LIM(MIN)}$= $I_{LIM1}$=0.54A

→ Lp ≥12.3μH.

Ex2: N=12, $V_{OUT}$=300V, selected min primary current limit value during operation, $I_{LIM(MIN)}$= $I_{LIM4}$=1.08A

→ Lp ≥ 7.7μH

For most applications, it's recommended to choose a transformer of $L_P$=6μH~15μH for $V_{BAT}$ in the voltage range of 1.8V~6V.

## Minimum off time of VLX

The acceptable minimum pulse of VLX should be larger than 500nS during the whole charging cycle. Otherwise, the FB signal detection scheme of LD7265A can't operate properly and will affect the accuracy of output voltage detection.

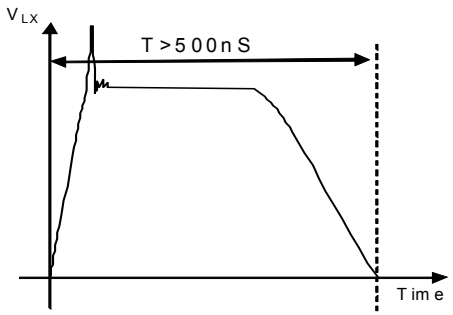



Fig.18

## Transformer Primary Leakage Inductance

The leakage inductance at the primary side of the transformer will result in the turn-off spike at LX pin. The spike should not exceed the dynamic rating of the LX pin. To restrict it, it's necessary to choose a transformer of lower leakage inductance.

## Transformer Secondary Capacitance

Any capacitance on the secondary will severely affect the efficiency. The secondary capacitance is multiplied by $N^2$ when reflected to the primary side and cause it larger. This capacitance forms a resonant circuit with the primary leakage inductance of the transformer. Therefore, both the primary leakage inductance and secondary capacitance should be minimized.

As well, the LD7265A also builds in with over current protection of LX pin to avoid transformer saturation condition. If the primary current is over 3A, then the IC will latch off and stop switching.

## Charging Current Drop Compensation

When the users select lower charging current limit values ($I_{LIM1}$ or $I_{LIM2}$) to charge the output capacitor, the input charging current will exhibit larger drop phenomena and cause longer charging time. The LD7265A built a charging current drop compensation scheme to compensate the drop phenomena. When the users select the lower charging current limit values ($I_{LIM1}$ or $I_{LIM2}$), LD7265A will linearly increase the primary current from 0% to 15%, during the whole charging cycle. Please refer to Fig.19 and Fig.20.

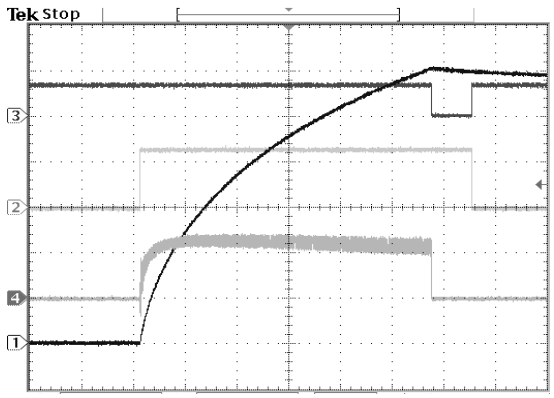



Fig.19 Charging Current with Drop Compensation

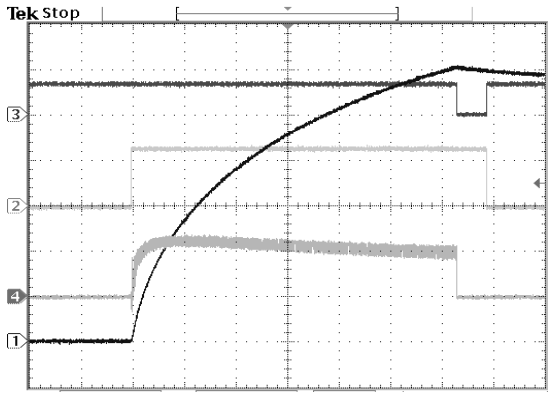



Fig.20 Charging Current without Drop Compensation

## Maximum ON Time

To prevent some worse cases like insufficient current from a poor power source (ie., an almost discharged battery), and may never reach current limit value, the LD7265A employs maximum on-time function for it. Once upon ON time exceeds 32μS, the LD7265A will latch off regardless of current limit detection.

## Adjust Output Voltage

A resistor divider can be connected to the central of the dual diode to eliminate the leakage current after the charging completes. Fig.21 shows the application circuit of resistor divider.

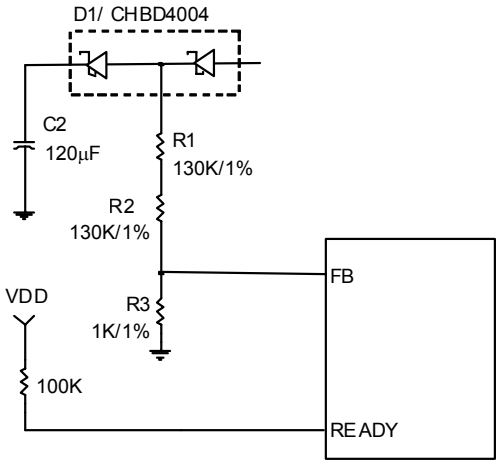



Fig.21

$$V_{OUT} = 1.15 \times (1 + \frac{R1 + R2}{R3})$$

It's not recommended to choose the resistors larger than 1KΩ to connect with FB to GND (R3 in Fig. 21), since larger resistors would combine with parasitic capacitance and affect the accuracy of $V_{OUT}$ detection. As well, the switching nodes such as LX pin or secondary side of XFMR should be kept routed away from FB pin in such application of Fig.20 to obtain accurate $V_{OUT}$ detection.

## Output Voltage Overcharge Protection

As shown in Fig.1, Fig.2, or Fig.3, the FB pin may fail to reach 1.15V during the charging cycle, either when the R3 is short to GND or R1 (or R2) open. It will cause $V_{OUT}$ increase continuously till over the target value of output voltage. LD7265A features proprietary detecting scheme to effeteively avoid this phenomenon.

## IGBT Driver

LD7265A separates the source and sink pin of IGBT driver, that enables the users to easily meet the requirement of any different IGBT applications. Besides, when VCC is under 2.5V (typ), OUTP and OUTN pin will have no output signal even TRIGGER pin is toggled high.

## Rectifying Diode Selection

Choose a rectifying diode with shorter reverse recovery time to limit the switching loss and increase the charging efficiency. And in addition, it would allow sufficient peak reverse voltage and peak forward current rating.

The peak reverse voltage is about:

$V_{PK-R} = V_{OUT} + N_X V_{BAT} + VS_{PIKE}$

The peak forward current is about:

$I_{PK-SEC}$= Ip / N, $I_P$: peak primary current (A), N: turn ratio

## Interface

CHARGE, READY and TRIGGER can be easily interfaced to a microprocessor.

The CHARGE pin is the ON/OFF control of charging circuit.

High=enable, Low =disable

The DONE# pin is an indicator of charging and output voltage state.

High= otherwise

Low= the charging is completed and CHARGE pin is high

The TRIGGER pin is the ON/OFF control of the strobe to generate a light pulse.

High=enable, Low =disable

Note that the trigger function is only active while the charging function is disabled.

## Layout Consideration

1. The layout of this IC should follow the rule of high voltage isolation to avoid any breakdown failure of this IC and circuit board.
2. Keep the bypass capacitor 1μF very close to IC GND. (<5mm)
3. Refer to Fig.21, there should be no GND plane or GND path close to nodes of R1, R2 and R3.
4. Keep output voltage feed back network close to IC and far away from any interference nodes or paths.
5. The LX pin and GND Pin should be with large metal trace area.
6. The switching nodes, such as LX pin or anode of rectifying diode should be kept routed away from FB pin.
7. Please refer to Fig.22 and the EV kit for the PCB layout example.

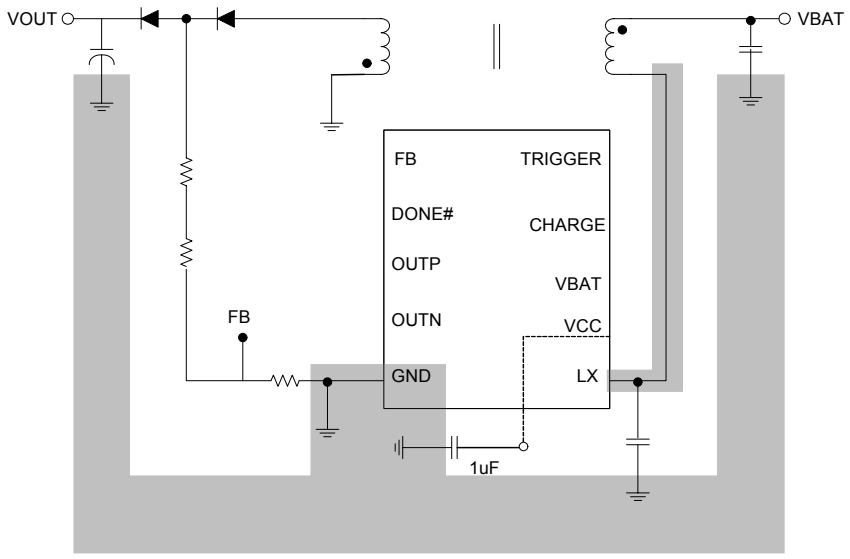



Fig.22 Recommended PCB layout

## Reference Design for DSC (IGBT solution)

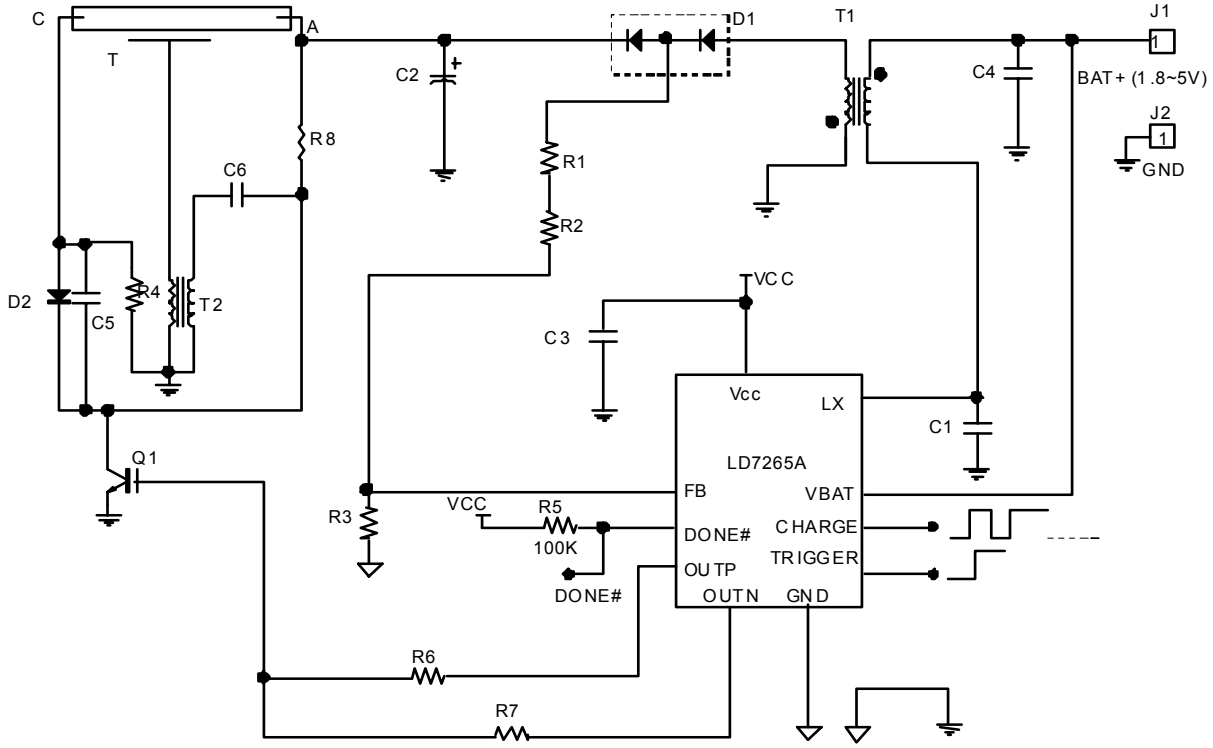



Fig. 22

**BOM list**

| REF | Value | PART NO. | Package | Vendor |
|---|---|---|---|---|
| U1 | | LD7265A | DFN-10 | Leadtrend |
| C1 | | | | |
| C2 | 120μF/330V | FW Series | Radial | Rubycon |
| C3 | 1μF/X5R/6.3V | | 0603 | |
| C4 | 22μF/X5R/6.3V | | 1206 | |
| C5, C6 | 33nF/500V | | 1206 | |
| R1, R2 | 130K/1%/200V | | 0603 | |
| R3 | 1K/1% | | 0402 | |
| R4 | 100K/300V | | 0805 | |
| R5 | 100K | | 0402 | |
| R6 | 0 | | 0402 | |
| R7 | 30 | | 0402 | |
| R8 | 1M/300V | | 0805 | |
| D1 | | CHBD4004SPT | SOT-23 | Chenmko |
| D2 | | RGF10M | SMA | Zowie |
| Q1 | | GT5G131 | SOP-8 | Toshiba |
| T1 | | | | |
| T2 | | | | |

## Reference Design for Camera Phone (IGBT solution)

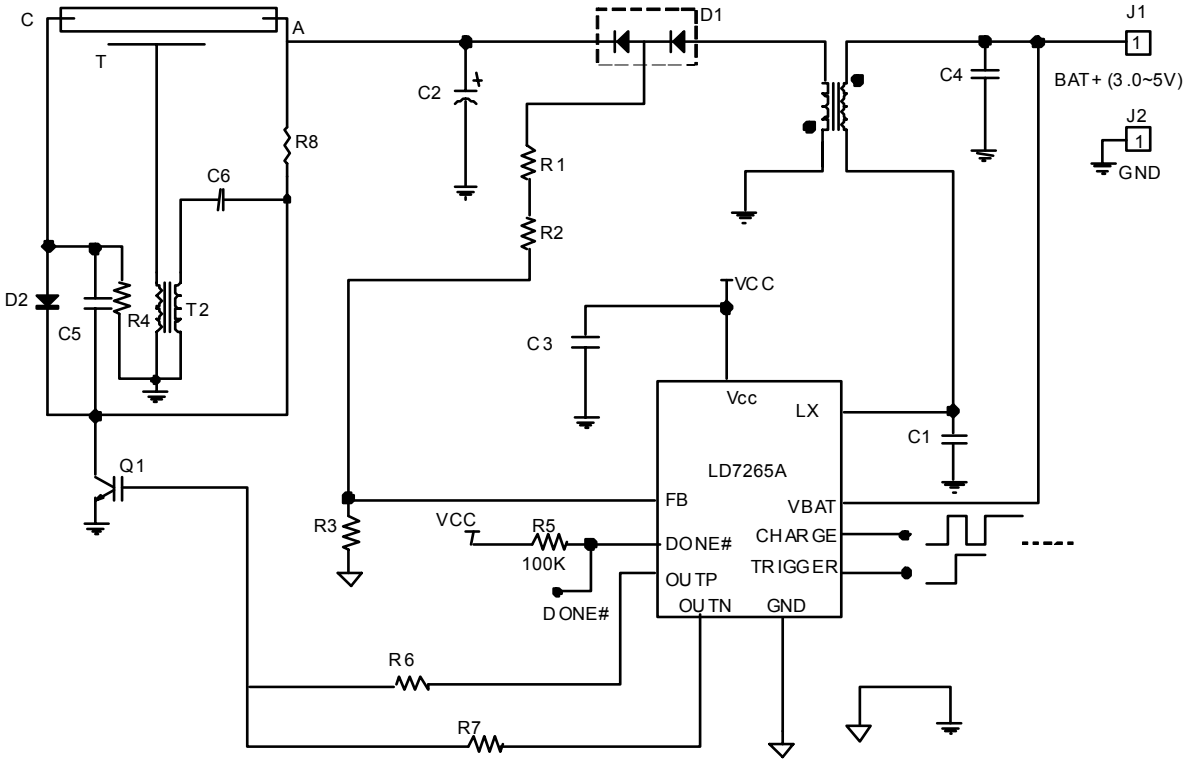



Fig. 23

**BOM list**

| REF | Value | PART NO. | Package | Vendor |
|---|---|---|---|---|
| U1 | | LD7265A | DFN-10 | Leadtrend |
| C1 | | | | |
| C2 | 33μF/330V | FW Series | Radial | Rubycon |
| C3 | 1μF/X5R/6.3V | | 0603 | |
| C4 | 22μF/X5R/6.3V | | 1206 | |
| C5, C6 | 33nF/500V | | 1206 | |
| R1, R2 | 130K/1%/200V | | 0603 | |
| R3 | 1K/1% | | 0402 | |
| R4 | 100K/300V | | 0805 | |
| R5 | 100K | | 0402 | |
| R6 | 0 | | 0402 | |
| R7 | 68 | | 0402 | |
| R8 | 1M/300V | | 0805 | |
| D1 | | CHBD4004SPT | SOT-23 | Chenmko |
| D2 | | RGF10M | SMA | Zowie |
| Q1 | | CY25CAH-8F | VSON8 | Renesas |
| T1 | | | | |
| T2 | | | | |

## Reference Design for Camera Phone (SCR solution)

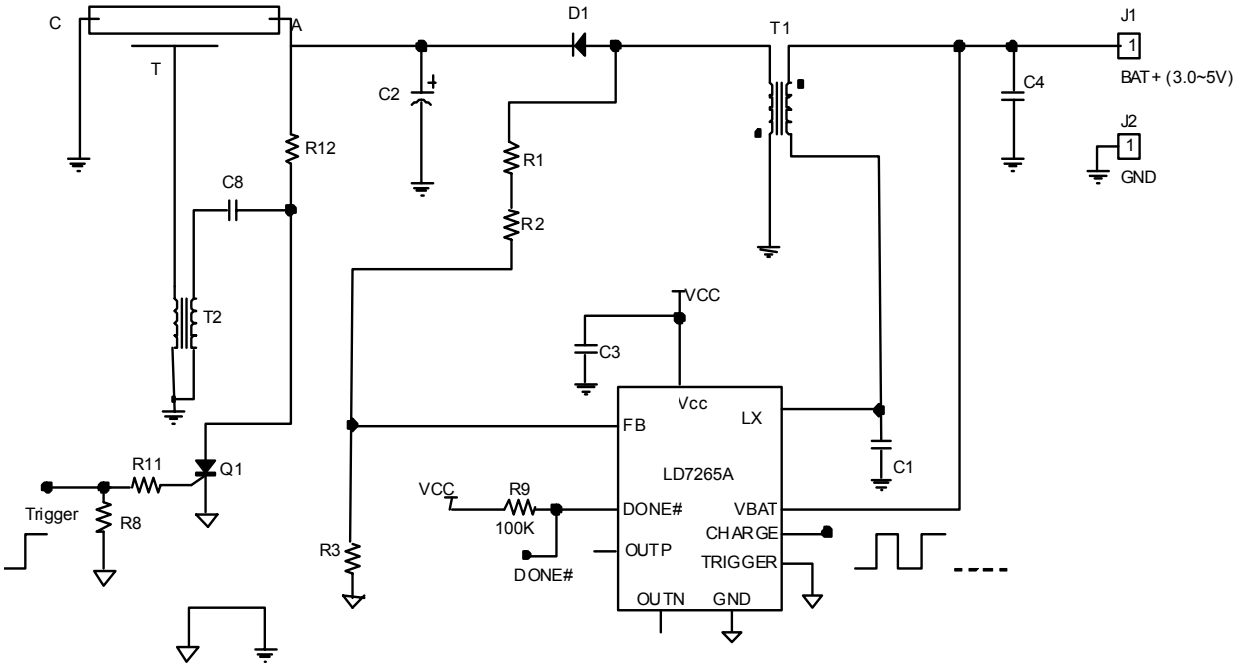


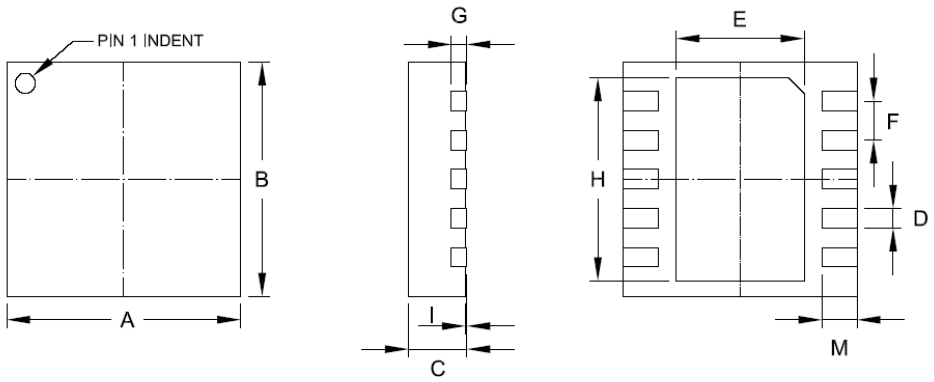

Fig. 24

## BOM list

| REF | Value | PART NO. | Package | Vendor |
|---|---|---|---|---|
| U1 | | LD7265A | DFN-10 | Leadtrend |
| C1 | | | | |
| C2 | 33μF/330V | FW Series | Radial | Rubycon |
| C3 | 1μF/X5R/6.3V | | 0603 | |
| C4 | 10μF/X5R/6.3V | | 0805 | |
| C8 | 33nF/500V | | 1206 | |
| R1, R2 | 130K/1%/200V | | 0603 | |
| R3 | 1K/1% | | 0402 | |
| R8 | 10K | | 0402 | |
| R9 | 100K | | 0402 | |
| R11 | 1K | | 0402 | |
| R12 | 1M/300V | | 0805 | |
| D1 | | FV02R80 | | Origin |
| Q1 | | S6A37 | SOT-23 | Toshiba |
| T1 | | | | |
| T2 | | | | |

# Package Information

## W type, DFN-10 (3mm x 3mm)

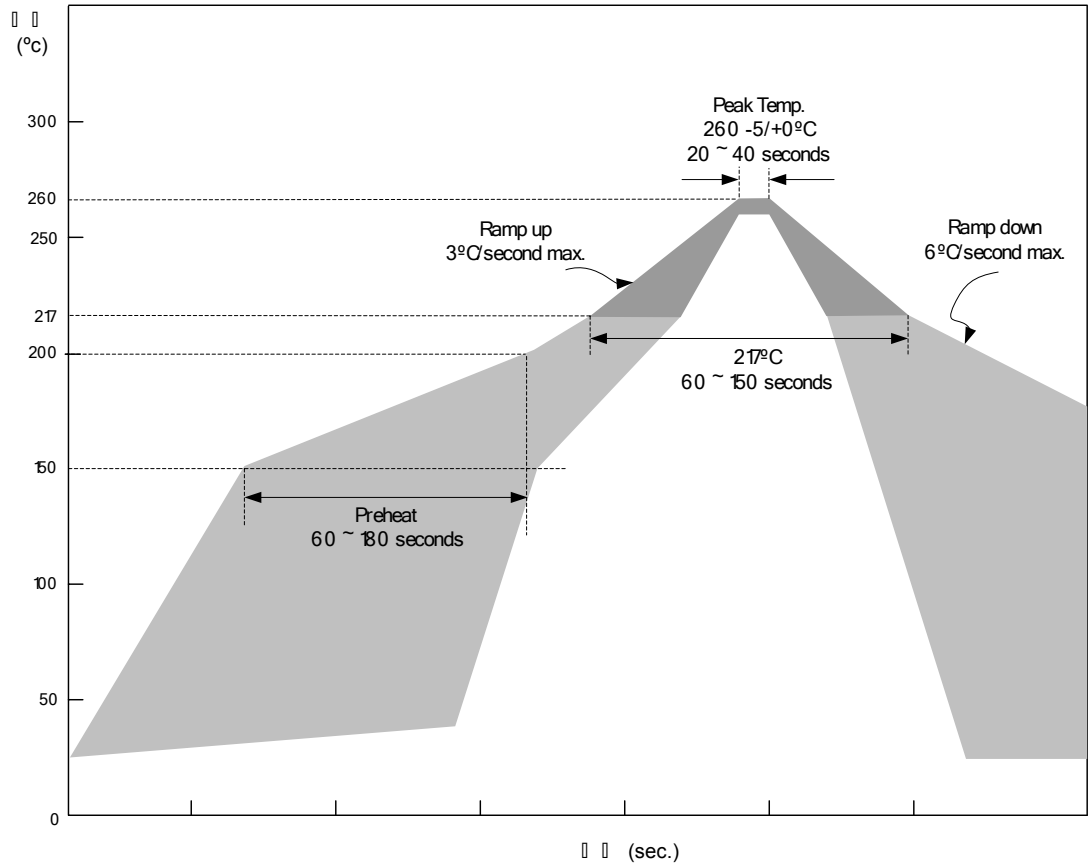



| Symbols | Dimensions in Millimeters | | Dimensions in Inch | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.900 | 3.100 | 0.114 | 0.122 |
| B | 2.900 | 3.100 | 0.114 | 0.122 |
| C | 0.650 | 0.850 | 0.026 | 0.033 |
| D | 0.180 | 0.300 | 0.007 | 0.012 |
| E | 1.100 | 1.690 | 0.043 | 0.067 |
| F | 0.50 TYP. | | 0.020 TYP. | |
| G | 0.20 REF | | 0.007 REF | |
| H | 2.100 | 2.650 | 0.083 | 0.104 |
| I | 0.000 | 0.050 | 0.000 | 0.002 |
| M | 0.400 | 0.650 | 0.016 | 0.026 |

### Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

## IR Profile for SMD Devices




| Item | Average Ramp-up Rate | Pre-heat (150 ~ 200°C) | Time Maintained Above 217°C | Peak Temp. | Ramp-down Rate |
|---|---|---|---|---|---|
| Required | 3°C second max. | 60~180 seconds | 60~150 seconds | 260 +0/-5°C 20~40 seconds | 6°C second max. |

## Revision History

| Rev. | Date | Change Notice |
|---|---|---|
| 00 | 6/10/08 | Original Specification. |
| 01 | 6/25/08 | Revision: Application schematic |