Photoflash Capacitor Charger with Integrated MOS

REV: 00

General Description

The LD7266A is an ideal charge control IC for flash units with internal soft start, adjustable charging current and output voltage. It provides a proprietary charging algorithm to charge photoflash capacitor quickly and efficiently. The LD7266A could operate in constant charging current mode or the mode with lowering the charging current at lower battery voltage. As well, the built-in 45V power switch and IGBT driver can save the board space.

The LD7266A is available in a space-saving MSOP10 or DFN-10 package and is ideal for DSC flash unit.

† Patented

Features

- Adjustable Charging Current and Output Voltage
- 1.8V~5V Battery Voltage Range
- Tiny Transformer
- Totem-Pole IGBT Driver
- Integrated 45V power switch
- Output Voltage Overcharge Protection

Applications

- DSC Flash Unit
- Cell Phone with Camera

Typical Application

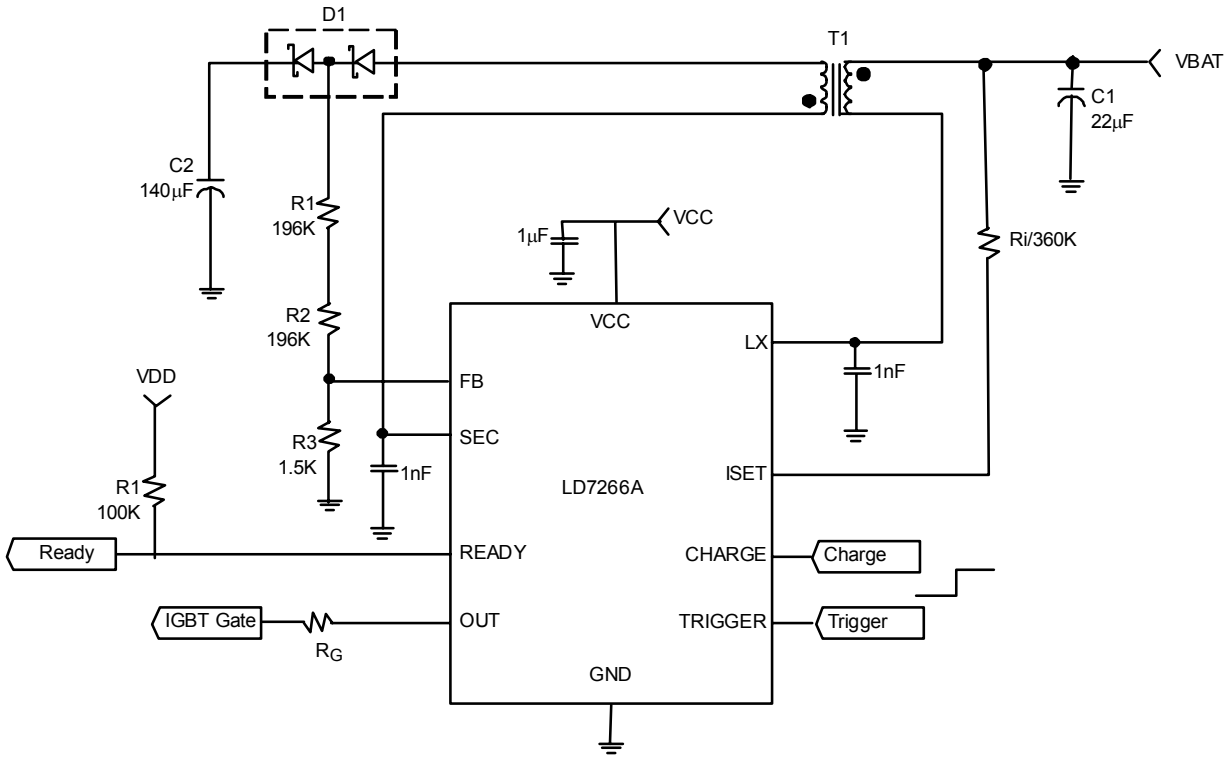
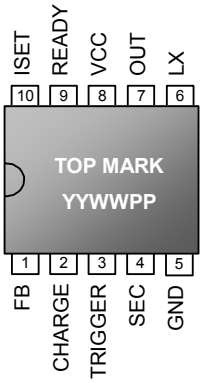


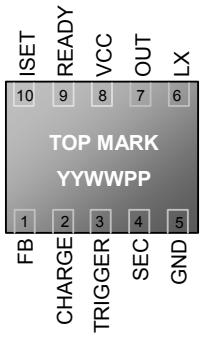
Fig.1

Pin Configuration

MSOP-10 (TOP VIEW)



DFN-10 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

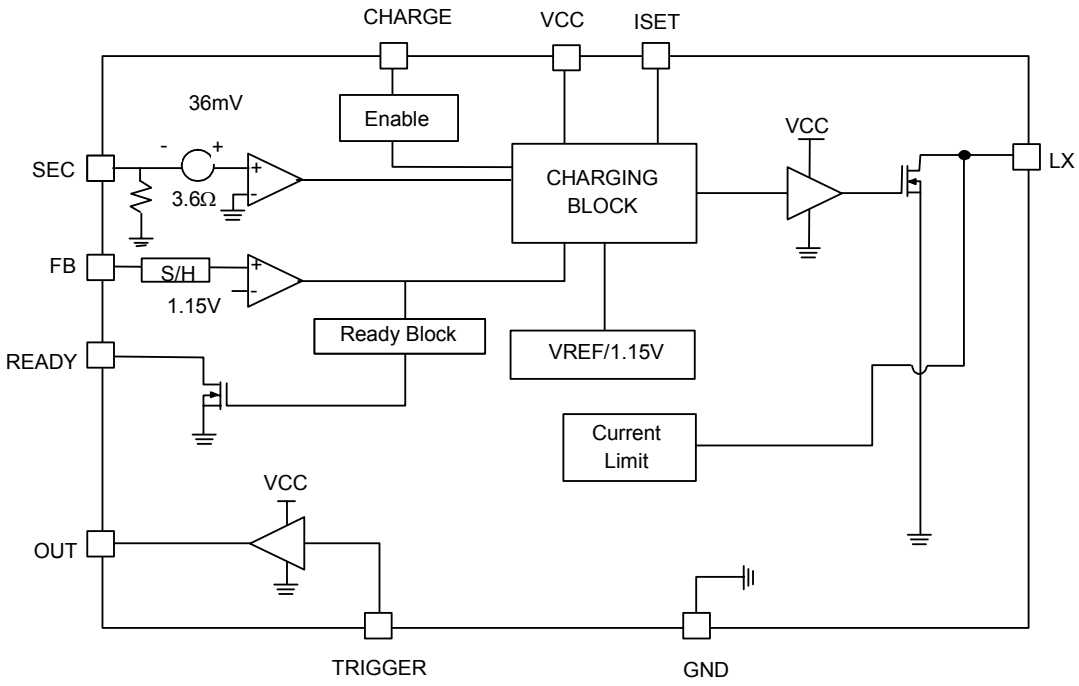
Part number	Package	Top Mark	Shipping
LD7266APL	MSOP-10	7266APL	2500 /tape & reel
LD7266AGL	MSOP-10 (Green Package)	7266AGL	2500 /tape & reel
LD7266APE	DFN-10	7266APE	2500 /tape & reel
LD7266AGE	DFN-10 (Green Package)	7266AGE	2500 /tape & reel

The LD7266A is ROHS complaint.

Pin Descriptions

PIN	NAME	FUNCTION
1	FB	Output voltage feedback
2	CHARGE	Charging on/off control pin. High=enable low=disable
3	TRIGGER	Trigger on/off control pin. High=enable low=disable
4	SEC	Secondary current sensing. Connect to transformer secondary.
5	GND	IC GND.
6	LX	NMOS drain pin. Connect to transformer primary as shown in Fig.1
7	OUT	IGBT driver output Pin.
8	VCC	Input power of IC. Bypass with a 1μF ceramic capacitor.
9	READY	Charge ready open drain output.
10	ISET	Adjust charging current with R to VBAT.
-	EP	Exposed Metal Pad. Exposed pad should be soldered to PCB board and connected to power ground plane to achieve better thermal dissipation. (for DFN-10 package)

Block Diagram



Absolute Maximum Ratings

Supply Voltage Vcc	-0.3V~6.0V
SEC Current	200mA
SEC pin	-0.6V~(Vcc+0.3)V
FB, Charge, Trigger, Ready, ISET pin	-0.3V~(Vcc+0.3) V
LX pin	
<200nS	-0.3V~45V
DC	-0.3V~40V
LX Current	4.5A
Package Thermal Resistance MSOP-10 θ_{JA}	120°C/W
Package Thermal Resistance DFN-10 θ_{JA}	60°C/W
Operating Temperature Range	-30°C to 85°C
Storage Temperature Range	-55°C to 125°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10sec)	260°C
ESD Level (Human Body Model)	2KV
ESD Level (Machine Model)	200V

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=3.3V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Power					
Operating Voltage V_{CC}		2.8		5.5	V
Shutdown Current I_{CC}	Charge=Off, Trigger=Off			1.5	μA
Nominal Supply Current	V_{CC}=3.3V, D=50%		0.6		mA
FB Pin					
Reference Voltage			1.15		V
Reference Voltage Tolerance				1.5	%
LX pin					
Current limit			2.0		A
On resistance	Vcc=3.3V, I_{LX}=1A		300	500	mΩ
LX leakage current	V_{LX}=40V			5	μA
IGBT Driver					
Output ON resistor	V_{CC}=3.3V		4	7.5	Ω
Output OFF resistor	V_{CC}=3.3V		14	21	Ω
Rising Time	V_{CC}=3.3V, C_L=3.9nF		70		nS
Falling Time	V_{CC}=3.3V, C_L=3.9nF		200		nS
ON/OFF					
Trigger On/Off	Enabled	1.4			V
	Disabled			0.6	V
Charge On/Off	Enabled	1.4			V
	Disabled			0.6	V
Impedance to GND					
Charge Pin to GND			100K		Ω
Trigger Pin to GND			100K		Ω
OUT Pin to GND			100K		Ω
SEC pin					
SEC Trip voltage			36		mV
SEC pin current sense blanking time			350		nS
Others					
Thermal Shutdown			160		°C
Max Turn On Time	Ri open		7		μS
Max Turn On Time Tolerance				6.6	%
Ready Pin Open Drain Resistance			90		Ω
Propagation Delay	(Trigger=High) delay to OUT		60		nS

Typical Performance Characteristics

C_{OUT}=140μF

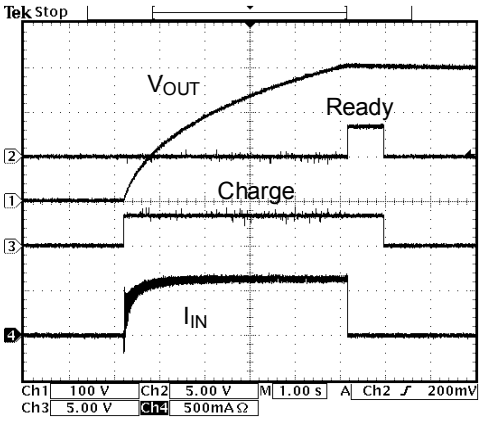


Fig. 2 Charging Waveform V_{IN}=3V, I_{IN}=600mA

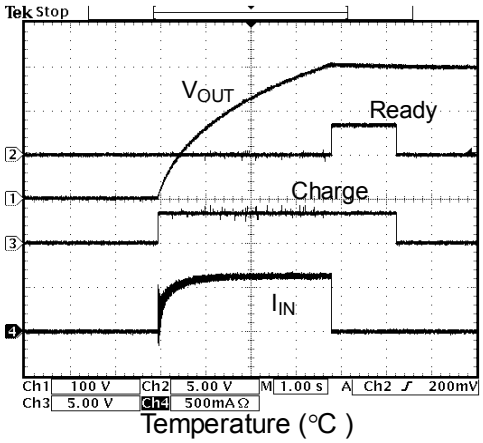


Fig. 3 Charging Waveform V_{IN}=4.2V, I_{IN}=600mA

C_{OUT}=47μF

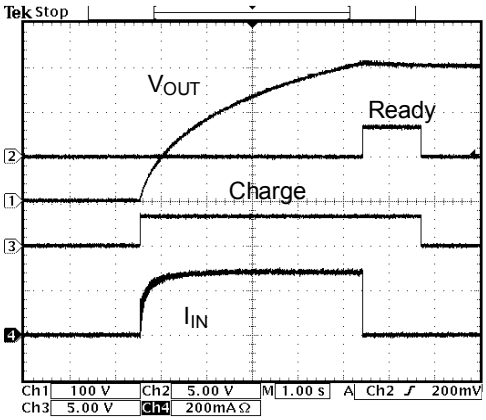


Fig. 4 Charging Waveform V_{IN}=3V, I_{IN}=280mA

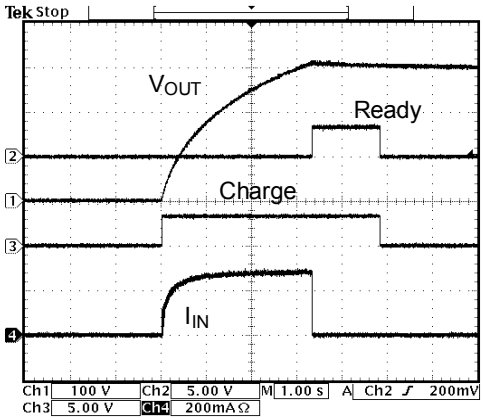


Fig. 5 Charging Waveform V_{IN}=4.2V, I_{IN}=280mA

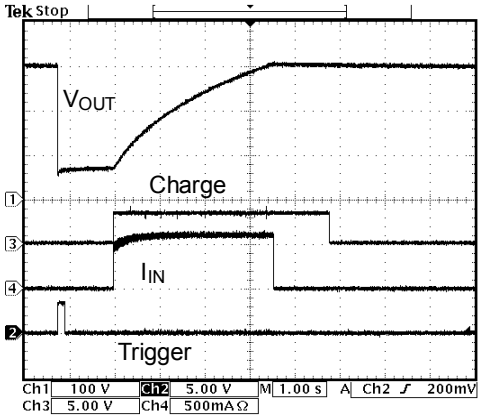


Fig. 6 Charging Waveform V_{IN}=4.2V

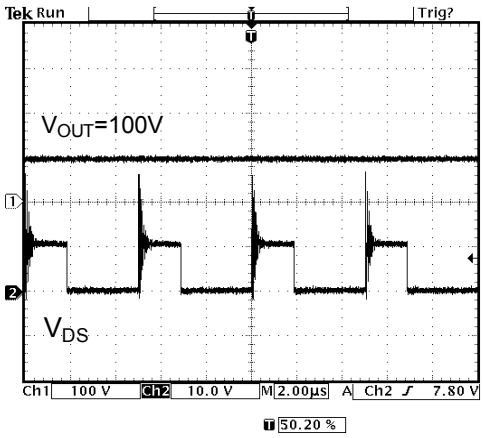


Fig. 7 VDS Waveform

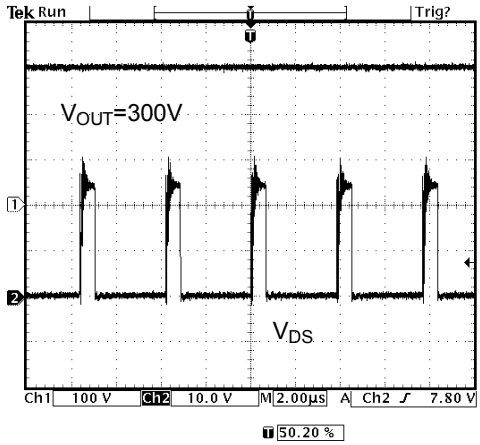


Fig. 8 VDS Waveform

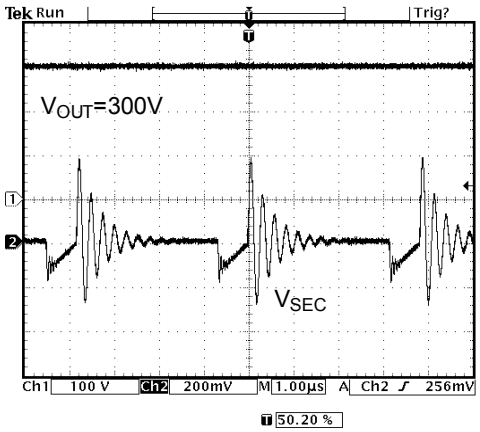


Fig. 9 V_{SEC} Waveform

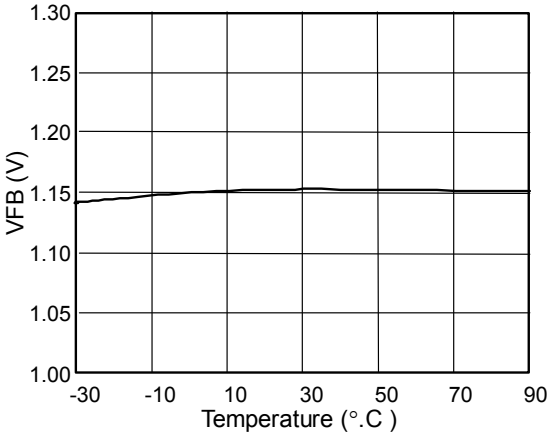


Fig. 10 FB Voltage vs. Temperature

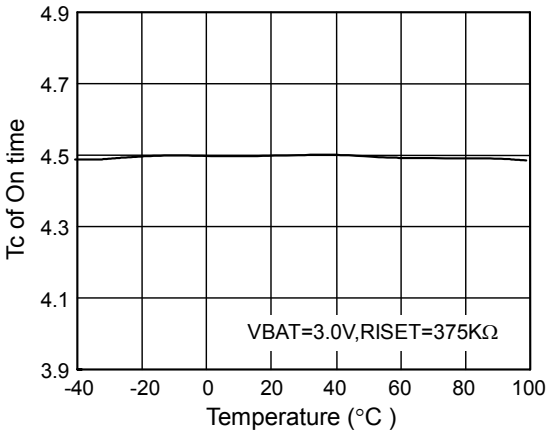


Fig. 11 On Time vs. Temperature

Function Description

Constant Charging Current

The LD7266A provides the solution of constant charging current for the lithium battery.

Simply adjust R_I to achieve the desired peak primary charging current.

$$R_I \approx 28L_P \times I_P K\Omega$$

L_P: primary inductance (μH)

I_P: desired peak primary current (A)

Ex: Desired I_P is 1.2A, L_P =10μH, then R_I =336K/1%

Note that the peak primary current must be less than the saturation current of transformer otherwise the transformer will be saturated.

Fig. 12 shows the example of this application

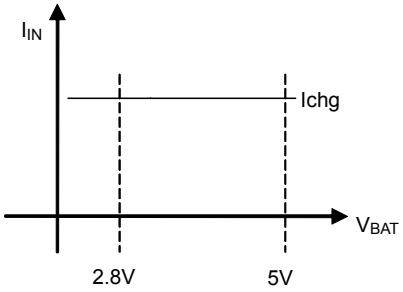


Fig. 12

Lower Charging Current at Low Battery Voltage

The LD7266A could operate in the mode with lowering the charging current at lower battery voltage, which is intended to use for 2AA battery. It provides a proprietary piecewise linearly charging current control to keep constant charging current at higher voltage and linearly lower charging current at lower battery voltage.

The Fig. 13 shows an example of the LD7266A in this application.

(1) If we want to set the cut-off voltage at V_{BAT}=2.5V, then Choose R_I according to the following equation.

$R_I = 200 \times V_{CUTOFF} K\Omega$

For this example, $R_I = 200 \times 2.5K\Omega = 500K\Omega$

(2) The max on time of LD7266A is 7μS, then the on time of V_{BAT}=3.3V is about 5.3μS (5.3μS=2.5V×7μS/3.3V)

(3) The ON time of V_{BAT} <2.5V keeps at 7μS.

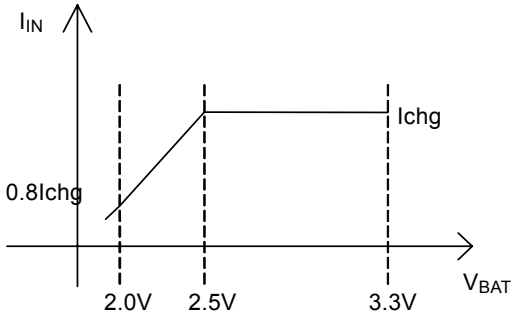


Fig. 13

Adjust Charging Current

Fig. 14 shows the curve of on time v.s. I_{SET} ($I_{SET}=V_{BAT}/R_I$).

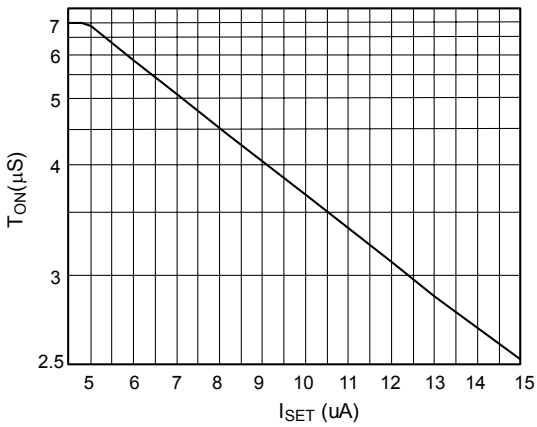


Fig.14 On time vs. I_{SET} (V_{CC}=3.3V)

Acceptable Minimum Ri

The acceptable minimum Ri for the LD7266A should be satisfied Eq.1 and Eq.2 at the same time.

$$R_{IMIN} \geq 13 \times \left(\frac{V_{OUTMAX}}{N} \right) K\Omega \text{ ---(1)}$$

$$R_{IMIN} \geq (1.1 L_P \times N) K\Omega \text{ ---(2)}$$

N: turn ration of transformer

L_P: primary inductance (μH)

Ex: N=12, V_{OUTMAX}=320V, Lp=10μH

→Ri > 346KΩ (Eq1); Ri>132 KΩ (Eq2)
→Choose Ri >346 KΩ

Please always keep RI value higher than the minimums described above to remain the proper operation in the whole battery range. If the RI value can't meet the requirement in charging application, please use a larger value of Lp to adjust the input current lower.

Transformer Selection

A carefully chosen transformer could result in best performance of the LD7266A. Usually, it's suitable to choose a transformer of L_P=10~20μH for V_{BAT} in the voltage range of 1.8V~5V. Also, the turning ratio of the transformer should be considered. The maximum voltage rating of the internal NMOS of the LD7266A is 45V. Thus, the turn ration is given by:

$$N \geq \frac{V_{OUTMAX} + V_{D1}}{45 - V_{BATMAX} - V_{SPIKE}}$$

where V_{D1} is the forward voltage of D1.

If V_{OUTMAX}=320V, V_{BATMAX}=5V and V_{SPIKE}=0V, this implies the turn ration N should be higher than 9. But considering V_{SPIKE}, a transformer with a turn ration of N>=10 is recommended for applications using the LD7266A.

Leakage Inductance and Parasitic Capacitance

The leakage inductance at the primary side of the transformer will result in the turn-off spike at LX pin. The spike should not exceed the dynamic rating of the LX pin. To restrict it, it's necessary to choose a transformer of lower leakage inductance or adding a snubber circuit. It's also recommended to maintain the leakage inductance at proper value. A too low level of leakage inductance will increase the parasitic capacitance, leading to high initial current swings when the switch turns on. Thus trade off is necessary between leakage inductance and parasitic capacitance. The LD7266A was built in with 1.2μS of blanking to avoid these high current swings to incorrectly trigger the current limit level (at 2A). As well, LD7266A was also built in over current protection of LX pin. If the primary current is over a maximum peak current (at 4A), then IC will latch off and stop switching. Care should be taken that the peak swing current not over 4A and its duration time which is over 2A should not longer than 1.2μS.

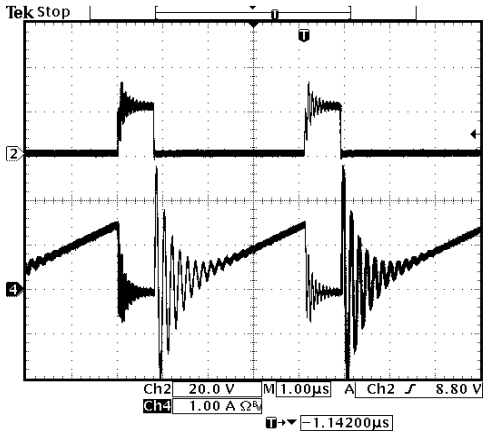


Fig. 15

Adjust Output Voltage

The LD7266A could sense output voltage by using an output resistor divider.

Fig.16 shows the application circuit of resistor divider.

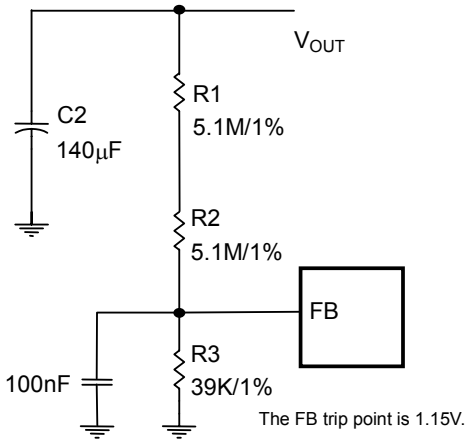


Fig.16

$$V_{OUT} = VFB \times (1 + \frac{R1 + R2}{R3})$$

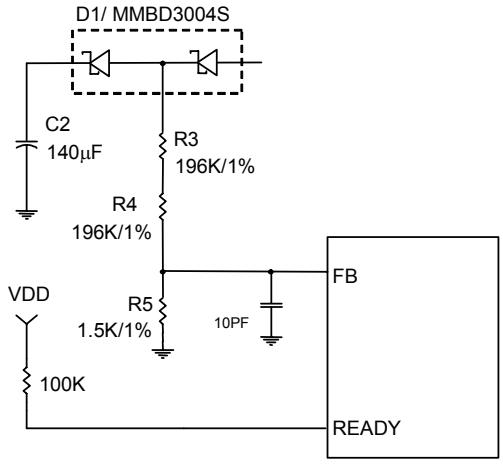


Fig.17

A resistor divider can be connected to the central of the dual diode to eliminate the leakage current in the application of Fig. 16 after the charging completes. The Fig. 17 shows the application circuit.

$$V_{OUT} = V_{FB} \times (1 + \frac{R3 + R4}{R5})$$

Choose the lower resistor (R5 in Fig. 17) connected form FB to GND, less than 2KΩ. Larger resistor combined with parasitic capacitance at FB pin would affect the V_{OUT} detection accuracy. As well, the switching nodes such as LX pin or secondary side of XFMR should be kept routed away from FB pin for Fig.17 application, otherwise it would affect the V_{OUT} detection accuracy. Use a small capacitor (10pF~33pF, connected between FB pin to GND) to filter the FB Pin noise if there exists the poor PCB layout issue, while using Fig.17 application.

Output Voltage Overcharge Protection

As shown in Fig.1, the FB pin would fail to reach 1.15V during the charging cycle, either when the R3 is short to GND or when the R1 (or R2) is open. It will cause V_{OUT} increase continuously till over the target value of output voltage. LD7266A provides a proprietary detecting scheme which could effetely avoid this phenomenon.

Interface

CHARGE, READY and TRIGGER can be easily interfaced to a microprocessor.

The CHARGE pin is the ON/OFF control of charging circuit.

High=enable, Low =disable

The READY pin is an indicator of charging and output voltage state.

High= the charging is completed and CHARGE pin is high

Low= otherwise

The TRIGGER pin is the ON/OFF control of the strobe to generate a light pulse.

High=enable, Low =disable

Because the impedance of CHARGE pin and TRIGGER pin to GND is about 100KΩ. Thus, the user could use a resistor to form as a divider to increase the enable and disable level.

Note that the trigger function is only active while the CHARGE pin goes low.

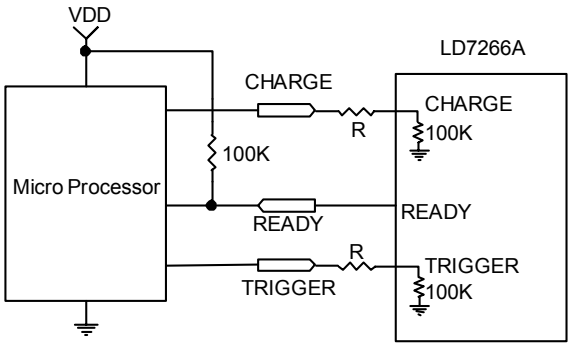


Fig. 18

Layout Consideration

1. The layout of this IC should follow the rule of high voltage isolation to avoid any breakdown failure of this IC and circuit board.
2. Keep the bypass capacitor 1μF very close to IC GND. (<5mm)
3. Keep output voltage feed back network, R_I and C_S very close to IC and far away from any interference nodes or paths.
4. The LX pin and GND Pin should be with large metal trace area.
5. The switching nodes, such as LX pin or anode of rectifying diode should be kept routed away from ISET, FB and SEC pin.
6. Please refer to Fig.19 and the EV kit for the PCB layout example.

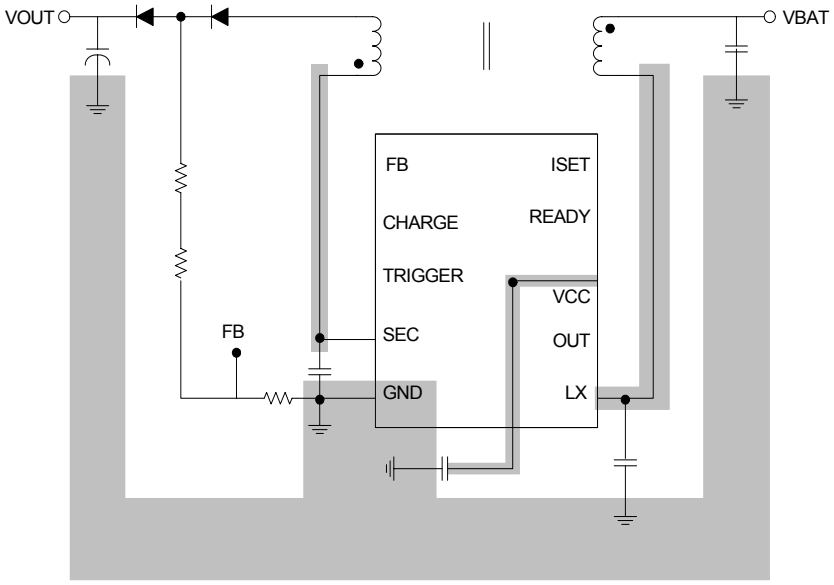
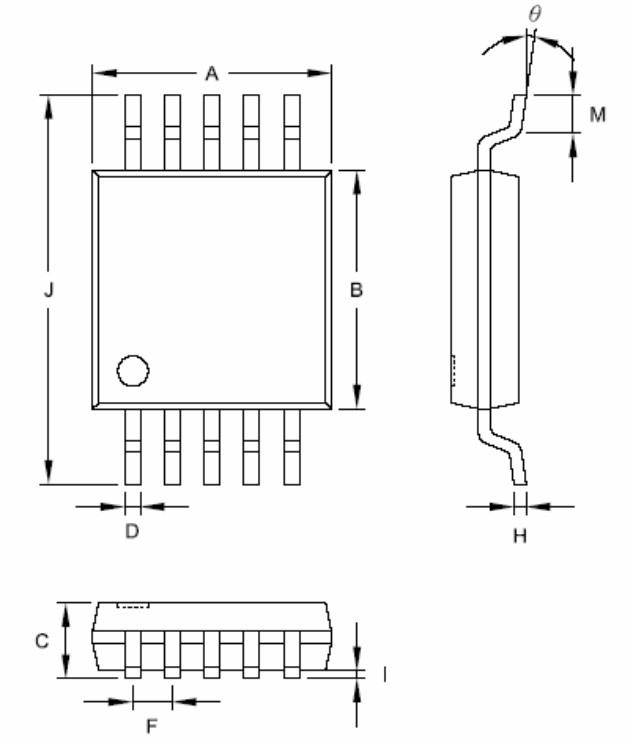


Fig.19 Recommended PCB layout

Package Information

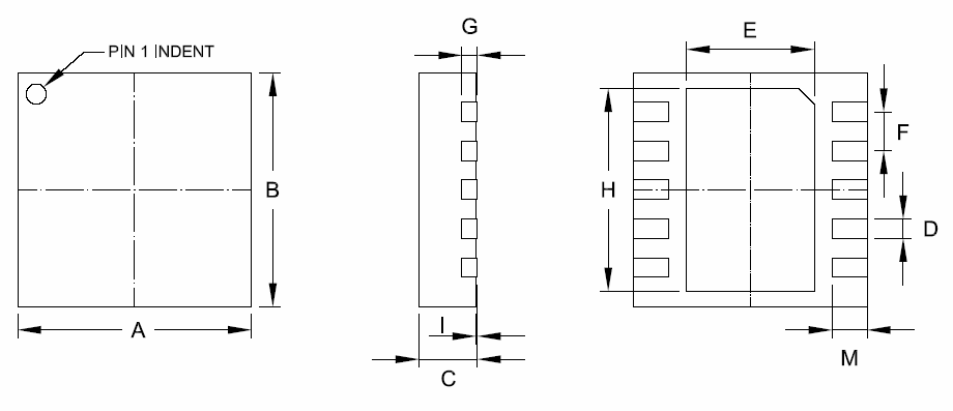
MSOP-10



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	2.896	3.099	0.114	0.122
B	2.896	3.099	0.114	0.122
C	0.813	1.219	0.032	0.048
D	0.152	0.305	0.006	0.012
F	0.470	0.530	0.018	0.020
H	0.127	0.229	0.005	0.009
I	0.051	0.152	0.002	0.006
J	4.699	5.105	0.185	0.201
M	0.406	0.660	0.016	0.026
θ	0°	6°	0°	6°

Package Information

DFN-10, (3mm x 3mm)

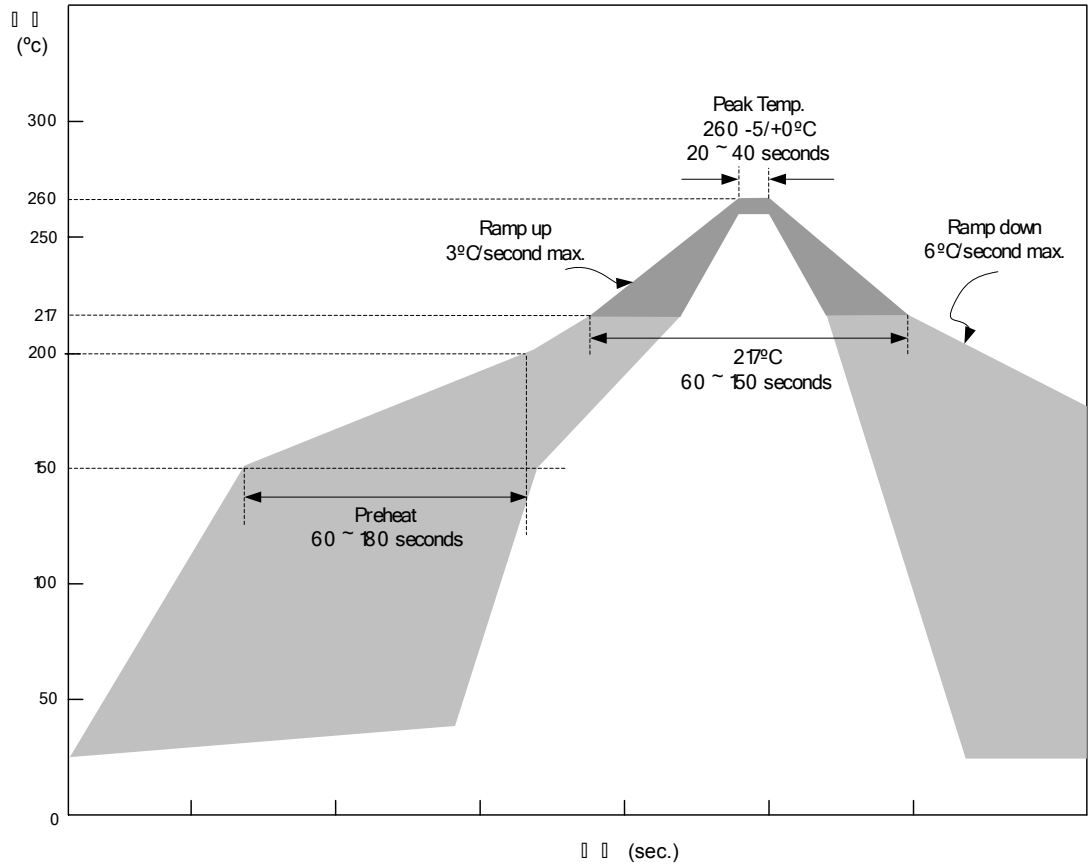


Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	2.900	3.100	0.114	0.122
B	2.900	3.100	0.114	0.122
C	0.650	0.850	0.026	0.033
D	0.180	0.300	0.007	0.012
E	1.100	1.690	0.043	0.067
F	0.50 TYP.		0.020 TYP.	
G	0.20 REF		0.007 REF	
H	2.100	2.650	0.083	0.104
I	0.000	0.050	0.000	0.002
M	0.400	0.650	0.016	0.026

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

IR Profile for SMD Devices



Item	Average Ramp-up Rate	Pre-heat (150 ~ 200°C)	Time Maintained Above 217°C	Peak Temp.	Ramp-down Rate
Required	3°C second max.	60~180 seconds	60~150 seconds	260 +0/-5°C 20~40 seconds	6°C second max.

Revision History

Rev.	Date	Change Notice
00	3/1/07	Original Specification.