Smart Photoflash Capacitor Charger with Integrated MOS

REV：03

General Description

The LD7270 is an ideal charge control IC for flash units, featuring internal soft start, adjustable charging current and output voltage. It provides a charging algorithm to speed up the charging with higher efficiency. The LD7270 can operate in desired constant peak current mode through adjusting R_I between ISET pin and GND. As well, LD7270 uses separate source and sink pin of IGBT driver, which enables the users to easily meet different IGBT application requirements.

The LD7270 is available in a space-saving WDFN-10L 3x3 package and is ideal for DSC flash unit.

† Patented

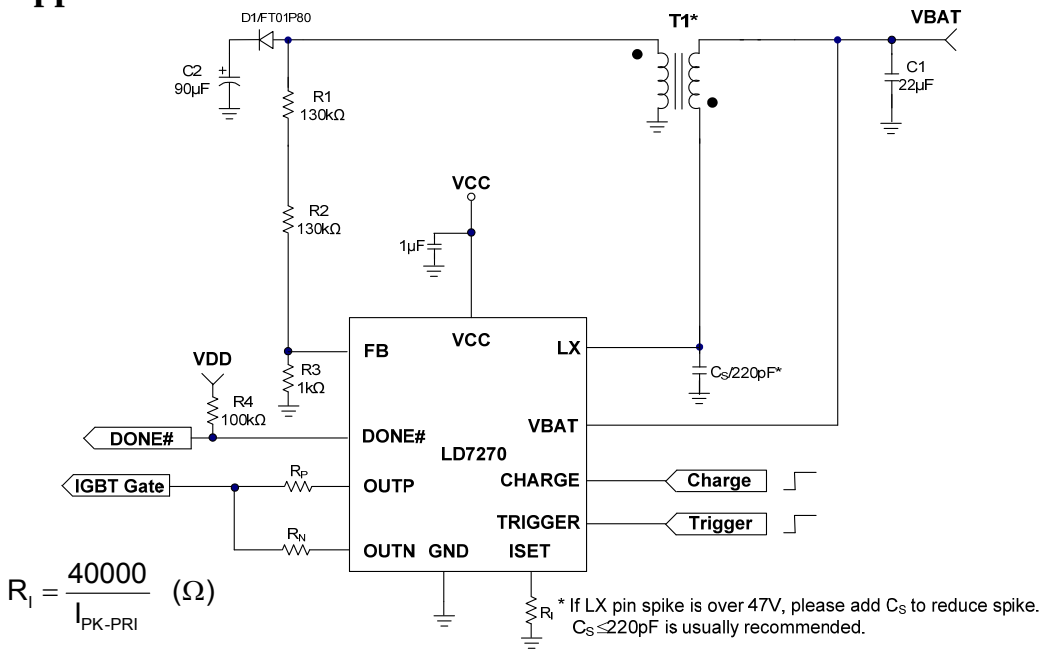
Features

- 1.8V~6V Battery Voltage Range
- Adjustable Output Voltage
- Adjustable Input Current
- Integrated 47V Power MOS
- Separate Source and Sink Pin of IGBT Driver
- False Triggering Prevention
- Soft Start
- Output Voltage Overcharge Protection
- High Efficiency

Applications

- DSC Flash Unit
- Cell Phone with Camera

Typical Application



$$R_I = \frac{40000}{I_{PK\text{-}PRI}} \quad (\Omega)$$

Fig.1

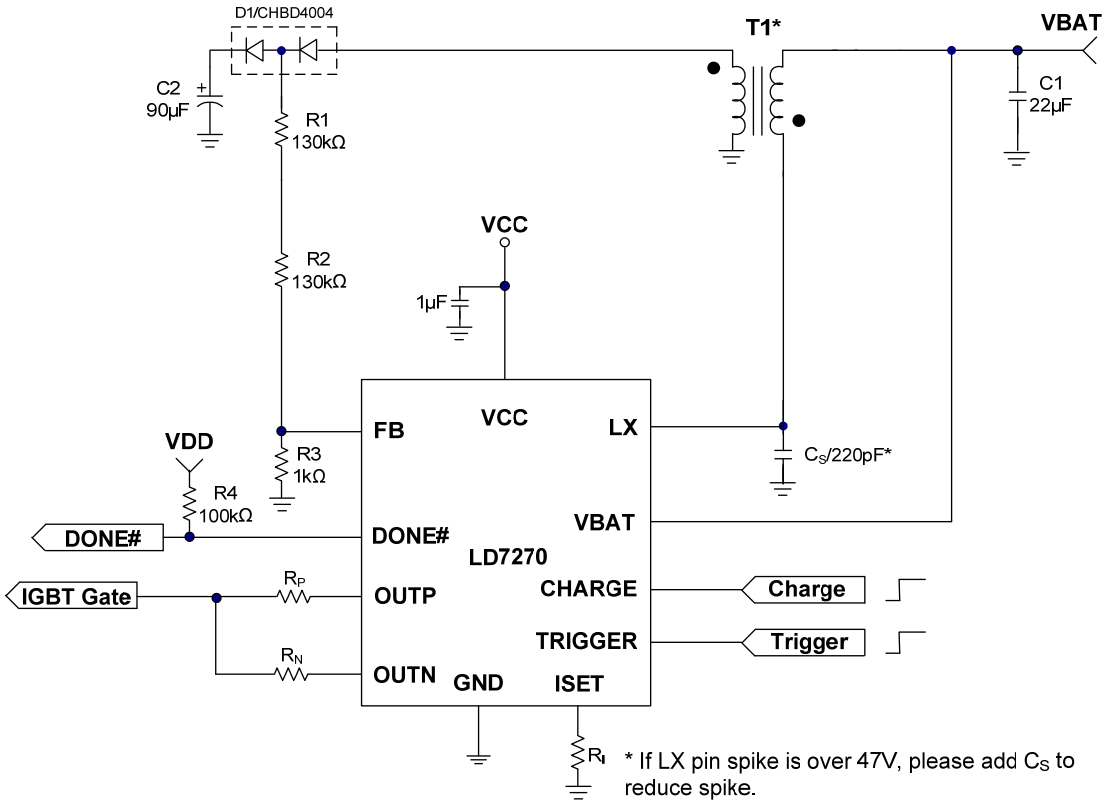

D1/CHBD4004
T1*
VBAT
C2
90µF
R1
130kΩ
C1
22µF
R2
130kΩ
VCC
1µF
FB
VCC
LX
VDD
R3
1kΩ
R4
100kΩ
CS/220pF*
DONE#
DONE#
VBAT
LD7270
IGBT Gate
RP
OUTP
CHARGE
Charge
TRIGGER
Trigger
RN
OUTN
GND
ISET
RI
* If LX pin spike is over 47V, please add CS to reduce spike.
CS≤ 220pF is usually recommended.

Fig. 2

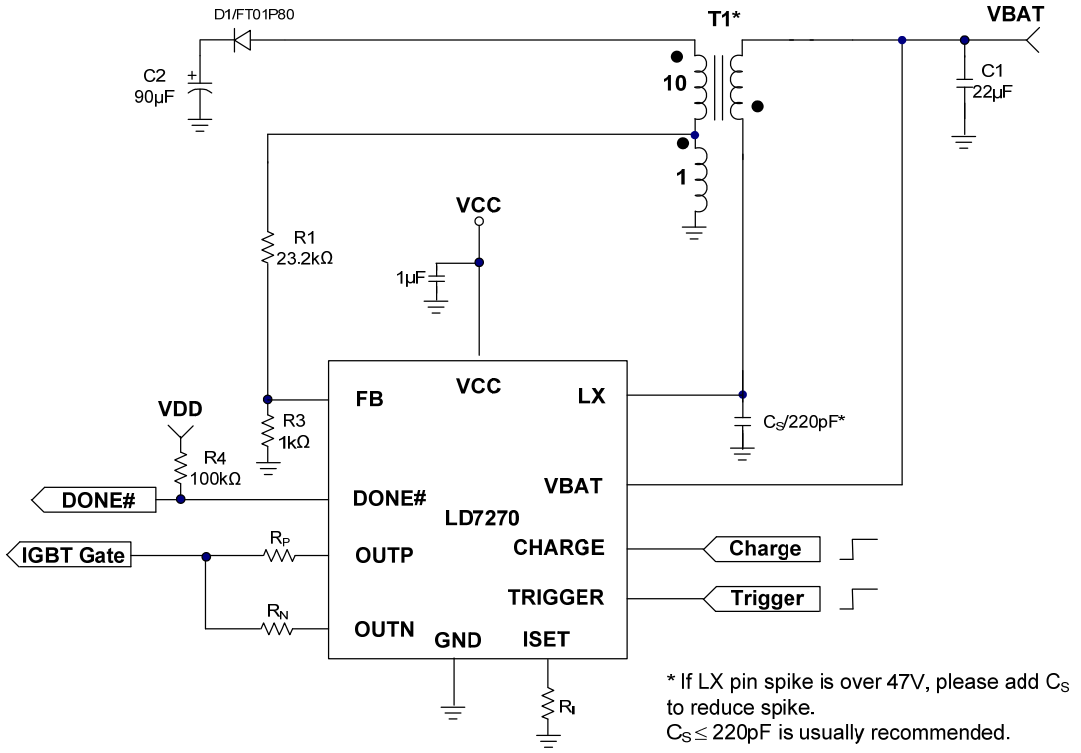

D1/FT01P80
T1*
VBAT
C2
90µF
10
C1
22µF
1
VCC
R1
23.2kΩ
1µF
FB
VCC
LX
VDD
R3
1kΩ
R4
100kΩ
CS/220pF*
DONE#
DONE#
VBAT
LD7270
IGBT Gate
RP
OUTP
CHARGE
Charge
TRIGGER
Trigger
RN
OUTN
GND
ISET
RI
* If LX pin spike is over 47V, please add CS to reduce spike.
CS≤ 220pF is usually recommended.

Fig. 3

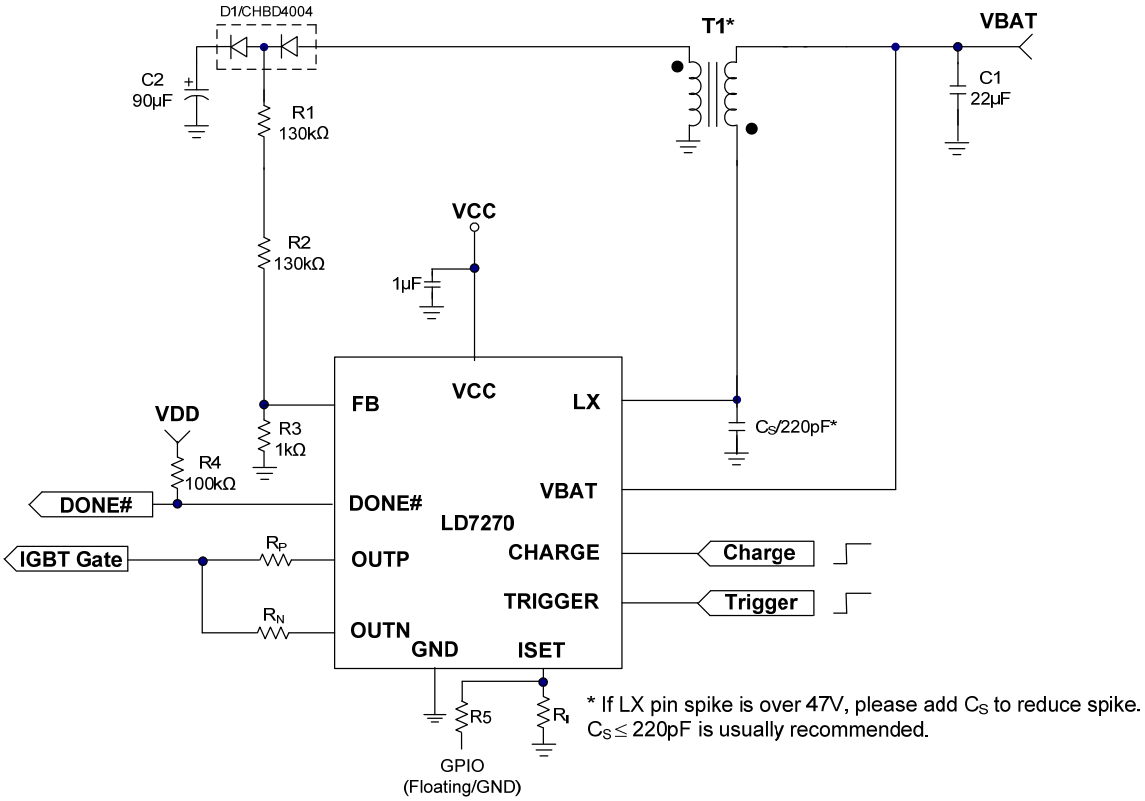
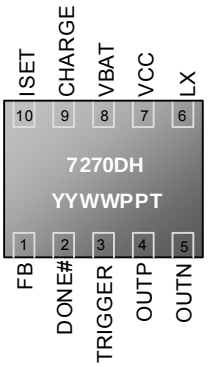


Fig. 4 Two level charging current.

Pin Configuration

WDFN-10 (3mm x 3mm)



YY: Year code
WW: Week code
PP: Production code
T: Thickness
W: 0.75mm (typical)

Ordering Information

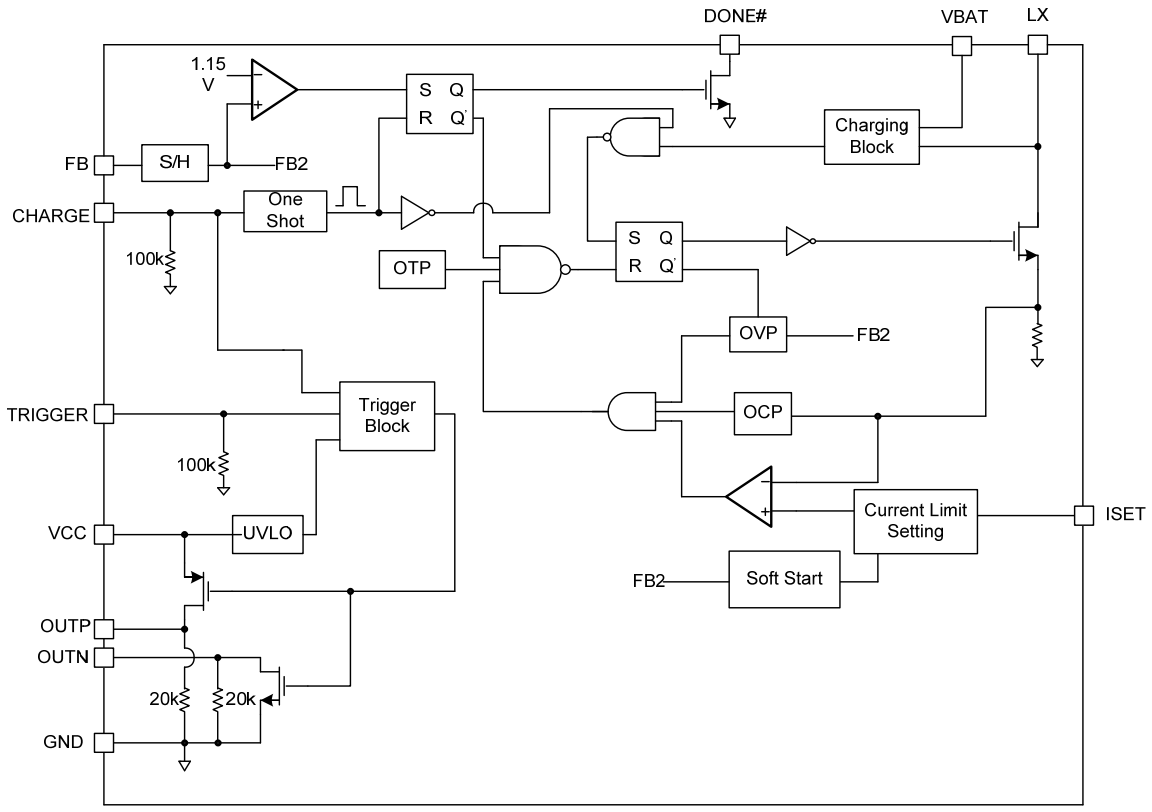
Part number	Package	Top Mark	Shipping
LD7270GDHW	WDFN-10L 3mm x 3mm	7270DH	2500 /tape & reel

The LD7270 is ROHS compliant.

Pin Descriptions

PIN	NAME	FUNCTION
1	FB	Output voltage feedback
2	DONE#	Charge Done Indicator. DONE# is an open drain output that pulls low when CHARGE is high and the circuit has finished charging the output capacitor.
3	TRIGGER	Trigger on/off control.
4	OUTP	IGBT driver source output pin.
5	OUTN	IGBT driver sink output pin.
6	LX	NMOS drain pin. Connect to transformer primary as shown in Fig.1.
7	VCC	Input power of IC. Bypass with a 1μF ceramic capacitor close to IC GND.
8	VBAT	Battery Voltage Input
9	CHARGE	Charging on/off control.
10	ISET	Input current setting pin.
Exposed Metal Pad	GND	IC GND. Exposed pad should be soldered to PCB board with a larger area

Block Diagram



Absolute Maximum Ratings

VCC and VBAT Pin	-0.3V~6.5V
FB pin	-0.45V~6.5V
Charge, Trigger, DONE#, ISET, OUTP and OUTN pin	-0.3V~6.5V
LX pin<200ns	-0.3V~47V
DC	-0.3V~42V
LX Current	3.3A
Package Thermal Resistance WDFN-10L 3mm×3mm, θ_{JA}	60°C/W
Operating Temperature Range	-30°C to 85°C
Storage Temperature Range	-55°C to 125°C
Junction Temperature	125°C
Lead Temperature (Soldering, 10sec)	260°C
ESD Level (Human Body Model)	2KV
ESD Level (Machine Model)	200V

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=3.3V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Power					
Operating Voltage V_{CC}		2.8		5.5	V
Under Voltage Lock Out (ON)			2.65		V
Under Voltage Lock Out (OFF)			2.55		V
Shutdown Current I_{CC}	Charge=Off, Trigger=Off			1.5	μA
Nominal Supply Current	V_{CC}=3.3V, D=50%		1		mA
FB					
Reference Voltage			1.15		V
Reference Voltage Tolerance		-1.5		+1.5	%
Sample time of FB detection		225	250	275	ns
LX pin					
On resistance	V_{CC}=3.3V, I_{LX}=0.75A		330		mΩ
LX leakage current	V_{LX}=35V			5	μA
Current Setting	Ri=80kΩ	0.45	0.5	0.55	A
Maximum Current Setting			1.8		A
IGBT Driver					
OUTP Resistance	V_{CC}=3.3V		4	7.5	Ω
OUTN Resistance	V_{CC}=3.3V		11	17	Ω
ON/OFF					
Trigger On/Off	Enabled	1.4			V
	Disabled			0.6	V
Charge On/Off	Enabled	1.4			V
	Disabled			0.6	V
Impedance to GND					
Charge Pin to GND			100k		Ω
Trigger Pin to GND			100k		Ω
OUTP Pin to GND			20k		Ω
OUTN Pin to GND			20k		Ω

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Others					
Thermal Shutdown			150		°C
Max ON Time			30		μs
Propagation Delay	(Trigger=High) delay to OUTP and OUTN		60		ns

Typical Performance Characteristics

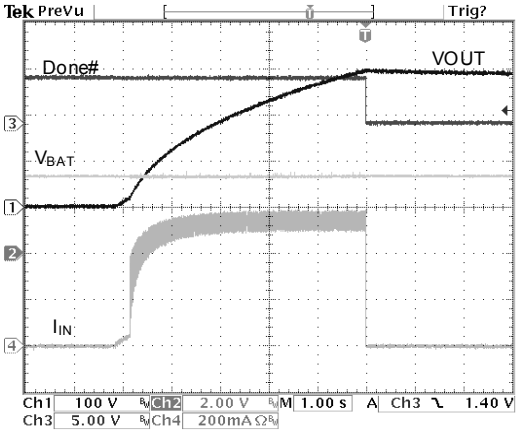


Fig. 5 Charging Waveform V_{BAT}=3V

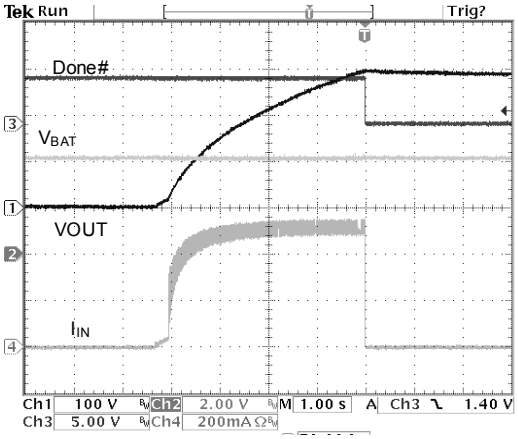


Fig. 6 Charging Waveform V_{BAT}=4.2V

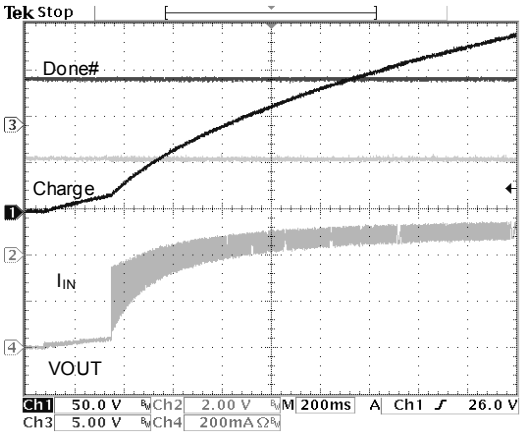


Fig. 7 Soft Start Function

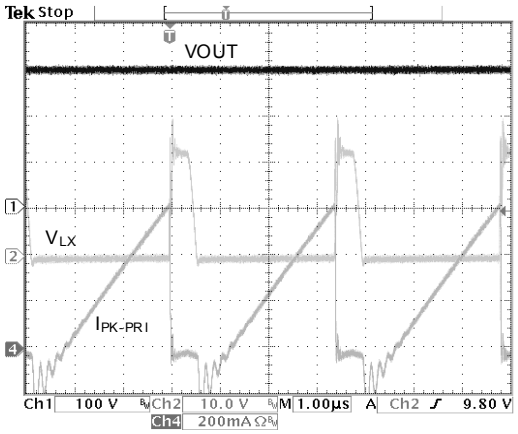


Fig. 8 Typical Switching Waveform

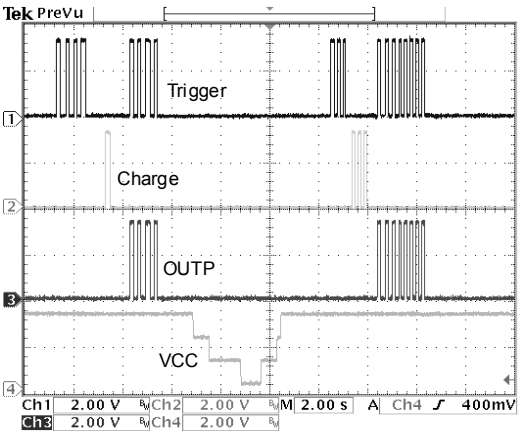


Fig. 9 False Triggering Prevention

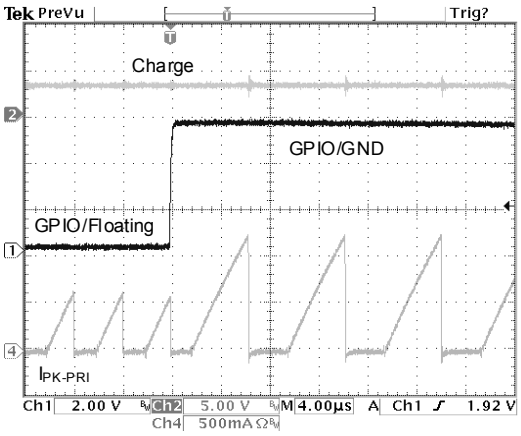


Fig. 10 Two Level charging Current Waveform

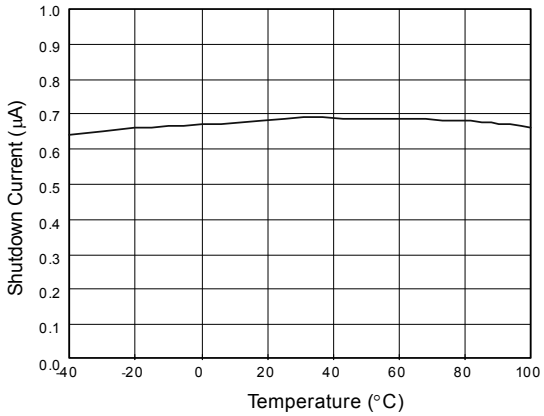


Fig. 11 Shut Down Current vs. Temperature

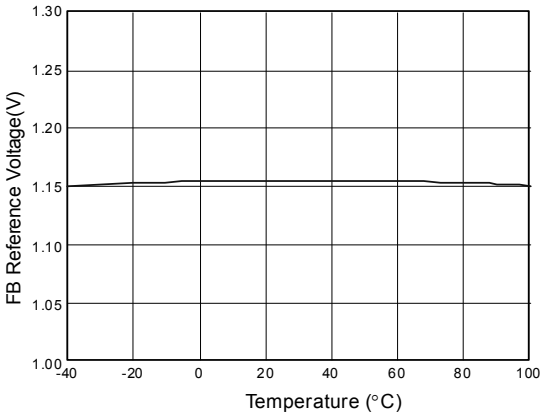


Fig. 12 FB Reference Voltage vs. Temperature

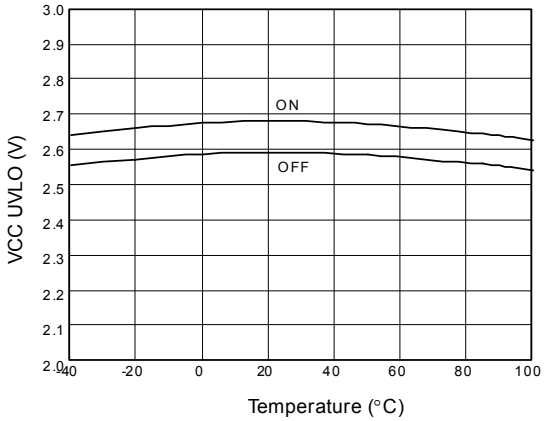


Fig. 13 VCC UVLO (ON/OFF) vs. Temperature

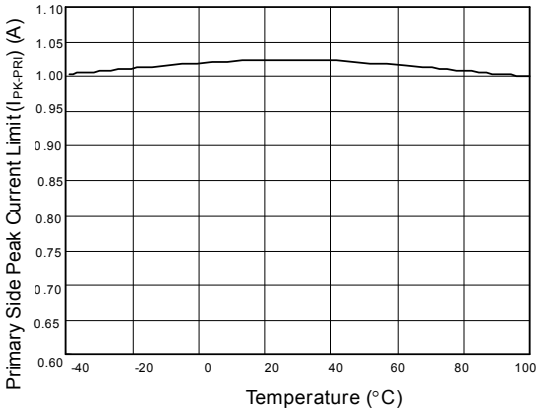


Fig. 14 Primary Side Peak Current Limit (R_I=40kΩ)

Function Description

Adjustable Charging Current

The primary side peak current of the transformer can be easily set by a resistor R_I connecting to ISET pin, which is shown as Fig. 15. The R_I value can be obtained according to the equation below.

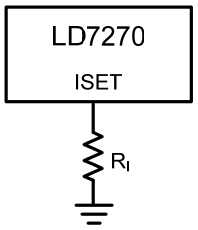


Fig. 15

$$R_I = \frac{40000}{I_{PK-PRI}} \quad (\Omega)$$

Where the I_{PK-PRI} is the primary side peak current of transformer. Users could select adaptive R_I according to the battery capability and desired charging current. Note that the adjustable maximum current is 1.8A.

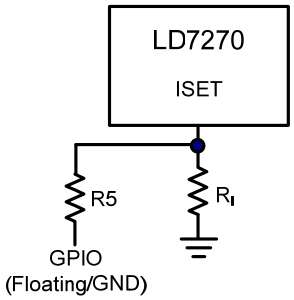


Fig. 16

Besides, the LD7270 can achieve two-level charging current setting according to GPIO interface status as shown in Fig. 16.

Ex: Assume R_I=R5=80kΩ, the primary side peak current corresponding to the GPIO status is shown in Fig.17.

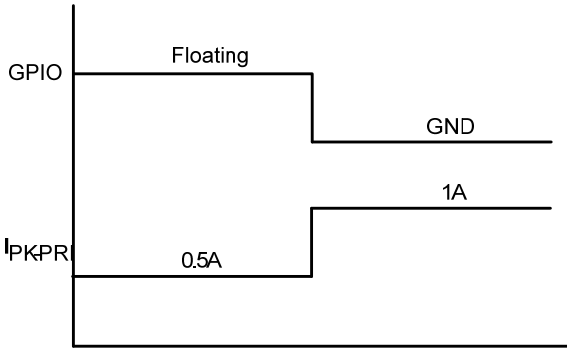


Fig. 17

Transformer Turn Ratio

A carefully chosen transformer could result in best performance of the LD7270. Also, the turn ratio of the transformer should be taken into consideration. The maximum voltage rating of the internal NMOS of the LD7270 is 47V. Thus, the turn ratio is obtained by:

$$N \geq \frac{V_{OUT} + V_{D1}}{47 - V_{BATMAX} - V_{SPIKE}}$$

N: turn ratio of transformer

V_{OUT}: target output voltage

V_{D1}: the forward voltage of D1.

If V_{OUT}=320V, V_{BATMAX}=6V and V_{SPIKE}=0V, the turn ratio N should be more than 8. In generally applications, the recommended turn ratio is 10~16.

Minimum Primary Inductance

To ensure accurate operation for the LD7270, the acceptable primary inductance, Lp (H), should meet the following formula:

$$L_P \geq \frac{275 \times 10^{-9} \times V_{OUT}}{N \times I_{PK-PRI}}$$

I_{PK-PRI}: the selected min primary current limit value during charging period

N: turn ratio of transformer

V_{OUT}: target output voltage

Ex1: N=14, V_{OUT}=300V, set primary side peak current limit value during operation, $I_{IPK-PRI}$=0. 6A
→ Lp ≥ 10μH.

In most applications, it's recommended to choose a transformer of L_P=6μH~15μH for V_{BAT} in the voltage range of 1.8V~6V.

Soft Start

The soft start will eliminate the inrush current at the beginning of charging process. When the output voltage is less than 20V, the LD7270 will set the lowest peak current limit (0.4A) to charge the capacitor. As output voltage rises up above 20V, the current limit will then rise up to the set current level. The advantage of this control scheme is to limit the initial inrush current and allow using a smaller input capacitor.

Minimum off time of V_{LX}

The acceptable minimum pulse of VLX should be larger than 400ns during the whole charging cycle. Otherwise, the FB signal detection scheme of LD7270 can't operate properly and will affect the accuracy of output voltage detection.

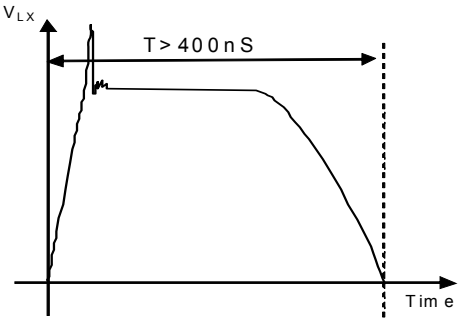


Fig. 18

Transformer Primary Leakage Inductance

The leakage inductance at the primary side of the transformer will result in the turn-off spike at LX pin. The spike should not exceed the dynamic rating of the LX pin. To restrict it, it's necessary to choose a transformer with lower leakage inductance.

Transformer Secondary Capacitance

Any capacitance on the secondary will severely affect the efficiency. The secondary capacitance is multiplied by N^2 when reflected to the primary side and cause it larger. This capacitance forms a resonant circuit with the primary leakage inductance of the transformer. Therefore, both the primary leakage inductance and secondary capacitance should be minimized.

As well, the LD7270 also builds in with over current protection of LX pin to avoid transformer saturation condition. If the primary current is over 3A, then the IC will latch off and stop switching.

False Triggering Prevention

The LD7270 also contains triggering prevention function, which can prevent IGBT from false triggering in case the trigger pin receives false triggering pulse from DSP during VCC power-on interval. See it as Fig. 19.

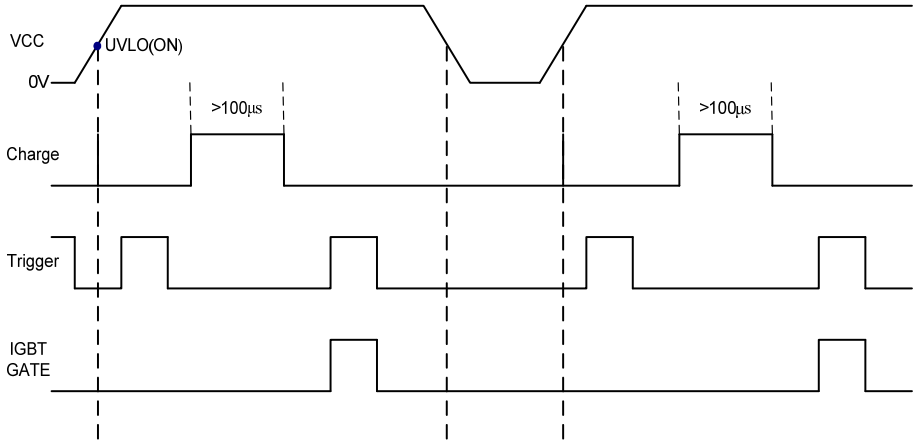


Fig. 19

The signal of IGBT gate will be high according to following sequence.

1. VCC>UVLO (ON) (typical 2.65V)
2. Charge pin is high (the pulse width should be larger than 100μs)
3. Trigger pin is high and charge pin is low.

Maximum ON Time

To protect against insufficient current from a poor power source (ie., an almost discharged battery) and unreachable current limit value, the LD7270 employs maximum on-time function for it. As soon as ON time of charging period exceeds 30μs, the LD7270 will be latched off in regardless of current limit detection.

Adjust Output Voltage

A resistor divider can be connected to the center of the dual diode to eliminate the leakage current after the charging completes. Fig.20 shows the application circuit of resistor divider.

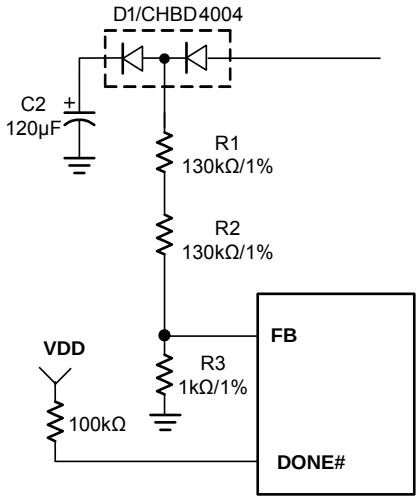


Fig. 20

$$V_{OUT} = 1.15 \times \left(1 + \frac{R1+R2}{R3}\right)$$

It's not recommended to choose the resistor larger than 1KΩ to connect with FB to GND (R3 in Fig. 20), since a larger resistor would combine with parasitic capacitance and affect the accuracy of V_{OUT} detection. As well, the switching nodes such as LX pin or secondary side of XFMR should be kept routed away from FB pin in such application of Fig.20 to obtain accurate V_{OUT} detection.

Output Voltage Overcharge Protection

As shown in Fig. 1, Fig. 2, Fig. 3 or Fig. 4, the FB pin may

fail to reach 1.15V during the charging cycle, either when the R3 is short to GND or R1 (or R2) open. It will cause V_{OUT} increase continuously till over the target value of output voltage. LD7270 features proprietary detecting scheme to effectively avoid this phenomenon.

IGBT Driver

LD7270 employs separate source and sink pin of IGBT driver, which enables the users to easily meet the requirement of any different IGBT applications. In addition, if VCC is below 2.55V (typ), OUTP and OUTN pin will be 0V even when TRIGGER pin is toggled.

Rectifying Diode Selection

It's preferable to choose a rectifying diode with less reverse recovery time to minimize the switching loss and increase the charging efficiency. And more, it would allow sufficient peak reverse voltage and peak forward current rating.

The peak reverse voltage is written as below.

$V_{PK-R}= V_{OUT}+N \times V_{BAT}+VS_{PIKE}$

The peak forward current is as below.

$I_{PK-SEC}= Ip / N$,

I_P: peak primary current (A),

N: turn ratio

Interface

CHARGE, DONE# and TRIGGER can be easily interfaced to a microprocessor.

The CHARGE pin is the ON/OFF control of charging circuit.

High=enable, Low =disable

The DONE# pin is an indicator of charging and output voltage state.

High= otherwise

Low= the charging is completed and CHARGE pin is high

The TRIGGER pin is the ON/OFF control of the strobe to generate a light pulse.

High=enable, Low =disable

Layout Consideration

1. The layout of this IC should follow the rule of high voltage isolation to avoid any breakdown failure of this IC and circuit board.
2. Keep the bypass capacitor 1μF very close to IC GND. (<5mm)
3. Refer to Fig.21, there should be no GND plane or GND path close to nodes of R1, R2 and R3.
4. Keep output voltage feedback network close to IC and far away from any interference nodes or paths.
5. The LX pin and GND Pin should be with large metal trace area.
6. The switching nodes, such as LX pin or anode of rectifying diode should be kept away from FB pin.
7. Please refer to Fig.21 and the EV kit for the PCB layout example.

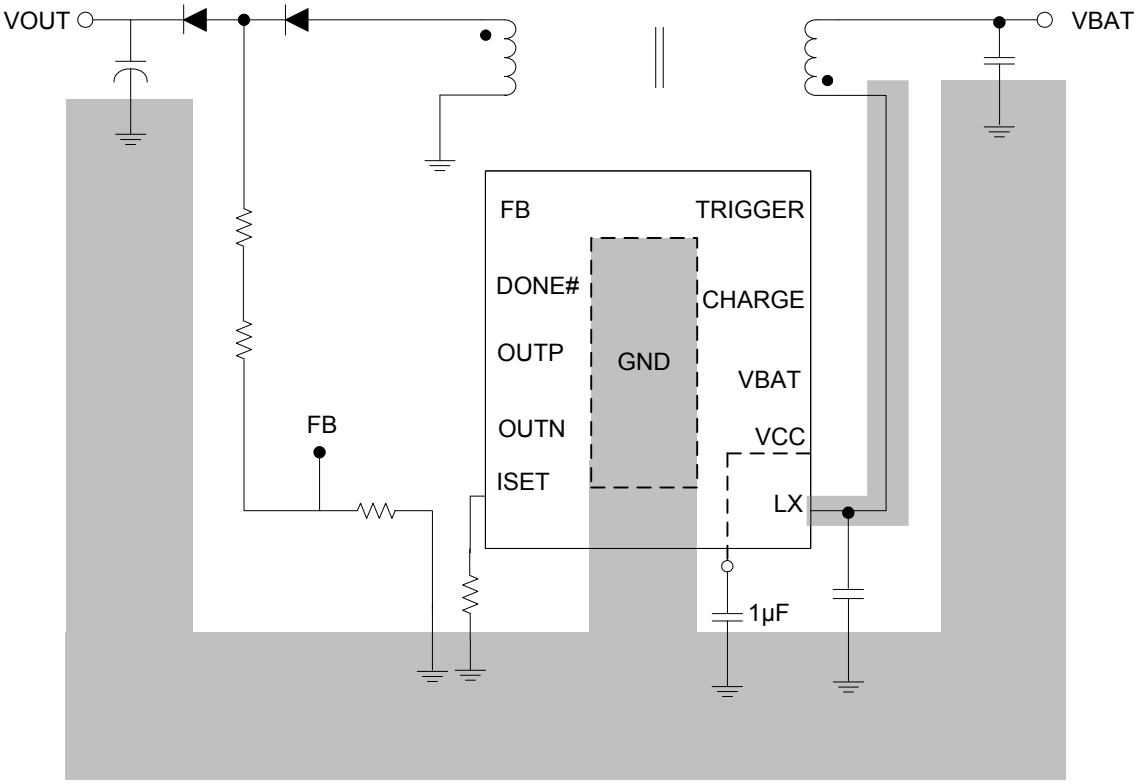


Fig. 21 Recommended PCB layout

Reference Design for DSC (IGBT solution)

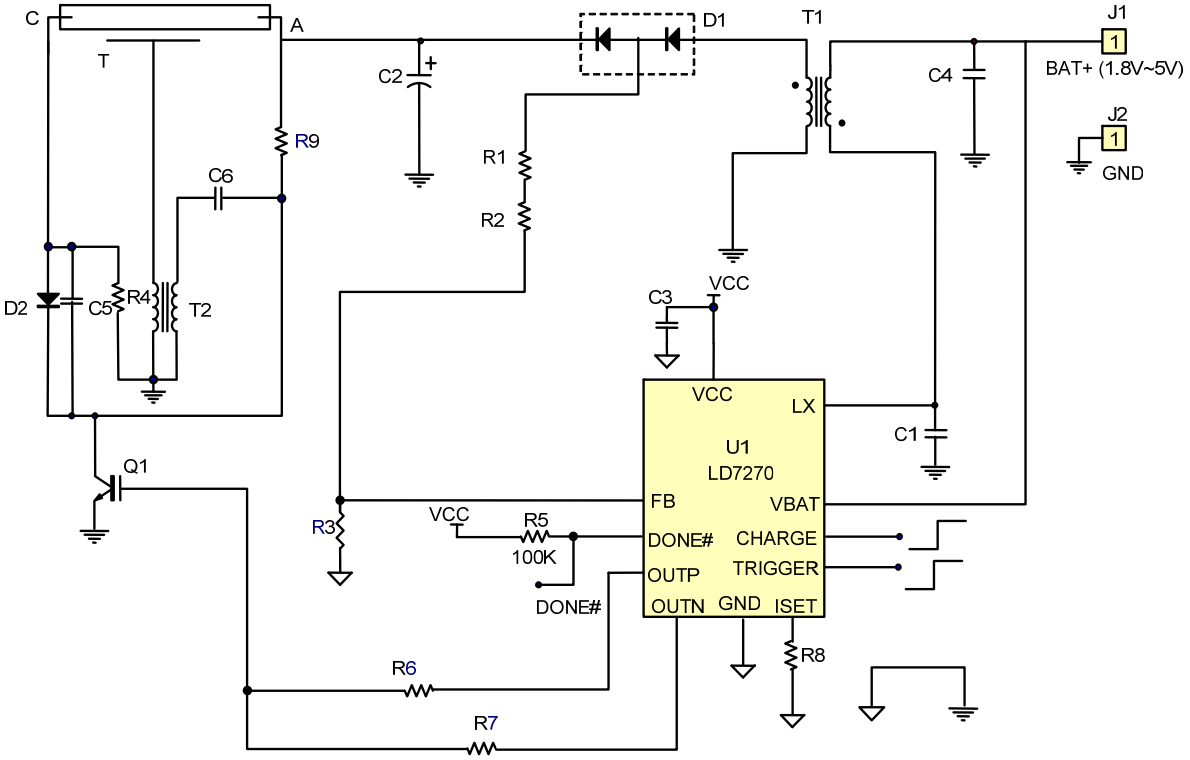


Fig. 22

BOM list

REF	Value	PART NO.	Package	Vendor
U1		LD7270	WDFN-10	Leadtrend
C1	220pF		0402	
C2	90μF/330V	FW Series	Radial	Rubycon
C3	1μF/X5R/6.3V		0603	
C4	22μF/X5R/6.3V		1206	
C5, C6	33nF/500V		1206	
R1, R2	130K/1%/200V		0603	
R3	1K/1%		0402	
R4	100K/300V		0805	
R5	100K		0402	
R6	0Ω		0402	
R7	30Ω		0402	
R8	40K		0402	
R9	1M/300V		0805	
D1		CHBD4004SPT	SOT-23	Chenmko
D2		RGF10M	SMA	Zowie
Q1		GT5G131	SOP-8	Toshiba
T1				
T2				

Reference Design for Camera Phone (IGBT solution)

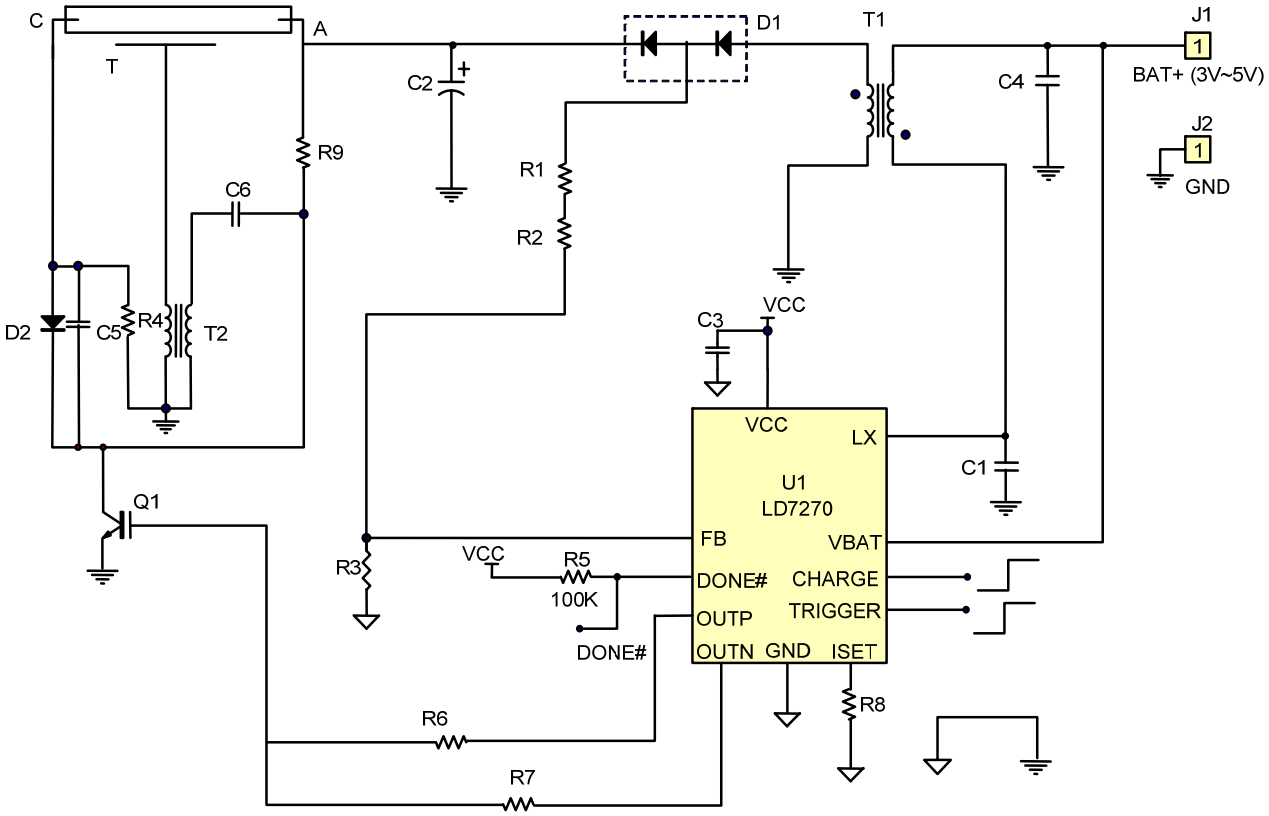


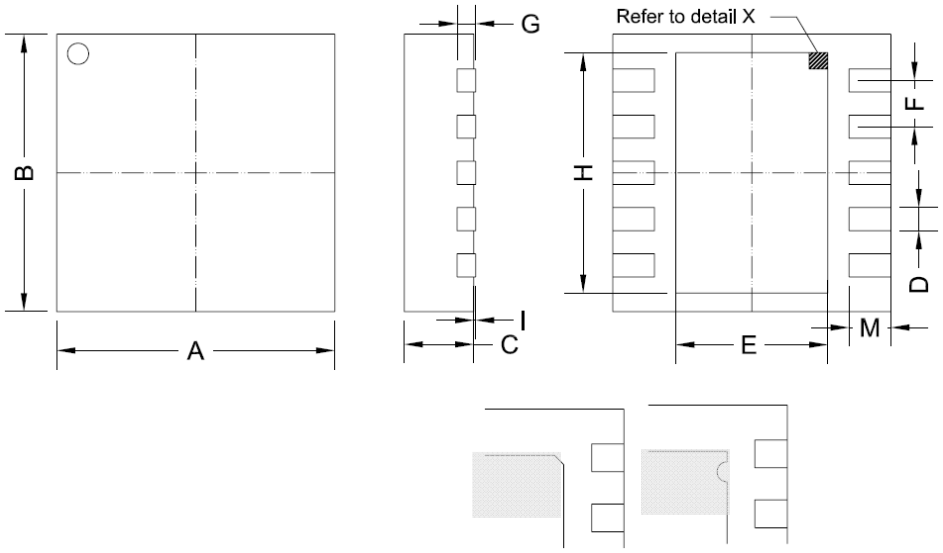
Fig. 23

BOM list

REF	Value	PART NO.	Package	Vendor
U1		LD7270	WDFN-10	Leadtrend
C1	220pF		0402	
C2	22μF/330V	FW Series	Radial	Rubycon
C3	1μF/X5R/6.3V		0603	
C4	22μF/X5R/6.3V		1206	
C5, C6	33nF/500V		1206	
R1, R2	130K/1%/200V		0603	
R3	1K/1%		0402	
R4	100K/300V		0805	
R5	100K		0402	
R6	0Ω		0402	
R7	82Ω		0402	
R8	40K		0402	
R9	1M/300V		0805	
D1		CHBD4004SPT	SOT-23	Chenmko
D2		RGF10M	SMA	Zowie
Q1		CY25CAH-8F	VSON8	Renesas
T1				
T2				

Package Information

WDFN-10L (3mm ×3mm)



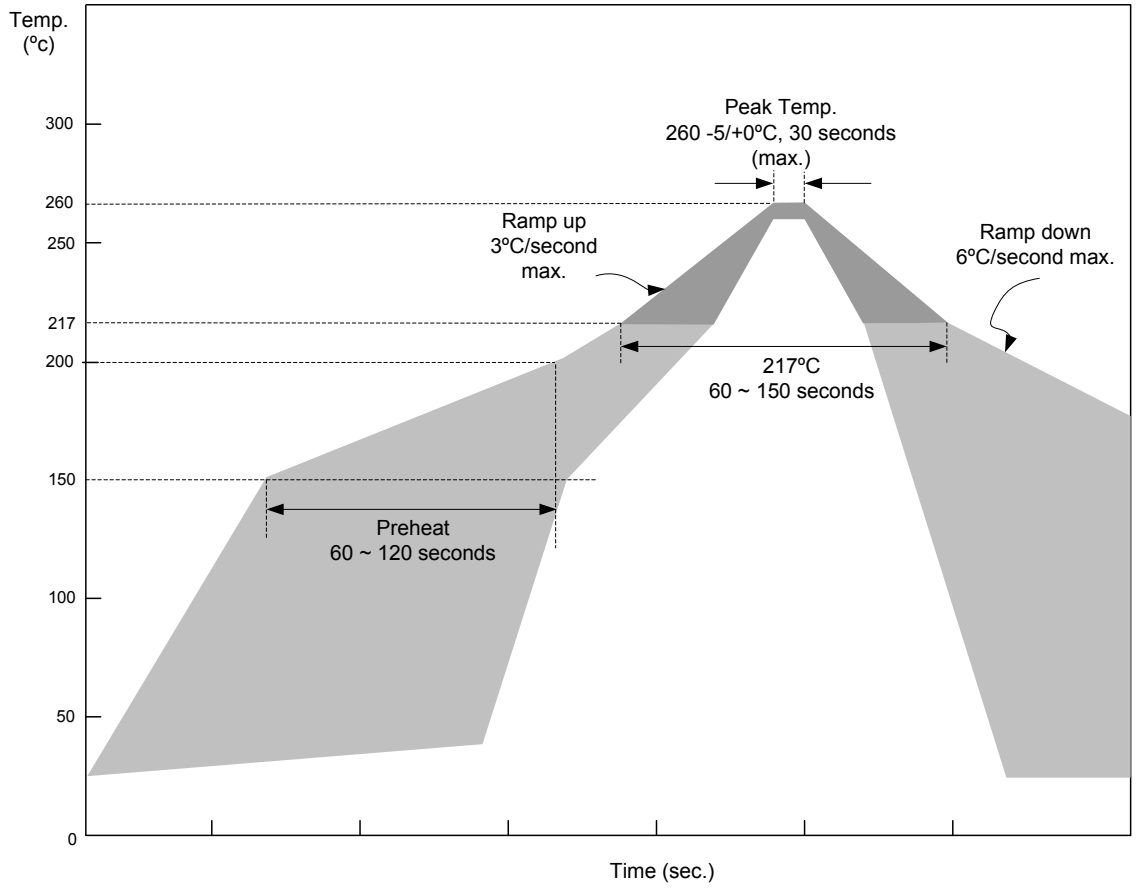
DETAIL X
THE CONFIGURATION OF THE PIN 1 IDENTIFIER IS OPTIONAL AS ABOVE.

Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	2.900	3.100	0.114	0.122
B	2.900	3.100	0.114	0.122
C	0.650	0.850	0.026	0.033
D	0.150	0.300	0.006	0.012
E	1.590	1.70	0.043	0.067
F	0.50 TYP.		0.020 TYP.	
G	0.20 REF		0.008 REF.	
H	2.100	2.650	0.083	0.104
I	0.000	0.050	0.000	0.002
M	0.400	0.500	0.016	0.020

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

IR Profile for SMD Devices



Item	Average Ramp-up Rate	Pre-heat (150 ~ 200°C)	Time Maintained Above 217°C	Peak Temp.	Ramp-down Rate
Required	3°C(max) /sec	60~120 sec	60~150 seconds	260 +0/-5°C 30 seconds	6°C (max) /sec

Revision History

Rev.	Date	Change Notice
00	3/19/2009	Original Specification
01	6/8/2009	Electrical Characteristics: Under Voltage Lock Out (OFF): 2.55V typ.
01a	11/19/2009	Typical application circuit update
02	1/18/2010	Enhancement for the max. voltage rating of LX pin. (43V)
03	6/18/2010	Enhancement for the max. voltage rating of LX pin. (47V)