Smart Photoflash Capacitor Charger with Integrated MOS

REV：02

General Description

The LD7271 is an ideal charge control IC for flash units, featuring internal soft start, adjustable charging current and output voltage. It provides a charging algorithm to speed up the charging with higher efficiency. The LD7271 can operate in desired constant peak current of eight different levels between 0.6A and 1.3A, by clocking the CHARGE pin.

The LD7271 is available in a space-saving W DFN-8L 2mm x 2mm package and is ideal for DSC flash unit.

† Patented

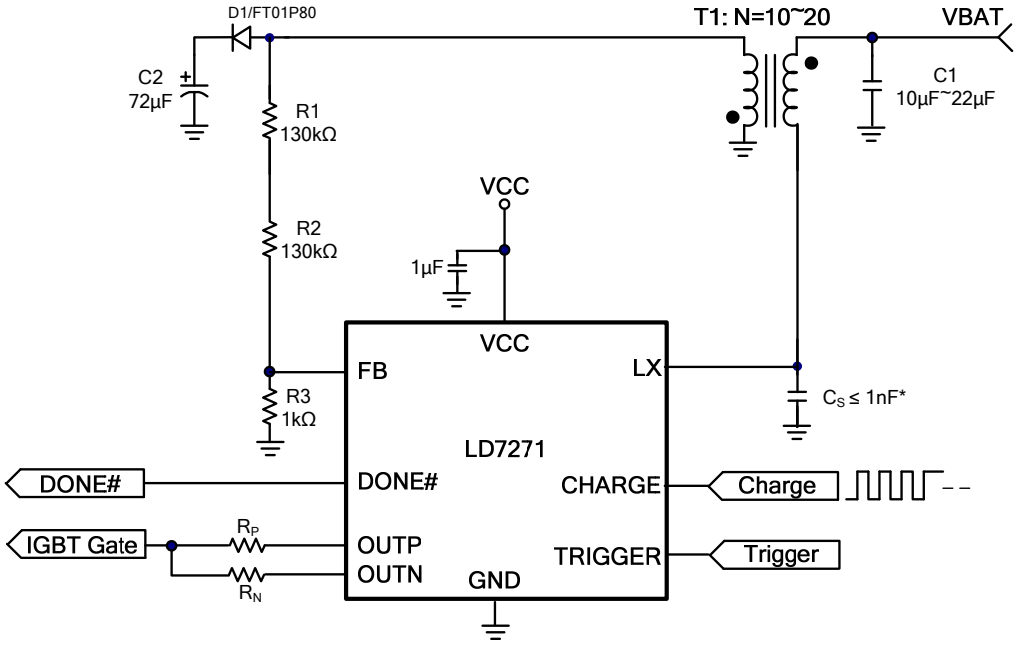
Features

- 1.8V~6V Battery Voltage Range
- Adjustable Output Voltage
- Adjustable Input Current
- Integrated 47V Power MOS
- False Triggering Prevention
- Soft Start
- Output Voltage Overcharge Protection
- High Efficiency

Applications

- DSC Flash Unit
- Camera Phone

Typical Application

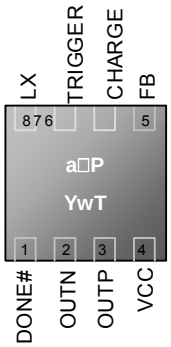


* If LX pin spike is over 47V, please add C_S to reduce spike.
C_S ≤ 1nF is recommended.

Fig.1

Pin Configuration

WDFN-8 (2mm x 2mm)



a: LD7271
□ : Blank space
p: Production code
Y : Year Code
W : Week Code
T: T hickness
W: 0.75mm (typical)

Ordering Information

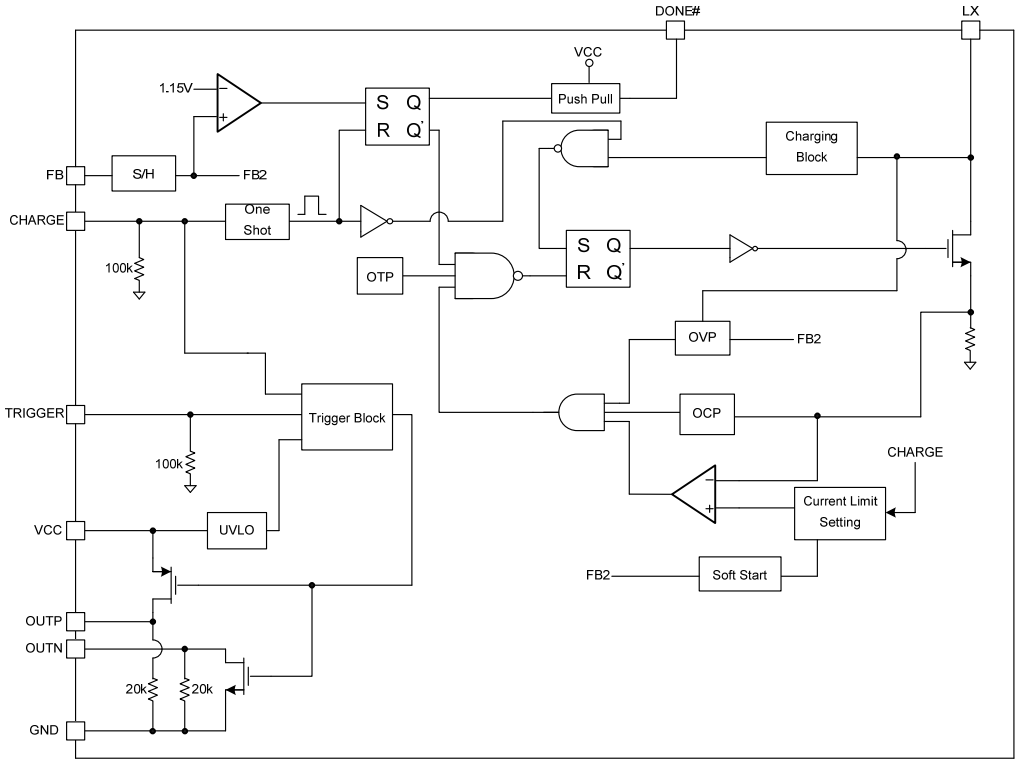
Part number	Package		Top Mark	Shipping
LD7271GDDW	WDFN-8L 2x2	Green Package	a□P	2500 /tape & reel

The LD7271 is green packaged.

Pin Descriptions

PIN N	AME	FUNCTION
1	DONE#	Charge Done Indicator. DONE# is a push-pull drain output that pulls low when CHARGE is high and the circuit has finished charging the output capacitor.
2	OUTN	IGBT driver sink output pin.
3	OUTP	IGBT driver source output pin.
4	VCC	Input power of IC. Bypass with a 1μF ceramic capacitor close to IC GND.
5	FB	Output voltage feedback
6	CHARGE	Charging on/off control.
7	TRIGGER	Trigger on/off control.
8	LX	NMOS drain pin. Connect to transformer primary as shown in Fig.1.
Exposed Metal Pad	GND	IC GND. Exposed pad should be soldered to PCB board with a larger area

Block Diagram



Absolute Maximum Ratings

VCC, CHARGE, TRIGGETR, DONE#, OUTP, OUTN, pin	-0.3V~ 6.5V
FB pin	-0.45V~ 6.5V
LX pin<200ns	-0.3V~ 47V
DC	-0.3V~ 42V
LX Current	3.3A
Power Dissipation, P_D@T_A=25°C (WDFN-8L 2 x 2)	606mW
Package Thermal Resistance (WDFN-8L 2 x 2), θ_{JA}	165 °C/W
Operating Ambient Temperature Range	-30 °C to 85°C
Operating Junction Temperature Range	-30 °C to 125°C
Maximum Junction Temperature	150 °C
Storage Temperature Range	-50 °C to 150°C
Lead Temperature (Soldering, 10sec)	260 °C
ESD Level (Human Body Model)	2kV
ESD Level (Machine Model)	200V

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=3.3V)

PARAMETER CONDITIONS		MIN	TYP	MAX	UNITS
Input Power					
Operating Voltage V_{CC}		2.8		5.5	V
Under Voltage Lock Out (ON)			2.65		V
Under Voltage Lock Out (OFF)			2.55		V
Shutdown Current I_{CC} Charge=Off,	Trigger=Off		1.5	3	μA
Nominal Supply Current	V_{CC}=3.3V, D=50%	1			mA
FB					
Reference Voltage		1.15			V
Reference Voltage Tolerance		-1.5		+1.5	%
Sample time of FB detection		225	250	275	ns
LX pin					
On resistance	I_{LX}=1.3A		250	330	mΩ
LX leakage current	VLX=42V			5	μA
Current Setting					
I_{ILM1}		0.555	0.6	0.645	A
I_{ILM2}*		0.647	0.7	0.753	A
I_{ILM3}*		0.74	0.8	0.86	A
I_{ILM4}*		0.832	0.9	0.968	A
I_{ILM5}*		0.925	1.0	1.075	A
I_{ILM6}*		1.017	1.1	1.183	A
I_{ILM7}*		1.11	1.2	1.29	A
I_{ILM8}*		1.202	1.3	1.398	A
IGBT Driver					
OUTP ON Resistance	V_{CC}=3.1V		2	3	Ω
OUTN OFF Resistance	V_{CC}=3.1V		40	50	Ω
ON/OFF					
Trigger On/Off	Enabled 1.4				V
	Disabled			0.6	V
Charge On/Off	Enabled 1.4				V
	Disabled			0.6	V

PARAMETER CONDITIONS		MIN	TYP	MAX	UNITS
DONE#					
DONE# Output Low Voltage	$I_{DONE\#}$=1mA		0.1		V
DONE# Output High Voltage	$I_{DONE\#}$=-1mA, V_{CC}-$V_{DONE\#}$		0.1		V
Impedance to GND					
Charge Pin to GND			100k		Ω
Trigger Pin to GND			100k		Ω
OUTP Pin to GND			20k		Ω
OUTN Pin to GND			20k		Ω
I_{PEAK} Clock high and low time of Charge Pin	Subsequent Pulses	2			μs
Total clock pulse setting time of Charge Pin			200		μs
Others					
Thermal Shutdown		150			°C
Max ON Time			30		μs
Propagation Delay	(Trigger=High) delay to OUTP and OUTN		60		ns

* I_{LM2-8} are guaranteed by design.

Typical Performance Characteristics

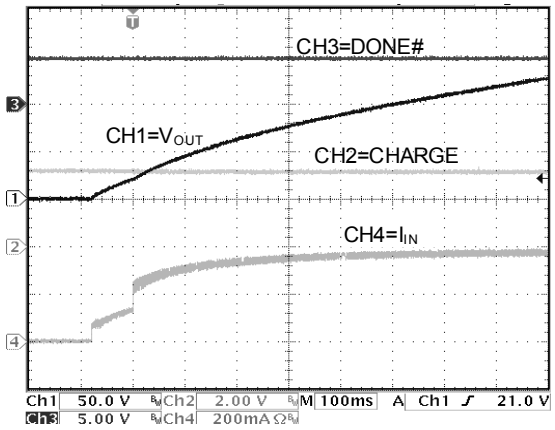


Fig. 2 Soft Start Function

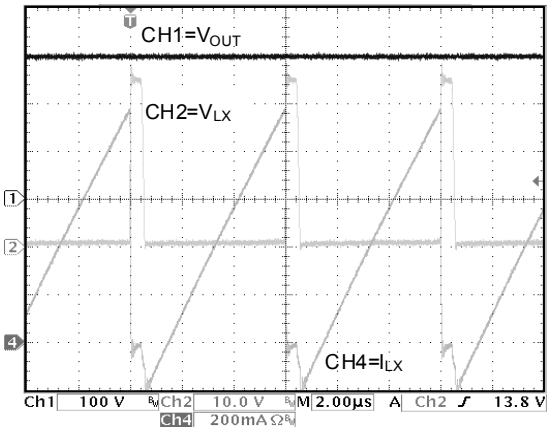


Fig. 3 Typical Switching Waveform

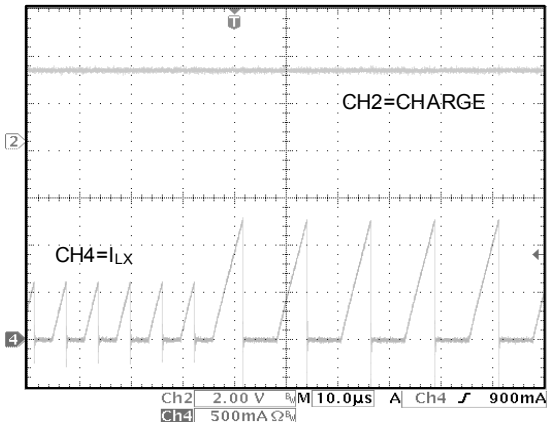


Fig. 4 Two Level Charging Current Waveform

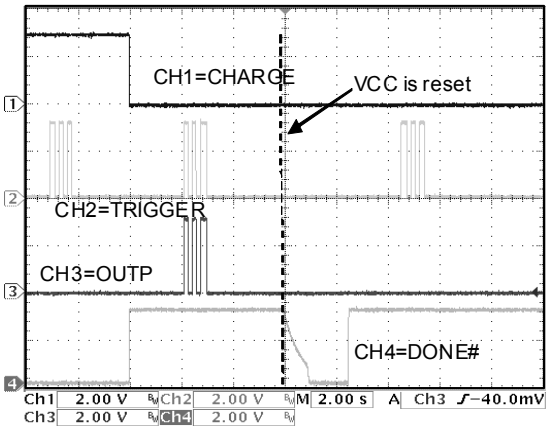


Fig. 5 False Triggering Prevention

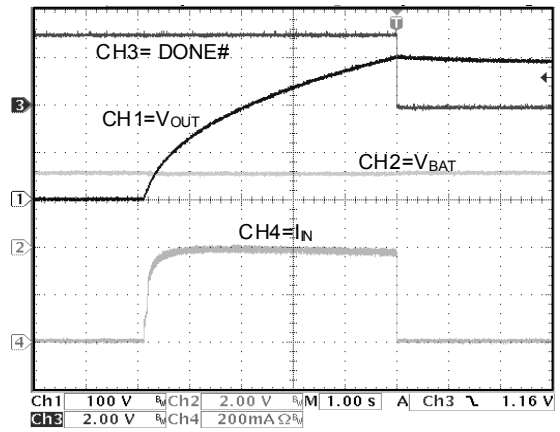


Fig. 6 Charging Waveform VBAT=3V

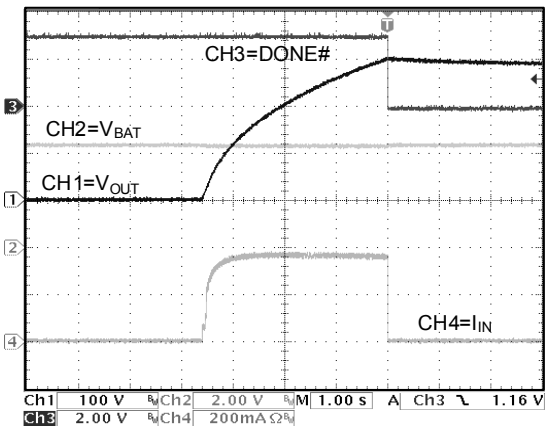


Fig. 7 Charging Waveform VBAT=4.2V

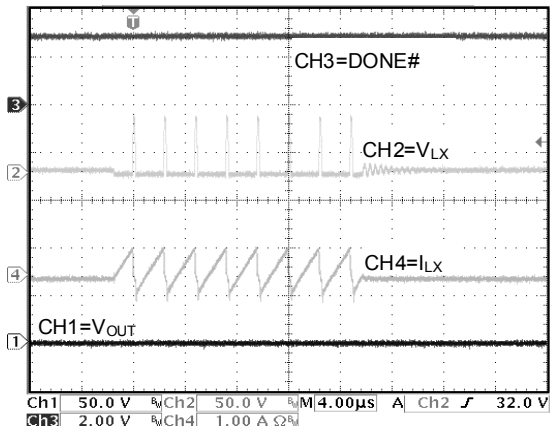


Fig. 8 Secondary Diode Open Circuit V_{BAT}=V_{CC}=4.2V

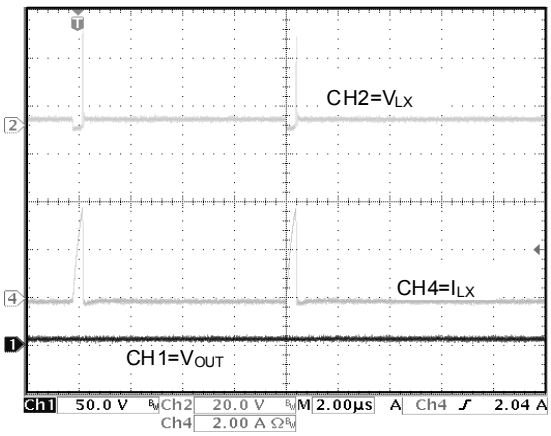


Fig. 9 T1 Secondary Side Short Circuit V_{BAT}=V_{CC}=4.2V

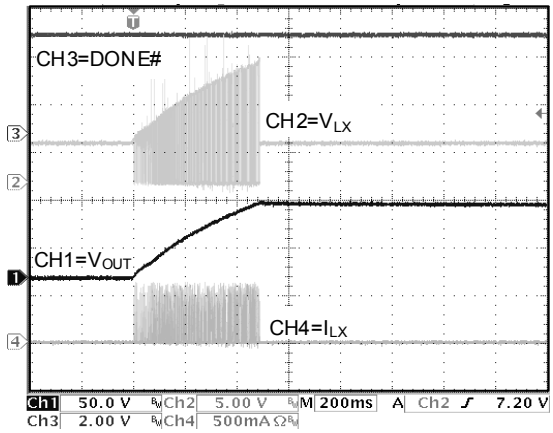


Fig. 10 FB Path Open Circuit (R1 or R2)

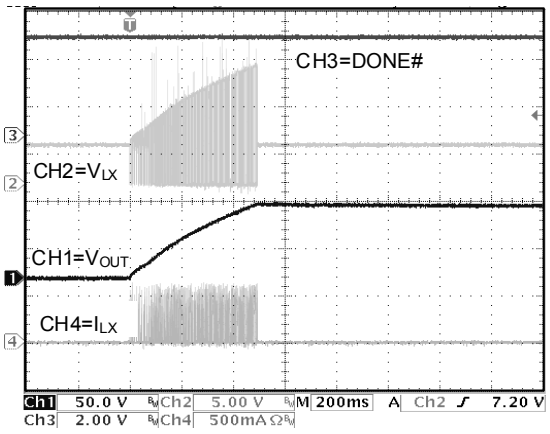


Fig. 10 FB Path Short Circuit (R3=0) V_{BAT}=V_{CC}=4.2V

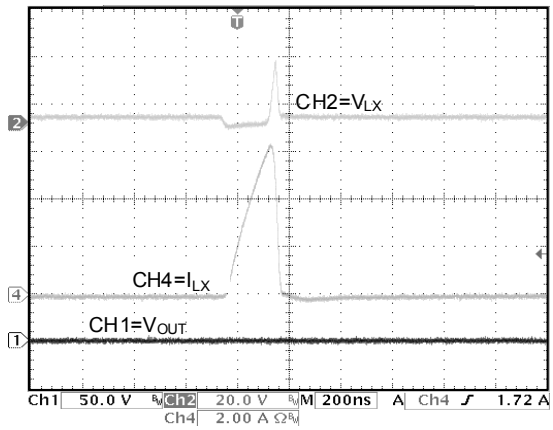


Fig. 11 Primary Side Inductor Short Circuit V_{BAT}=V_{CC}=4.2V

Function Description

Adjustable Charging Current

The primary side peak current is adjustable to eight different levels between 0.6A and 1.3A, by clocking the CHARGE pin, which is shown as Fig. 12.

The total charging current setting time of charge clock must be set within 200 µs from the first edge to the last low-to-high edge.

The minimum pulse width from low-to-high to high-to-low must be larger than 2µs at least during current setting time interval.

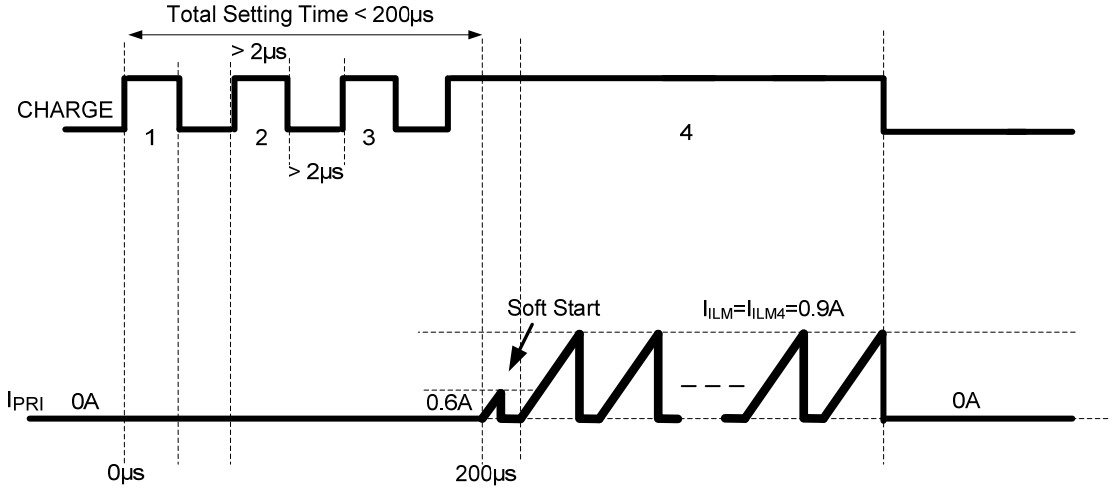


Fig. 12 I_{IILM} Clock Timing Definition

Transformer Turn Ratio

A carefully chosen transformer can result in best performance of the LD7271. Also, the turn ratio of the transformer should be taken into consideration. The maximum voltage rating of the internal NMOS for LD7271 is 47V. Thus, the turn ratio is obtained by:

$$N \geq \frac{V_{OUT} + V_{D1}}{47 - V_{BATMAX} - V_{SPIKE}}$$

N: turn ratio of transformer

V_{OUT}: target output voltage

V_{D1}: the forward voltage of D1.

If V_{OUT}=320V, V_{BATMAX}=6V and V_{SPIKE}=0V, the turn ratio N should be more than 8. In generally applications, the recommended turn ratio is 10~20.

Minimum Primary Inductance

To ensure accurate operation for the LD7271, the acceptable primary inductance, Lp (H), should meet the following formula:

$$L_P \geq \frac{275 \times 10^{-9} \times V_{OUT}}{N \times I_{PK\text{-}PRI}}$$

I_{PK-PRI}: the selected min primary current limit value during charging period

N: turn ratio of transformer

V_{OUT}: target output voltage

Ex1: N=14, V_{OUT}=300V, set primary side peak current limit value during operation, $I_{IPK-PRI}$=0.6A
→ Lp ≥ 10μH.

In most applications, it's recommended to choose a transformer of L_P=6μH~15μH for V_{BAT} in the voltage range of 1.8V~6V.

Soft Start

The soft start will eliminate the inrush current at the beginning of charging process. When the output voltage is less than 20V, the LD7271 will set the lowest peak current limit (0.6A) to charge the capacitor. As output voltage rises up above 20V, the current limit will then rise up to the set current level. The advantage of this control scheme is to limit the initial inrush current and allow using a smaller input capacitor.

Minimum off time of V_{LX}

The acceptable minimum pulse of VLX should be larger than 400ns during the whole charging cycle. Otherwise, the FB signal detection scheme of LD7271 can't operate properly and will affect the accuracy of output voltage detection.

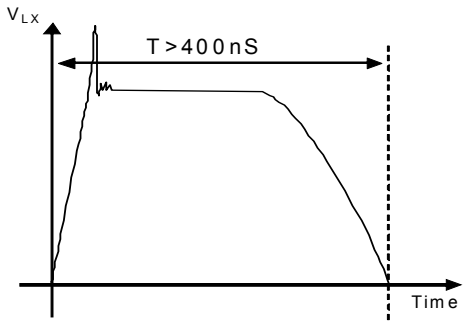


Fig. 13

Transformer Primary Leakage Inductance

The leakage inductance at the primary side of the transformer will result in the turn-off spike at LX pin. The spike should not exceed the dynamic rating of the LX pin. To restrict it, it's necessary to choose a transformer with lower leakage inductance.

Transformer Secondary Capacitance

Any capacitance on the secondary will severely affect the efficiency. The secondary capacitance is multiplied by N^2 when reflected to the primary side and cause it larger. This capacitance forms a resonant circuit with the primary leakage inductance of the transformer. Therefore, both the primary leakage inductance and secondary capacitance should be minimized.

As well, the LD7271 also builds in with over current protection of LX pin to avoid transformer saturation condition. If the primary current is over 3A, then the IC will latch off and stop switching.

False Triggering Prevention

The LD7271 also consist of false triggering prevention function, which can prevent IGBT from false triggering in case the trigger pin receives false triggering pulse from DSP during VCC power-on interval. See it as Fig. 14.

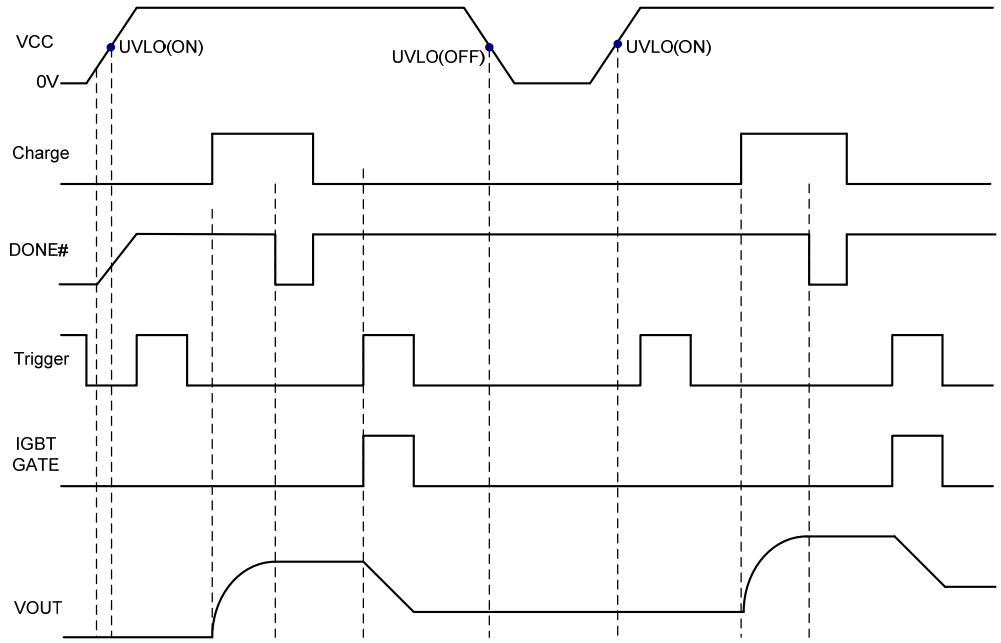


Fig. 14

The signal of IGBT gate will be high according to following sequence.

1. VCC>UVLO (ON) (typical 2.65V)
2. Charge pin turned to low once and DONE# pin turned to low once.
3. Trigger pin is high and charge pin is low.

Maximum ON Time

To protect against insufficient current from a poor power source (i.e., an almost discharged battery) and unable to reach current limit value in time, the LD7271 will employ maximum on- time function for it. Once ON-time of charging period exceeds 30μs, the LD7271 will be latched off in regardless of current limit detection.

Adjust Output Voltage

A resistor divider can be connected to the center of the dual diode to eliminate the leakage current after the charging completes. Fig.15 shows the application circuit of resistor divider.

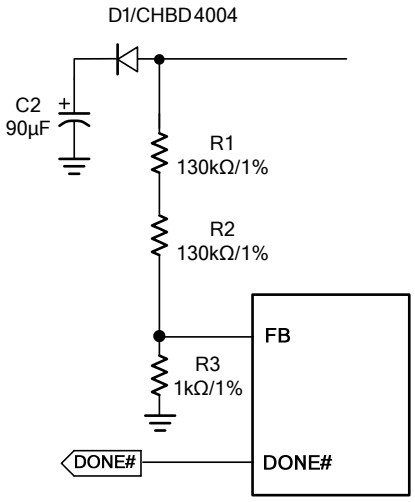


Fig. 15

$$V_{OUT} = 1.15 \times \left(1 + \frac{R1+R2}{R3}\right)$$

It's not recommended to choose a resistor larger than 1KΩ to connect with FB to GND (R3 in Fig. 15), since a larger resistor would carry parasitic capacitance and affect the accuracy of V_{OUT} detection. As well, the switching nodes such as LX pin or secondary side of XFMR should be routed away from FB pin in such application as Fig. 20 to obtain accurate V_{OUT} detection.

Output Voltage Overcharge Protection

As shown in Fig. 1, the FB pin may fail to reach 1.15V during the charging cycle, neither when the R3 is short to GND or R1 (or R2) open. It will cause V_{OUT} increase continuously till over the target value of output voltage. LD7271 features proprietary detecting scheme to effectively avoid this phenomenon.

IGBT Driver

LD7271 employs separate source and sink pin of IGBT driver, which enables the users to easily meet the requirement of any different IGBT applications. In addition, if VCC is below 2.55V (typ), OUTP and OUTN pin will be 0V even when TRIGGER pin is toggled.

Rectifying Diode Selection

It's preferable to choose a rectifying diode with less reverse recovery time to minimize the switching loss and increase the charging efficiency. And more, it would allow sufficient peak reverse voltage and peak forward current rating.

The peak reverse voltage is written as below.

$V_{PK-R}= V_{OUT}+N\times V_{BAT}+VS_{PIKE}$

The peak forward current is as below.

$I_{PK-SEC}= Ip / N$,

I_P: peak primary current (A),

N: turn ratio

Interface

CHARGE, DONE# and TRIGGER can be easily interfaced to a microprocessor.

The CHARGE pin is the ON/OFF control of charging circuit.

High=enable, Low =disable

The DONE# pin is an indicator of charging and output voltage state.

High= otherwise

Low= the charging is completed and CHARGE pin is high

The TRIGGER pin is the ON/OFF control of the strobe to generate a light pulse.

High=enable, Low =disable

Abnormal Operation Protection

LD7271 features many protections against abnormal operation, likes secondary diode open circuit, feedback resistor open circuit and primary side inductor short circuit etc. Refer it to the figures from Fig. 8~11 for the actually test waveforms.

Layout Consideration

1. Please follow the layout guide below for high voltage isolation to avoid any breakdown failure.
2. Place the C_{VCC} bypass capacitor of 1μF very close to IC GND. (<5mm)
3. Refer to Fig.16; please route GND plane or GND path away from nodes of R1, R2 and R3.
4. Keep output voltage feed back network close to IC and far away from any interference nodes or paths.
5. Place LX pin and GND Pin with large metal trace area.
6. The switching nodes, such as LX pin or anode of rectifying diode should be kept away from FB pin.
7. Please refer to Fig.16 and the EV kit for the PCB layout example.

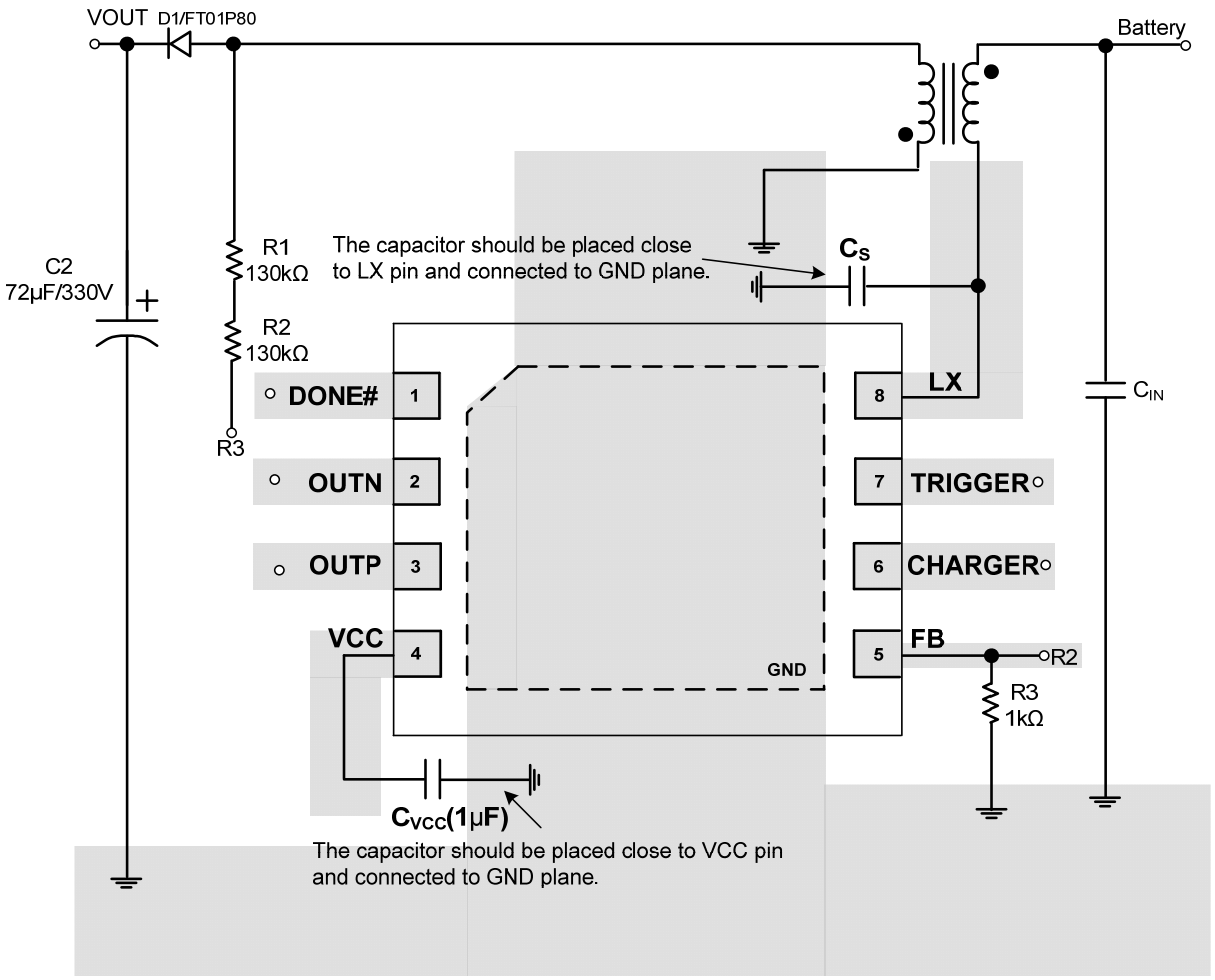
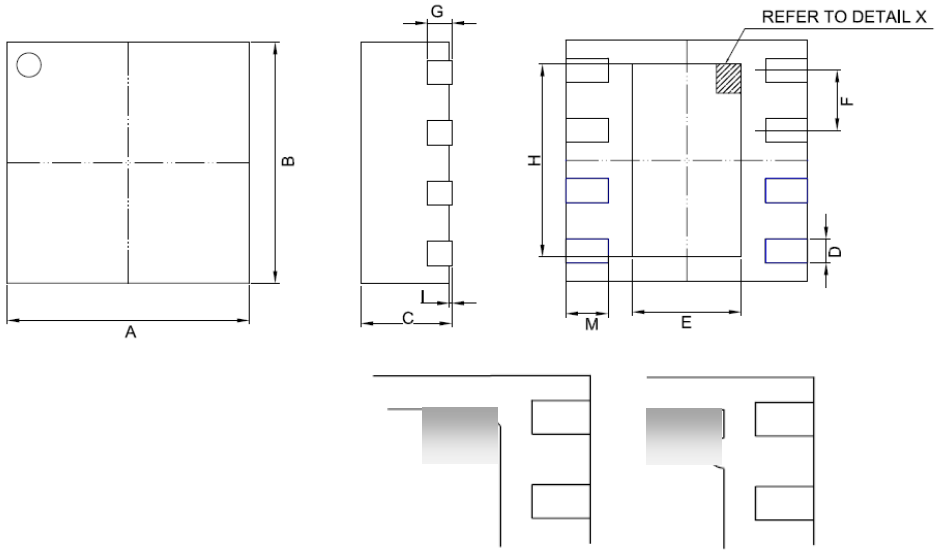


Fig. 16 Recommended PCB layout

Package Information

WDFN-8L



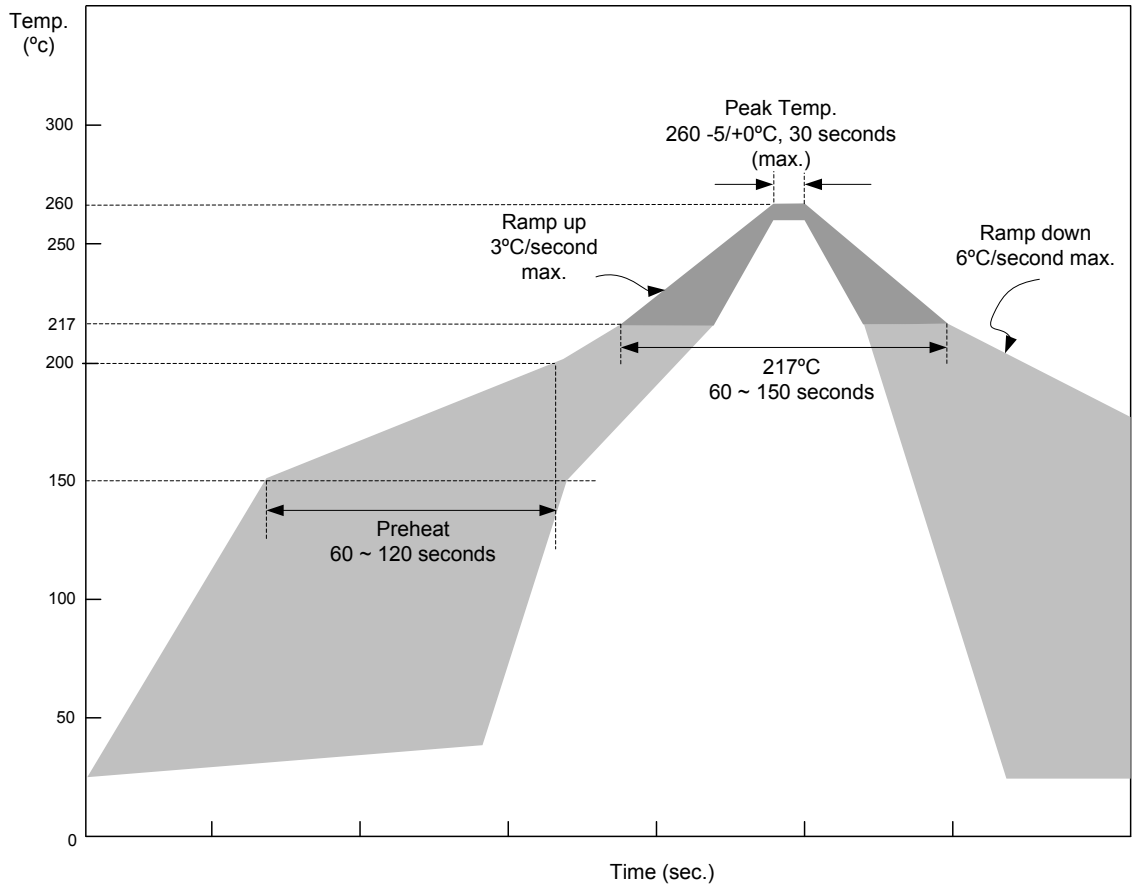
DETAIL X
THE CONFIGURATION OF THE PIN 1
IDENTIFIER IS OPTIONAL AS ABOVE.

Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	1.900	2.100	0.075	0.083
B	1.900	2.100	0.075	0.083
C	0.650	0.850	0.026	0.033
D	0.150	0.300	0.006	0.012
E	0.550	0.950	0.022	0.037
F	0.5 TYP.		0.02 TYP.	
G	0.190	0.250	0.007	0.01
H	1.150	1.650	0.045	0.065
I	0.000	0.050	0.000	0.002
M	0.300	0.400	0.012	0.016

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

IR Profile for SMD Devices



Item	Average Ramp-up Rate	Pre-heat (150 ~ 200°C)	Time Maintained Above 217°C	Peak Temp.	Ramp-down Rate
Required	3°C(max) /sec	60~120 sec	60~150 seconds	260 +0/-5°C 30 seconds	6°C (max) /sec

Revision History

Rev.	Date	Change Notice
00	2/22/2011	Original Specification
01	8/10/2011	Revision: Lx leakage current condition in Electrical Characteristics from 47V to 42V.
02	9/13/2011	Revision: Total clock pulse setting time of Charge Pin: 200μS. (was 80μS) Shunt down current: 1.5μA (Typ.) 3.0μA (Max.) (was 1.5μA, Max)