ACPI-STR Controller

REV: 00

General Description

The LD7301/02 is an ACPI-compliant controller for the applications of microprocessor and computers. It integrates a switch controller to generate a 5VDL from ATX power supply, a linear controller VDDQ and a bus terminator VTT controller. As well, it supports DDRI and DDRII with dual modes.

The device also integrates a charge pump engine, which enables to drive a NMOS application. As well, the LD7301/02 also offers power OK status checking and reporting, under voltage detection, soft start and shutdown function necessary for complete ACPI implementation.

The LD7301/02 is available in a space saving SSOP-20 package.

+ Patent Pending

Features

- Dual Modes of Configuration
- Under Voltage Protection
- Power OK status checking and reporting
- Soft Start Function
- Shutdown Function
- Drives all NMOS Designs
- +1, -1.5% accuracy for
  2.6V (mode A) and 1.8V (mode B)
- DDR reverse plug in protection

Applications

- ACPI-Compliant Power Regulation for Motherboard

Typical Application

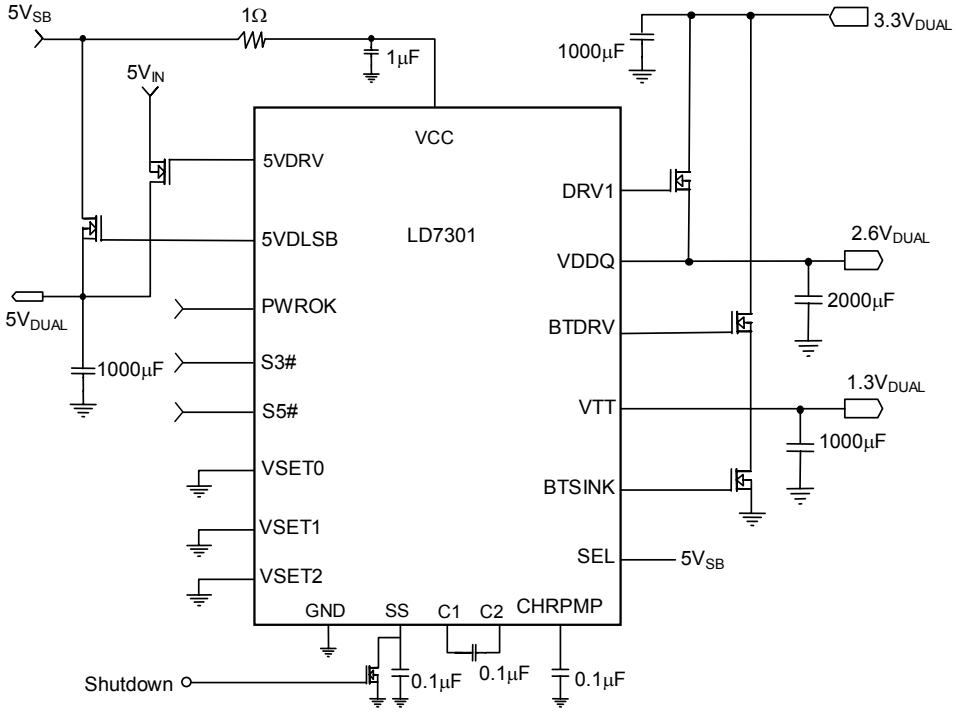


Fig. 1 The Application Circuit for Mode A of LD7301

Note: The LD7301 is for 5V Logic System

Mode A	SEL	VSET0	VSET1	VSET2	VDDQ	VTT
DDRI	5V	0V	0V	0V	2.6V$_{DUAL}$	1.30V$_{DUAL}$
	5V	0V	2.5V	0V	2.7V$_{DUAL}$	1.35V$_{DUAL}$
	5V	0V	5V	0V	2.8V$_{DUAL}$	1.40V$_{DUAL}$
	5V	5V	0V	0V	2.9V$_{DUAL}$	1.45V$_{DUAL}$
	5V	5V	2.5V	0V	3.0V$_{DUAL}$	1.50V$_{DUAL}$
	5V	5V	5V	0V	3.1V$_{DUAL}$	1.55V$_{DUAL}$

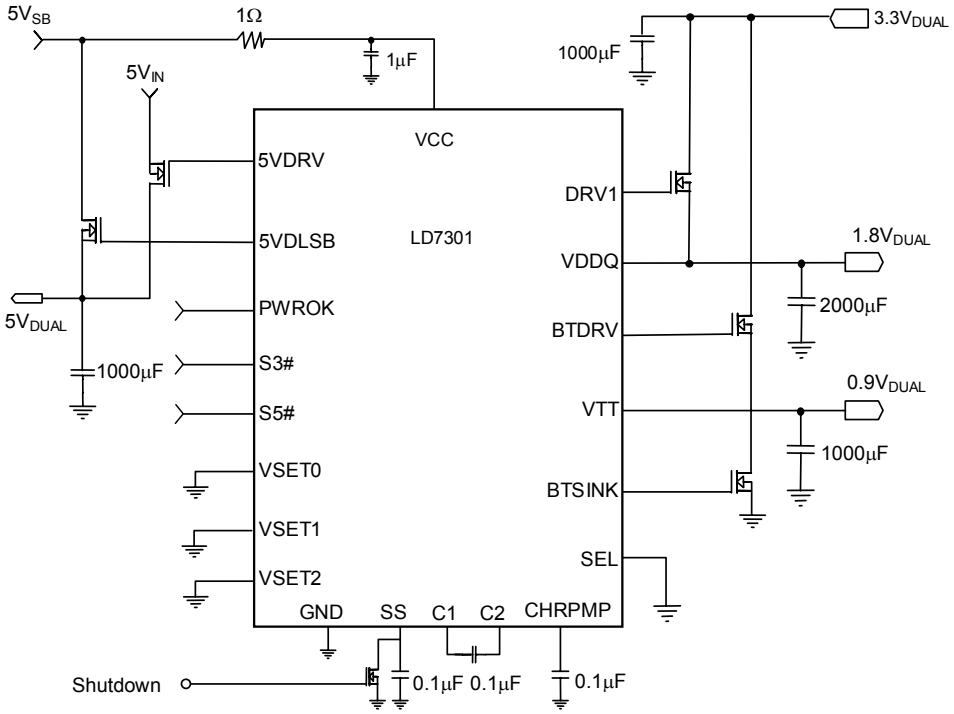


Fig.2 The Application Circuit for Mode B of the LD7301

Note: LD7301 is for 5V Logic System

Mode B	SEL	VSET0	VSET1	VSET2	VDDQ	VTT
DDRII	0V	0V	0V	0V	1.8V$_{DUAL}$	0.90V$_{DUAL}$
	0V	0V	2.5V	0V	1.9V$_{DUAL}$	0.95V$_{DUAL}$
	0V	0V	5V	0V	2.0V$_{DUAL}$	1.00V$_{DUAL}$
	0V	5V	0V	0V	2.1V$_{DUAL}$	1.05V$_{DUAL}$
	0V	5V	2.5V	0V	2.2V$_{DUAL}$	1.10V$_{DUAL}$
	0V	5V	5V	0V	2.3V$_{DUAL}$	1.15V$_{DUAL}$

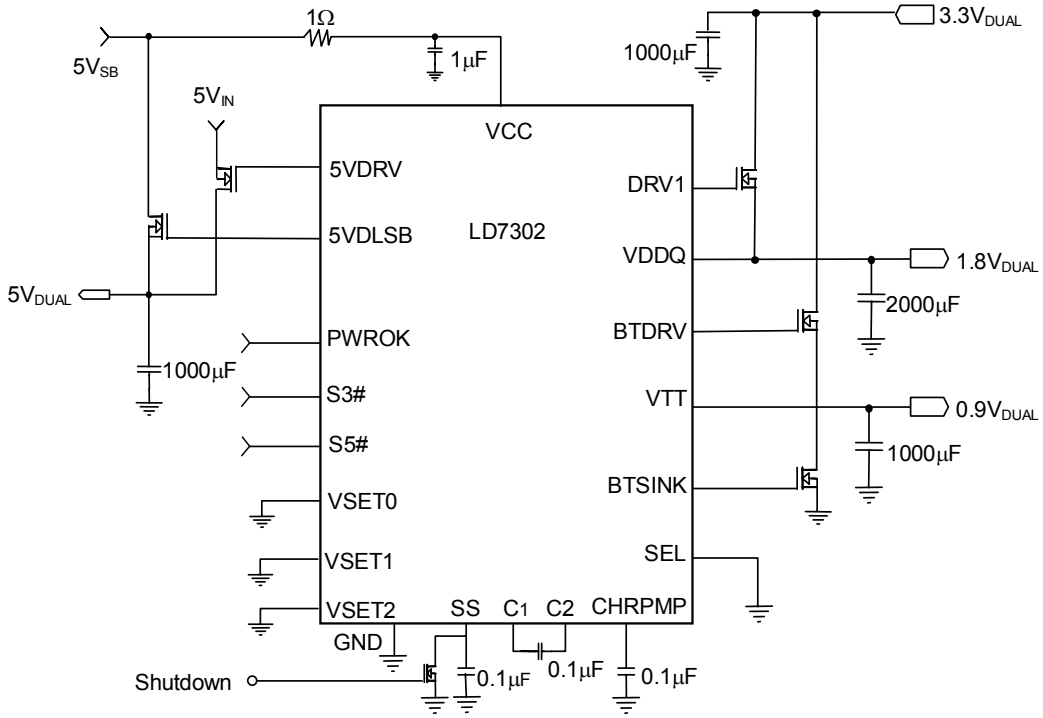


Fig.3 The Application Circuit for Mode A of the LD7302

Note: LD7302 is for 3.3V Logic System

Mode A	SEL	VSET0	VSET1	VSET2	VDDQ	VTT
DDRI	3.3V	0V	0V	0V	$2.5V_{DUAL}$	$1.25V_{DUAL}$
	3.3V	0V	0V	3.3V	$2.6V_{DUAL}$	$1.30V_{DUAL}$
	3.3V	0V	3.3V	0V	$2.7V_{DUAL}$	$1.35V_{DUAL}$
	3.3V	0V	3.3V	3.3V	$2.8V_{DUAL}$	$1.40V_{DUAL}$
	3.3V	3.3V	0V	0V	$2.9V_{DUAL}$	$1.45V_{DUAL}$
	3.3V	3.3V	0V	3.3V	$3.0V_{DUAL}$	$1.50V_{DUAL}$
	3.3V	3.3V	3.3V	0V	$3.1V_{DUAL}$	$1.55V_{DUAL}$
	3.3V	3.3V	3.3V	3.3V	$3.2V_{DUAL}$	$1.60V_{DUAL}$

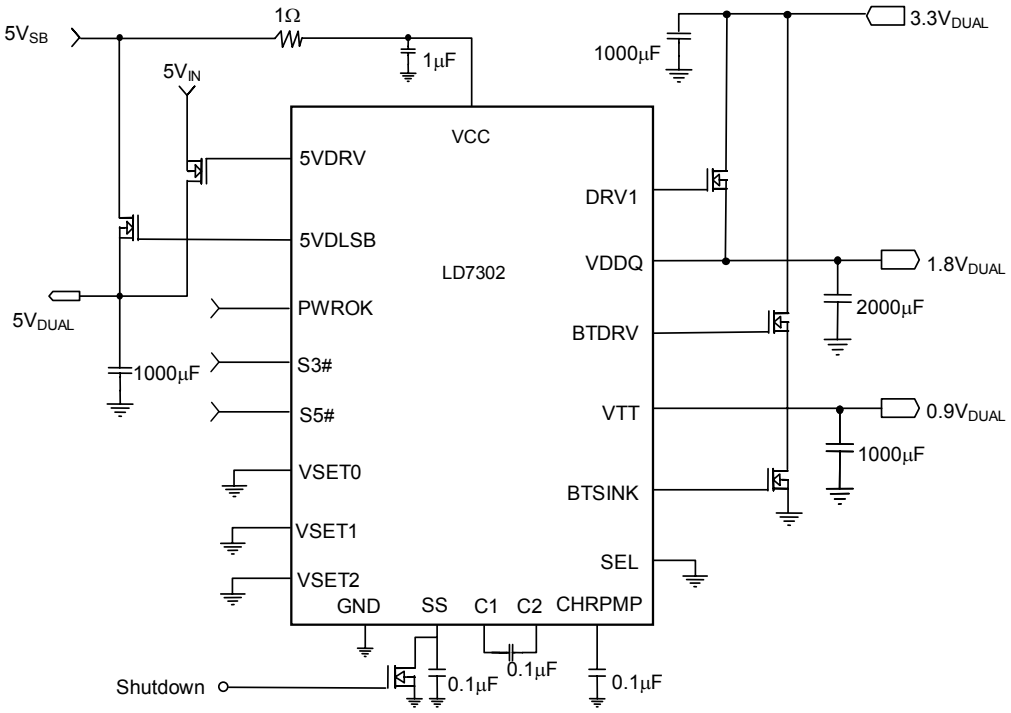


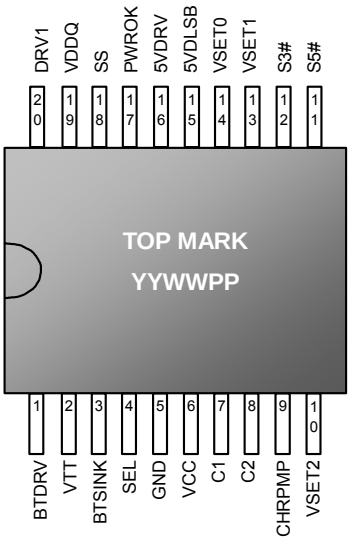
Fig.4 The Application Circuit for Mode B of LD7302

Note: LD7302 is for 3.3V logic system

Mode B	SEL	VSET0	VSET1	VSET2	VDDQ	VTT
DDRII	0V	0V	0V	0V	$1.8V_{DUAL}$	$0.90V_{DUAL}$
	0V	0V	0V	3.3V	$1.9V_{DUAL}$	$0.95V_{DUAL}$
	0V	0V	3.3V	0V	$2.0V_{DUAL}$	$1.00V_{DUAL}$
	0V	0V	3.3V	3.3V	$2.1V_{DUAL}$	$1.05V_{DUAL}$
	0V	3.3V	0V	0V	$2.2V_{DUAL}$	$1.10V_{DUAL}$
	0V	3.3V	0V	3.3V	$2.3V_{DUAL}$	$1.15V_{DUAL}$
	0V	3.3V	3.3V	0V	$2.4V_{DUAL}$	$1.20V_{DUAL}$
	0V	3.3V	3.3V	3.3V	$2.5V_{DUAL}$	$1.25V_{DUAL}$

Pin Configuration

SSOP-20 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

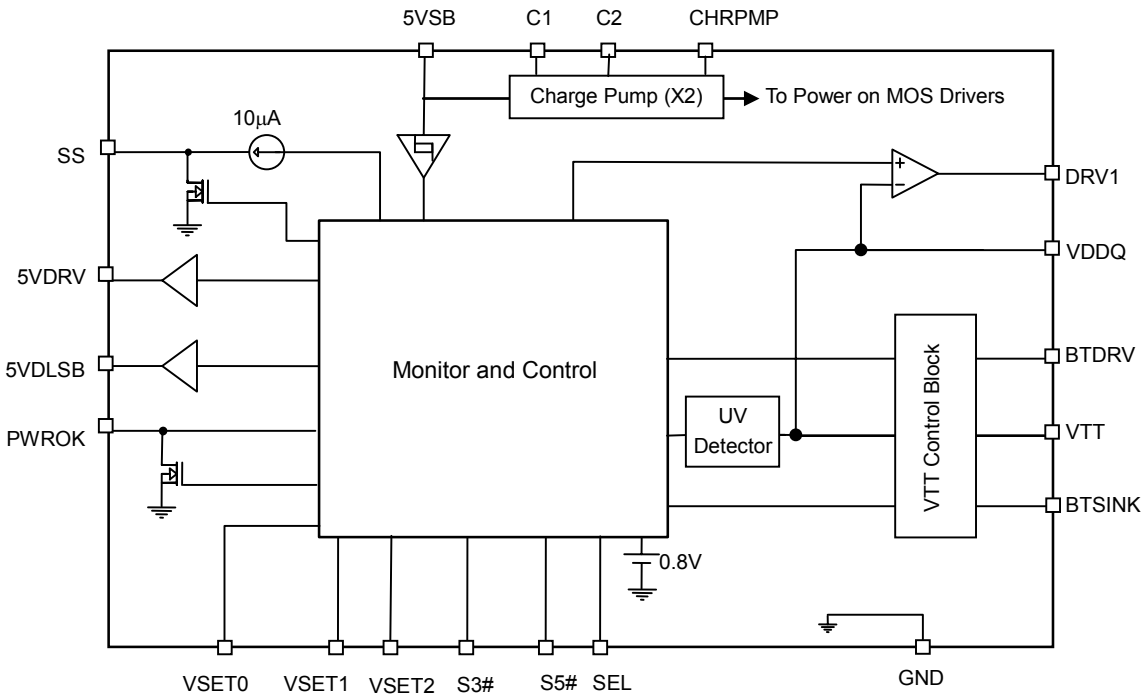
Part number	Package	Top Mark	Shipping
LD7301 PG	**SSOP-20 (PB FREE)**	LD7301PG	2000 /tape & reel
LD7302 PG		LD7302PG	2000 /tape & reel

Pin Descriptions

PIN	NAME	FUNCTION
1	BTDRV	BT Current Source. Connect this pin to the gate of a suitable NMOS for driving bus termination regulator output.
2	VTT	BT controller feedback input. Connect this pin to the bus termination regulator output.
3	BTSINK	BT Current Sink. This pin is used to drive a NMOS to sink the redundant current in the high-speed bus.
4	SEL	Mode selection pin. LD7301 will select to work in Mode A while SEL=5.0V, and Mode B while SEL=0V. LD7302 will select to work in Mode A while SEL=3.3V, and Mode B while SEL=0V.
5	GND	Signal GND. All voltage levels are measured with respect to this pin.
6	VCC	1uF with X5R type ceramic capacitor is recommended for the bypass capacitor of 5VSB pin. The voltage at this pin is monitored for power-on reset (POR) purposes.

PIN	NAME	FUNCTION
7	C1	Charge Pump Capacitor. Connect a flying capacitor between this pin and C2 to generate internally- used high voltage from 5VSB power supply
8	C2	Charge Pump Capacitor. Connect a flying capacitor between this pin and C1 to generate internally- used high voltage from 5VSB power supply
9	CHRPMP	Charge Pump Output. This pin provides double 5VSB supply voltage by charge pumping. Bypass with a 0.1μF (voltage rating >10V) capacitor.
10	VSET2	Combine with VSET0 and VSET1 to select output voltages of VDDQ and VTT.
11	S5#	This pin and S3# switch the IC's operating state from active (S0, S1/S2) to sleep states (S3, S4/S5). Connect this pin to the computer system's SLP_S5 # signal. Internal pull low resistor is 100K.
12	S3#	This pin and S5# switch the IC's operating state from active (S0, S1/S2) to sleep states (S3, S4/S5). Connect this pin to the computer system's SLP_S3 # signal.
13	VSET1	Combine with VSET0 and VSET2 to select output voltages of VDDQ and VTT.
14	VSET0	Combine with VSET1 and VSET2 to select output voltages of VDDQ and VTT.
15	5VDLSB	Connect this pin to the gate of a suitable NMOS. The transistor is switched on, connecting the 5VSB output to the 5VDL regulator output during sleep states (S3, S4/S5).
16	5VDRV	Connect this pin to the gate of a suitable NMOS. The transistor is switched on, connecting the 5Vin output to the 5VDL regulator output in active states (S0, S1/S2).
17	PWROK	This pin provides a bi-directional signal to ensure the system work normally. When the system transfers from state G3, S3 or S5 (PWROK=0), to state S0, the LD7301/02 will detect the PWROK signal to ensure that the external system power is OK and then switch each outputs into state S0.
18	SS	Connect this pin to a small ceramic capacitor (100nF recommend). The internal soft start (SS) current source along with the external capacitor creates a voltage ramp to control the ramp-up of the output voltages.
19	VDDQ	VDDQ controller feedback input. Connect this pin to the VDDQ regulator output.
20	DRV1	VDDQ Driver. Connect this pin to the gate of a suitable NMOS for driving VDDQ output.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3~6.0V
CHRPMP, 5VDRV, 5VDLSB, DRV1, BTDRV and C2 Pin	-0.3~12.0V
Operating Temperature Range	-30°C to 85°C
Storage Temperature Range	-55°C to 125°C
Junction Temperature	125°C
Lead Temperature (Soldering, 10sec)(LD7301/02PL)	260 °C
ESD Level (Human Body Model)	2KV

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=5V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Vcc Supply Current					
Nominal Supply Current			6		mA
Shutdown Supply Current	Vss=0V, S3#=0, S5#=0		2		mA
POWER ON RESET					
Rising 5VSB POR Threshold	V_{CHRPMP} >8V	3.9	4.15	4.4	V
5VSB Hysteresis			0.5		V
Rising V_{CHRPMP} POR Threshold	5VSB >4.3V	6.9	7.3	7.7	V
V_{CHRPMP} Hysteresis			1.0		V
VDDQ Linear Regulator Mode A (LD7301)					
VDDQ Voltage	SEL=5.0V, V_{SET0}=0V, V_{SET1}=0V, V_{SET2}=0V		2.6		V
VDDQ Voltage	SEL=5.0V,V_{SET0}=5V, V_{SET1}=5V, V_{SET2}=0V		3.1		V
VDDQ Voltage Tolerance		-1.5		+1	%
Under Voltage Falling Threshold			80		%
VDDQ Linear Regulator Mode A (LD7302)					
VDDQ Voltage	SEL=3.3V, V_{SET0}=0V, V_{SET1}=0V, V_{SET2}=3.3V		2.6		V
VDDQ Voltage	SEL=3.3V, V_{SET0}=3.3V, V_{SET1}=3.3V, V_{SET2}=3.3V		3.2		V
VDDQ Voltage Tolerance		-1.5		+1	%
Under Voltage Falling Threshold			80		%
VDDQ Linear Regulator Mode B (LD7301)					
VDDQ Voltage	SEL=0V, V_{SET0}=0V, V_{SET1}=0V, V_{SET2}=0V		1.8		V
VDDQ Voltage	SEL=0V, V_{SET0}=5V, V_{SET1}=5V, V_{SET2}=0V		2.3		V
VDDQ Voltage Tolerance		-1.5		+1	%
Under Voltage Falling Threshold			80		%

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VDDQ Linear Regulator Mode B (LD7302)					
VDDQ Voltage	SEL=0V, V_{SET0}=0V, V_{SET1}=0V, V_{SET2}=0V		1.8		V
VDDQ Voltage	SEL=0V, V_{SET0}=3.3V, V_{SET1}=3.3V, V_{SET2}=3.3V		2.5		V
VDDQ Voltage Tolerance		-1.5		+1	%
Under Voltage Falling Threshold			80		%
BUS TERMINATOR					
VTT Output Voltage/ VDDQ	Compare to actual VDDQ	49.25	50	50.75	%
Under Voltage Falling Threshold			80		%
5VDL SWITCH driver capacity					
5VDRV Source Current	C_L=3nF		7		mA
5VDRV Sink Current	C_L=3nF		-0.7		mA
5VDLSB Source Current	C_L=3nF		7		mA
5VDLSB Sink Current	C_L=3nF		-0.7		mA
DRV1, BTDRV, BTSINK Output					
Source Current			7		mA
Sink Current			-7		mA
Control I/O S3#, S5#, SEL and PWROK					
S3#, S5#, SEL and PWROK	High level Threshold	2.6			V
	Low level Threshold			0.8	V
VSET1 (LD7301)					
VSET1	High level Threshold	3.6			V
	2.5V level Threshold	1.8		3.2	V
	Low level Threshold			1.4	V
VSET0 and VSET2 (LD7301)					
VSET0 and VSET2	High level Threshold	2.6			V
	Low level Threshold			0.8	V
VSET0, VSET1 and VSET2 (LD7302)					
VSET0, VSET1 and VSET2	High level Threshold	2.6			V
	Low level Threshold			0.8	V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Soft Start					
Soft Start Current			6.5		μA
Vss upper limit			4.0		V
Soft Start Shutdown Voltage Threshold				0.5	V
Charge Pump					
Charge pump switching frequency			250		KHz
Others					
PWROK pin output impedance			150		Ω

Function Description

Initialization

The LD7301/02 will initialize automatically upon receipt of input power. It continuously monitors the 5VSB input supply voltage with the function of Power ON Reset (POR). As soon as the 5VSB reaches up with the POR threshold, the LD7301/02 will initialize in the G3 state.

In the initial state, there's only 5Vdual produced. Then it will enter the state of S0, as S3#=1, S5#=1 and PWROK=1. The Fig. 5 shows the transition relationship of legal states.

The Facts of output operations

The operating mode (active or sleep outputs) are selectable through two digital control pins, S3 # and S5#.

The truth combinations pertaining to all outputs for mode A are described in Table 1 and mode B in Table 2. It's prohibited to allow the transition from the state of S5 to S3 due to the limit of the internal circuitry. (The LD7301/02 will ignore the input signals from S3# and S5# and remain at the state of S5).

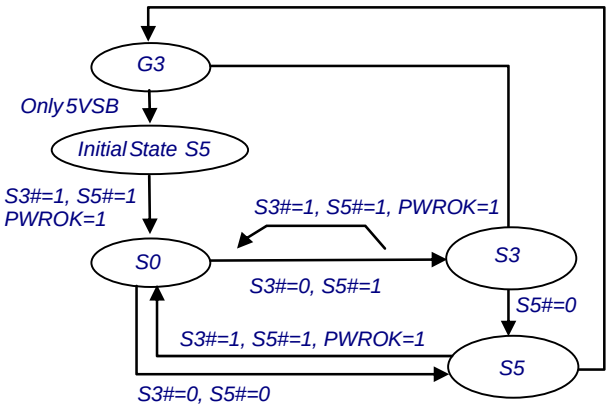


Fig.5 The transition relationship of legal states

Table 1-- Mode A:

S5#	S3#	5VDLSB	5VDRV	5VDL	VDDQ	BT	UVP	Remark
1	1	0V	10V	5V	2.5V	1.25V	ON	S0
1	0	10V	0V	5V	2.5V	1.25V	ON	S3
0	0	10V	0V	5V	0V	0V	OFF	S5

Table 2--Mode B:

S5#	S3#	5VDLSB	5VDRV	5VDL	VDDQ	BT	UVP	Remark
1	1	0V	10V	5V	1.8V	0.9V	ON	S0
1	0	10V	0V	5V	1.8V	0.9V	ON	S3
0	0	10V	0V	5V	0V	0V	OFF	S5

Soft Start Interval

The built-in soft-start circuitry allows precise control for the slew-up speed of the output voltages, which will enable the power-ups free from supply drop-off. Since the outputs will ramp up in a linear fashion, the current dedicated to charging the output capacitors can be figured out by the following formula:

$$I_{COUT} \approx \frac{I_{SS}}{C_{SS} \times 1.6} \times \Sigma(C_{OUT} \times I_{OUT}), \text{ where}$$

Iss- soft start current (typical 10μA)

Css- Soft start capacitor

$\Sigma(C_{OUT} \times I_{OUT})$ - the sum of the product between the capacitance and the voltage of an output

Due to the various timing events of the system, it is recommended that the soft start interval should not exceed 30mS.

Fault Protection

All the outputs are monitored against undervoltage events. A severe overcurrent caused by a failure load on any of the outputs, in turn, would cause the specific output will drop suddenly. If VDDQ or BT output voltages drops below 80% (typical) of their set value, it will shut off VDDQ and BT outputs, pull the PWROK pin low and latch off the entire circuit. Note that the UVP event only shuts off VDDQ and BT outputs and will not change the state of 5VDRV and 5VLSB. The latch-off condition can be reset by cycling the bias power (5VSB). The Under-voltage sensing is disabled during all disabled outputs, the interval of soft- start ramp up and before PWROK=1.

Shutdown

Whenever a fatal occurs to damage a computer system, it could shutdown the LD7301/02 by pulling the SS pin below 0.5V with an open drain device capable of sinking a minimum of 2mA. Through this, it will effectively shut down all the pass elements (including 5VDRV and 5VLSB), pull the PWROK pin low and latch off the entire circuit. Upon releasing of the SS pin and cycling the bias power (5VSB), the LD7301/02 will undergo a new soft start cycle and resume normal operation in accordance to the ATX supply and the status of control pins.

Layout Consideration

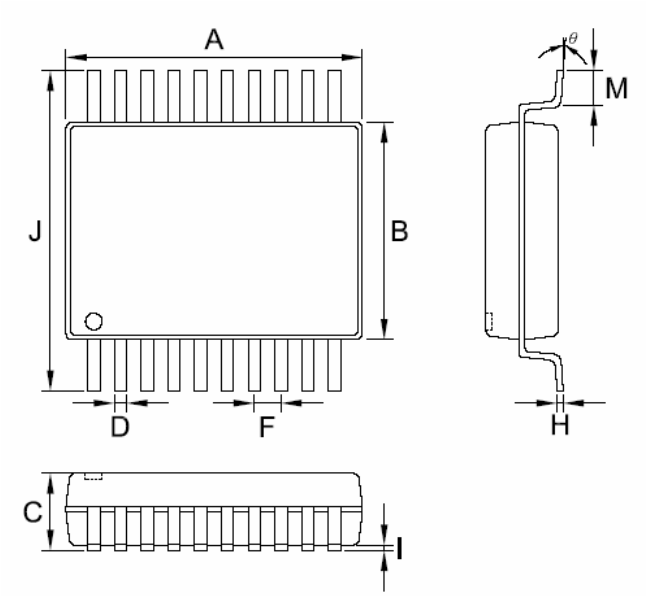
The typical application employing the LD7301/02 is a fairly straight-forward implementation. It resembles the use of the regular linear regulators. Some attention has to be paid to the layout with the few potentially sensitive nodes or those supplying critical bypass current.

Below are the guidelines for the PCB layout while using the LD7301/02.

1. The control IC should be placed in a central position on the motherboard, closer to the memory load.
2. Please keep the bypass capacitor 1μF of 5VSB pin very close to the IC (<5mm) to well decouple the input noise.
3. The pass transistors should be placed on pads capable of heat-sinking, matching with the device's power dissipation.
4. Locate all small signal components close to the respective pins of the IC, and connect them to ground, if applicable, placed a via close to the ground pad.
5. If possible, a multi-layer PCB is recommended.

Package Information

SSOP-20



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	6.900	7.500	0.272	0.295
B	5.000	5.600	0.197	0.220
C	1.650	2.000	0.065	0.079
D	0.220	0.380	0.009	0.015
F	0.650 TYP.		0.026 TYP.	
H	0.150 TYP.		0.006TYP.	
I	0.050	0.210	0.002	0.008
J	7.400	8.200	0.291	0.323
M	0.550	0.950	0.022	0.037
θ	0°	8°	0°	8°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	4/13/06	Original Specification.