Leadtrend 通嘉科技

LD7522H

1/9/2009

Smart Green-Mode PWM Controller with Multiple Latch-Mode Protections

Rev. 04

General Description

The LD7522H is a low startup current, current mode PWM controller with green-mode power-saving operation. The SOP-8/DIP-8 package integrated functions such as the leading- edge blanking of the current sensing, internal slope compensation, line compensation, and several protection features. The protection functions include cycle-by-cycle current limit, OVP, OTP, OLP, and brownout protection. It provides the users a high efficiency, low external component counts solution for AC/DC power applications.

Furthermore, to satisfy various protection requirements, both latch-mode protection and auto-recoverable protection can be easily achieved by configuring LD7522H on different operation modes.

The special green-mode control is not only to achieve the low power consumption but also to offer a non-audible-noise operation when the LD7522H is operating under light load or no load condition.

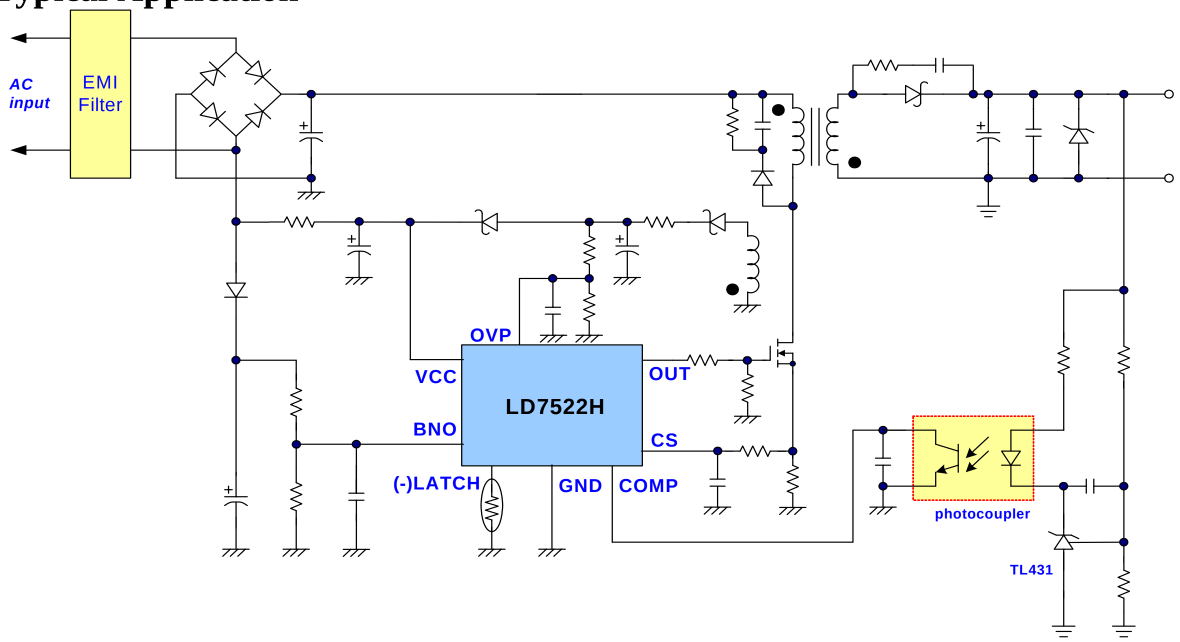
Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (< 35μA)
- Current Mode Control
- Non-audible-noise Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Slope Compensation
- OVP (Over Voltage Protection)
- OLP (Over Load Protection)
- OTP (Over Temperature Protection) through a NTC
- Brownout Protection
- Flexibility on Latch/Auto-Recoverable Protection Mode
- 500mA Driving Capability

Applications

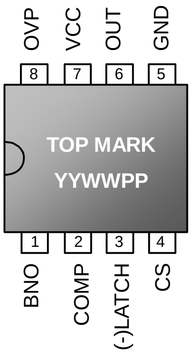
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

Typical Application



Pin Configuration

SOP-8 & DIP-8 (TOP VIEW)



YY: Year code (D: 2004, E: 2005…..)
WW: week code
PP: production code

Ordering Information

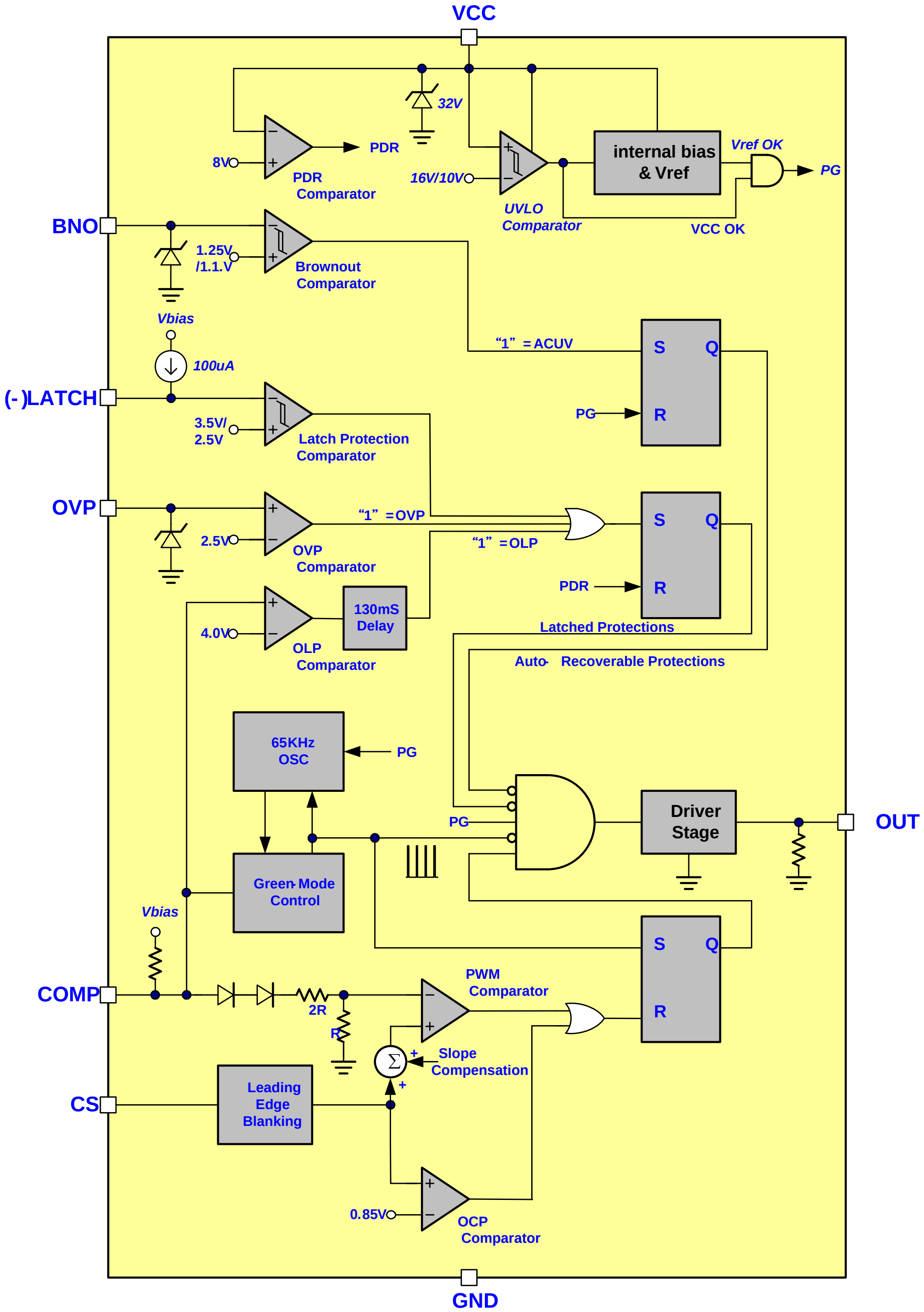
Part number	Package		Top Mark	Shipping
LD7522H GS	SOP-8	Green Package	LD7522HGS	2500 /tape & reel
LD7522H PS	SOP-8	PB Free	LD7522HPS	2500 /tape & reel
LD7522H PN	DIP-8	PB Free	LD7522HPN	3600 /tube /Carton

The LD7522H is ROHS compliant/ Green Package.

Pin Descriptions

PIN	NAME	FUNCTION
1	BNO	Brownout Protection Pin. Connected a resistor divider from this pin to bulk capacitor voltage to set the brownout level and line compensation. When the voltage of this pin is lower than threshold voltage, the PWM output will be off.
2	COMP	Voltage feedback pin (same as the COMP pin in UC384X), By connecting a photo-coupler to close the control loop and achieve the regulation.
3	(-) LATCH	Pull this pin to lower than 2.5V will shutdown the controller to the latch mode until the AC power-on recycling. By connecting a NTC from this pin to ground will achieve the OTP protection function. Keep this pin as floating to disable the latch protection.
4	CS	Current sense pin, connect to sense the MOSFET current
5	GND	Ground
6	OUT	Gate drive output to drive the external MOSFET
7	VCC	Supply voltage pin
8	OVP	This pin is high-active to provide the OVP function. By the connecting a zener or a resistor voltage divider to Vcc will set the OVP level. Whenever the voltage is higher than 2.5V, the OVP is tripped and the gate drive will be off. Short this pin to ground to disable the OVP function.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	30V
COMP, CS, (-) LATCH	-0.3 ~7V
OVP, BNO	-0.3 ~7V
Sinking Current Capability of OVP pin (V_{OVP}=5V)	200μA
Sinking Current Capability of BNO pin (V_{BNO}=5V)	200μA
Junction Temperature	150°C
Operating Ambient Temperature	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8)	160°C/W
Package Thermal Resistance (DIP-8)	100°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	400mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	3KV
ESD Voltage Protection, Machine Model	200V
Gate Output Current	500mA

Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)					
Startup Current			20	35	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		3.5	5.0	mA
	V_{COMP}=3V		3.0		mA
	Protection Mode (note 1)		0.7		mA
UVLO (off)		9.0	10.0	11.0	V
UVLO (on)		15.0	16.0	17.0	V
Voltage Feedback (Comp Pin)					
Short Circuit Current	V_{COMP}=0V		2.5	4.0	mA
Green Mode Threshold VCOMP			2.6		V
Current Sensing (CS Pin)					
Maximum Input Voltage, $V_{CS(OFF)}$		0.800	0.850	0.900	V
Leading Edge Blanking Time			350		nS
Input impedance		1			MΩ
Delay to Output			150		nS
Gate Drive Output (OUT Pin)					
Output Low Level	V_{CC}=15V, Io=20mA			1.0	V
Output High Level	V_{CC}=15V, Io=20mA	9.0			V
Rising Time	Load Capacitance=1000pF		50	160	nS
Falling Time	Load Capacitance=1000pF		30	60	nS
Oscillator					
Frequency		60	65	70	KHz
Green Mode Frequency			20		KHz
Frequency Temp. Stability	(-40°C~85°C)			3	%
Frequency Voltage Stability	(VCC=12V-30V)			1	%
Latch Protection (-)LATCH Pin)					
(-)LATCH Pin Source Current		92	100	108	μA
Turn-On Trip Level		3.30	3.50	3.70	V
Turn-Off Trip Level		2.40	2.50	2.60	V
(-)LATCH pin de-bounce time		100			μS
De-latch Vcc Level	(PDR, Power Down Reset)	6.8	8.0	8.7	V
Brownout Protection (BNO Pin)					
Brownout Turn-On Trip Level		1.20	1.25	1.30	V
Brownout Turn-Off Trip Level		1.05	1.10	1.15	V
BNO pin de-bounce time		100			μS
Zener Clamping Voltage on BNO Pin	I_{BNO}=1.5μA		5.0		V

Note 1: When OVP, OLP, or Latch Protection is tripped.

Electrical Characteristics (Continued)

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Over Voltage Protection (OVP Pin)					
OVP Trip Level		2.35	2.50	2.65	V
OVP De-bounce Time		100			μS
Zener Clamping Voltage on OVP pin	I_{OVP}=1.5μA		5.0		V
OLP (Over Load Protection)					
OLP Trip Level	$V_{COMP(OLP)}$		4.0		V
OLP Delay Time	V_{COMP}> $V_{COMP(OLP)}$		130		mS

Typical Performance Characteristics

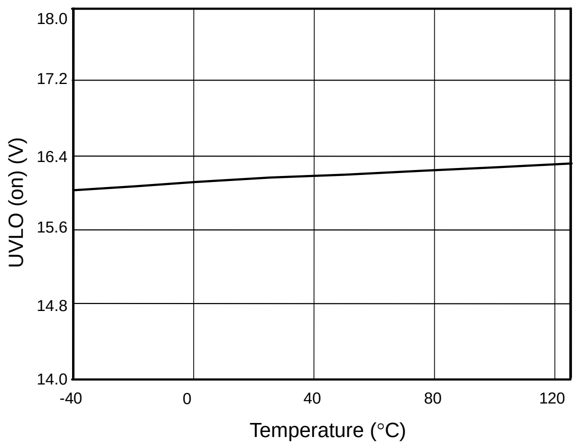


Fig. 1 UVLO (on) vs. Temperature

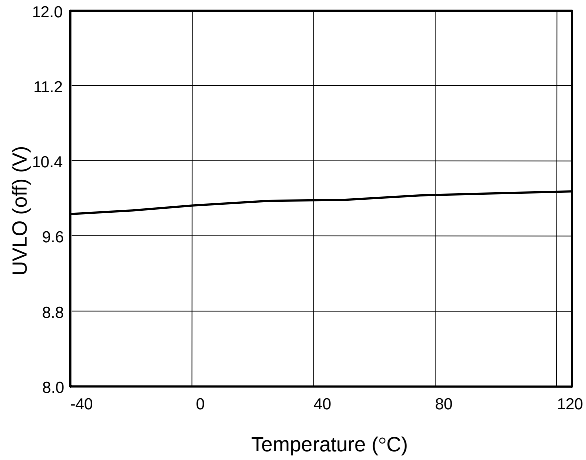


Fig. 2 UVLO (off) vs. Temperature

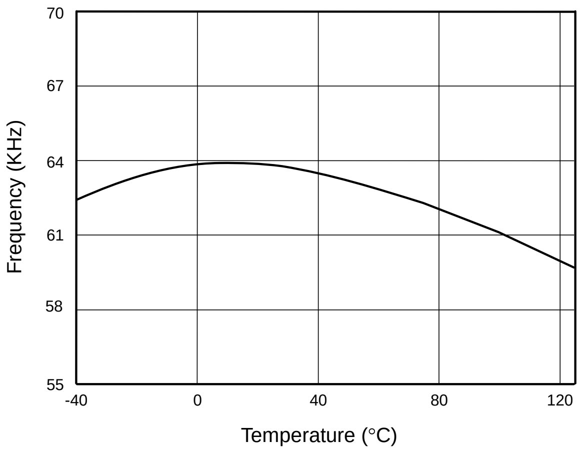


Fig. 3 Frequency vs. Temperature

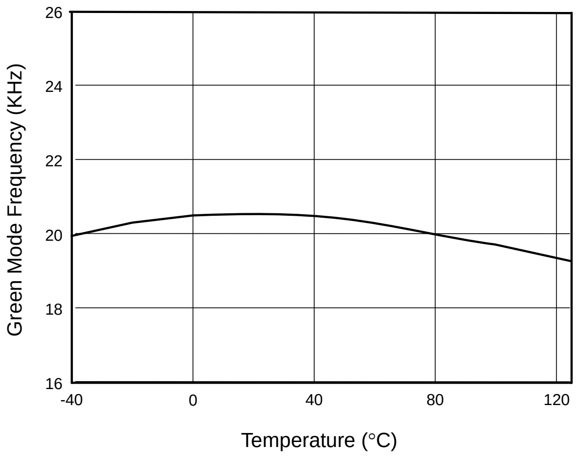


Fig. 4 Green Mode Frequency vs. Temperature

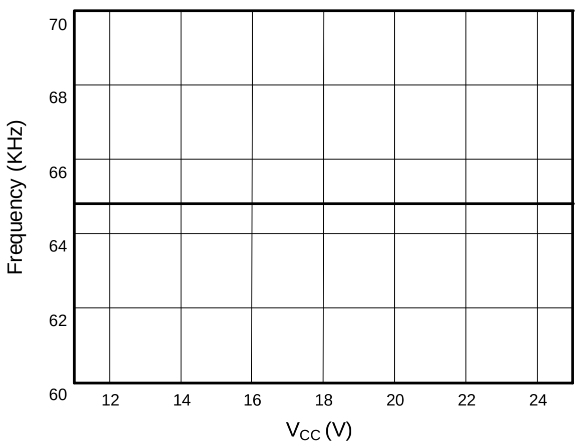


Fig. 5 Frequency vs. V_{CC}

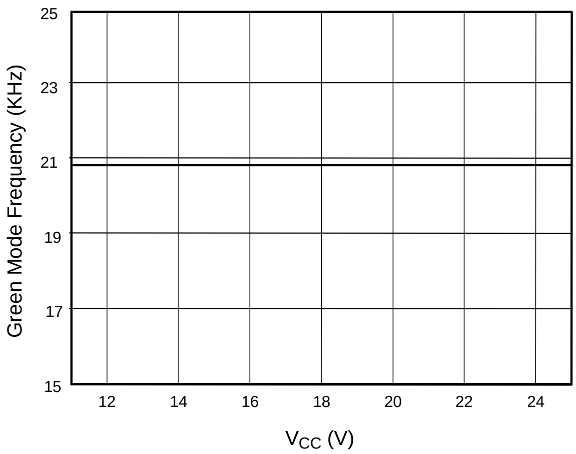


Fig. 6 Green Mode Frequency vs. V_{CC}

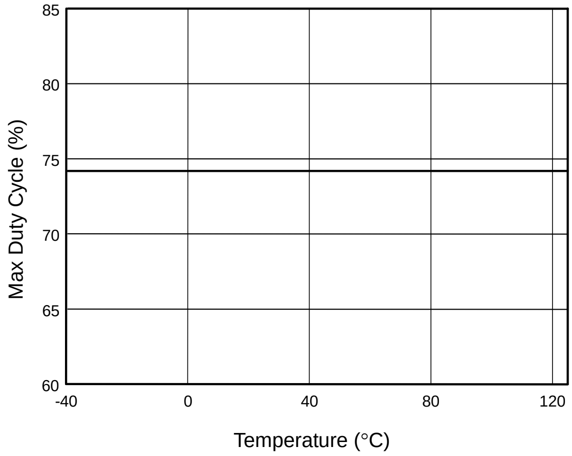


Fig. 7 Max Duty Cycle vs. Temperature

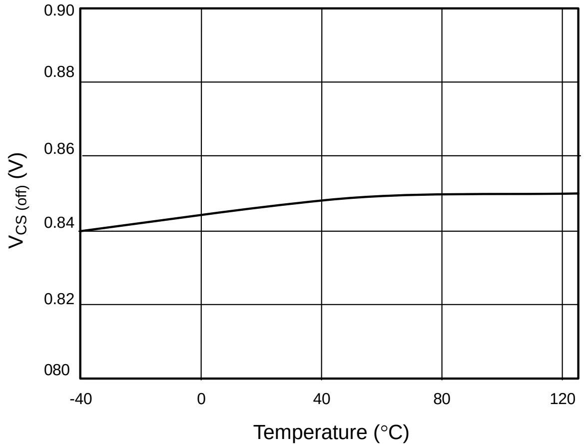


Fig. 8 Vcs (off) vs. Temperature

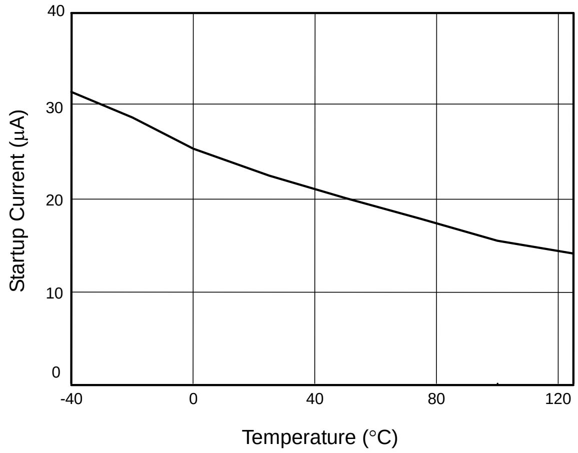


Fig. 9 Startup Current vs. Temperature

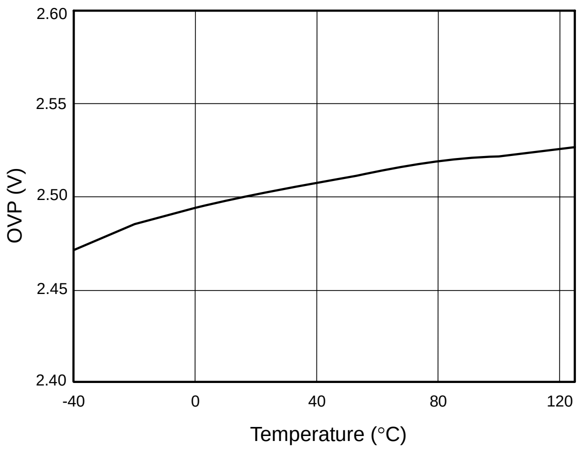


Fig. 10 OVP-Trip Level vs. Temperature

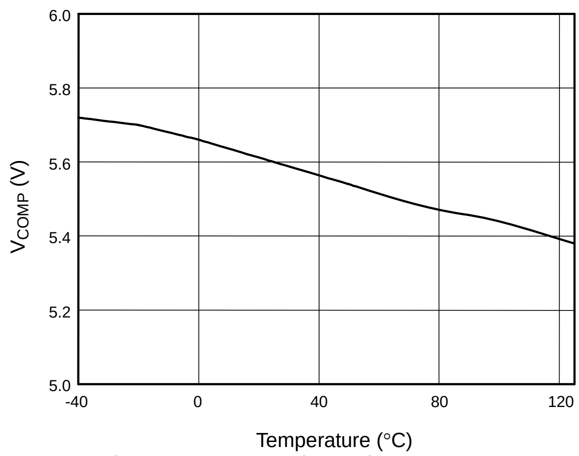


Fig. 11 V_{COMP} open-loop voltage vs. Temperature

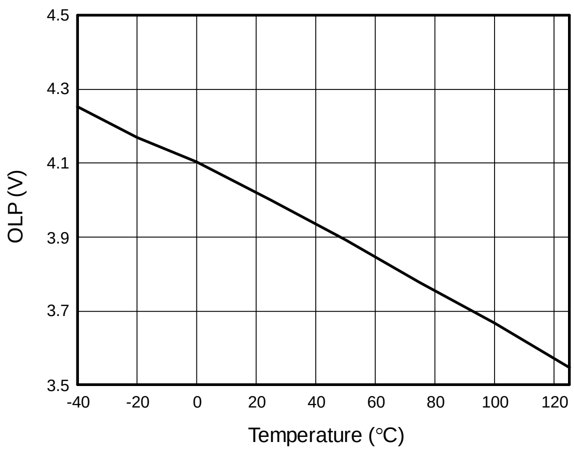


Fig. 12 OLP-Trip Level vs. Temperature

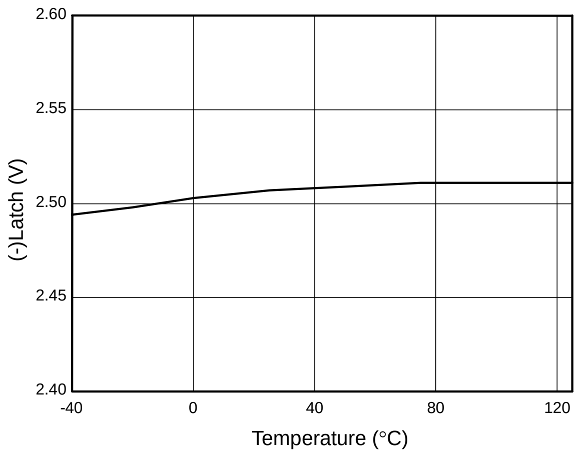


Fig. 13 (-)Latch Pin Off-Level vs. Temperature

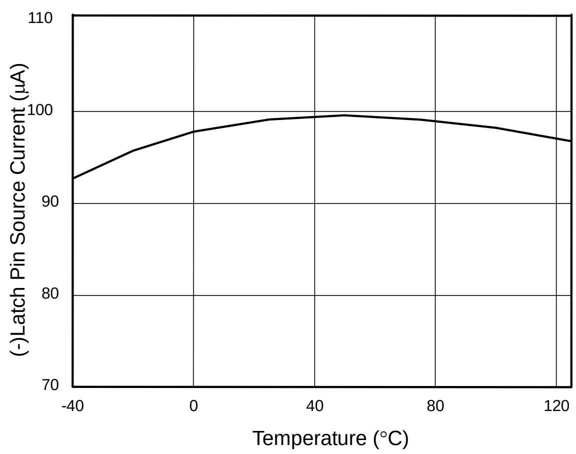


Fig. 14 (-)Latch Pin Source Current vs Temperature

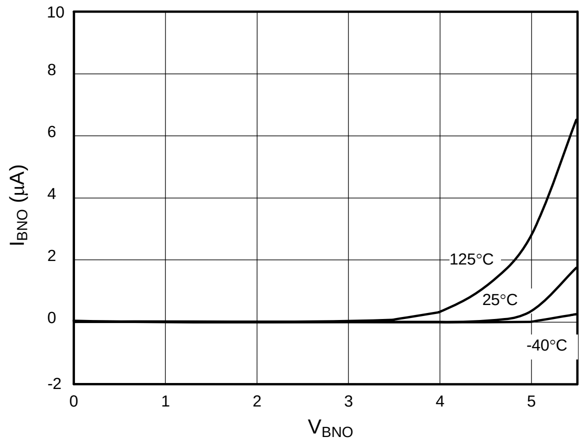


Fig. 15 V_{BNO} vs. I_{BNO}

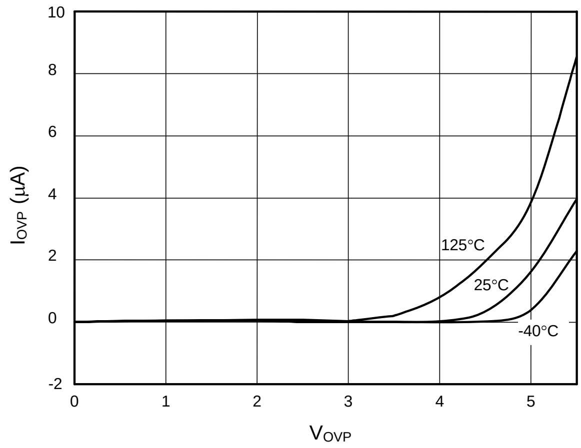


Fig. 16 V_{OVP} vs. I_{OVP}

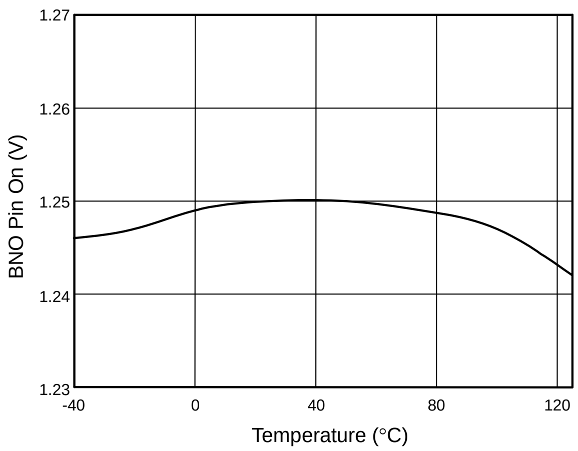


Fig. 17 BNO Pin On Level vs. Temperature

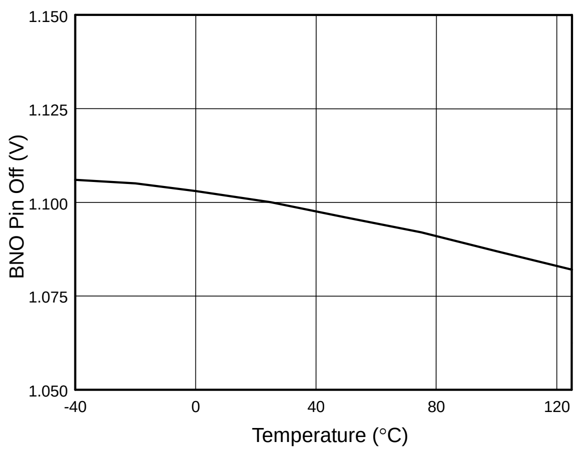


Fig. 18 BNO Pin Off Level vs. Temperature

Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adapters, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation force the PWM controllers need to be powerful to integrate more functions to reduce the external part counts. The LD7522H is targeted on such application to provide an easy and cost effective solution; its detail features are described as below:

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD7522H PWM controller and further to drive the power MOSFET. As shown in Fig. 19, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16V and 10.0V, respectively.

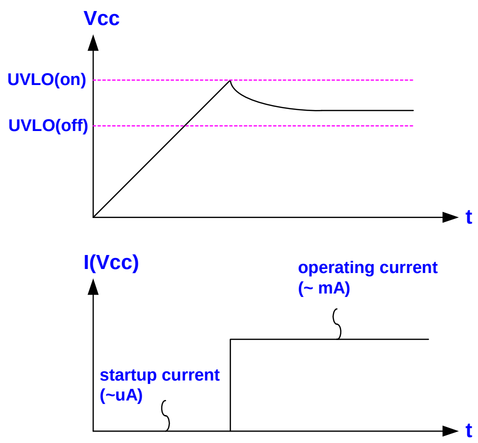


Fig. 19

Startup Current and Startup Circuit

The typical startup circuit to generate the LD7522H is shown in Fig. 20. During the startup transient, the Vcc is lower than the UVLO threshold thus there is no gate pulse produced from LD7522H to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the Vcc voltage is high enough to turn on the LD7522H and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD7522H is only 35μA.

If a higher resistance value of the R1 is chosen, it usually takes more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

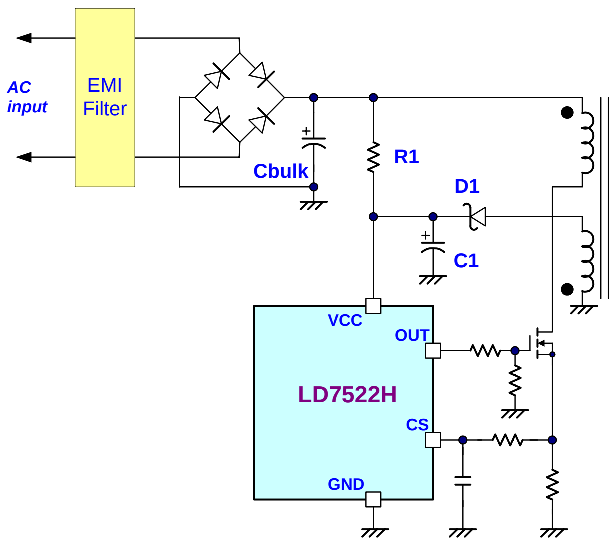


Fig. 20

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7522H is limited to 75% to avoid the transformer saturation.

Oscillator and Switching Frequency

The switching frequency of LD7522H is fixed as 65KHz internally to provide the optimized operations by considering the EMI performance, thermal treatment, component sizes and transformer design.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 in the secondary side through the photo-coupler to the COMP pin of LD7522H. The input stage of LD7522H, like the UC384X, is with 2 diodes voltage offset then feeding into the voltage divider with 1/3 ratio, that is,

$$V_{+(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally thus can be eliminated on the external circuit.

Dual-Oscillator Green-Mode Operation

There are many different topologies has been implemented in different chips for the green-mode or power saving requirements such as "burst-mode control", "skipping-cycle mode", "variable off-time control "…etc. The basic operation theory of all these approaches intended to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reduce the switching frequency.

By using this dual-oscillator control, the green-mode frequency can be well controlled and further to avoid the generation of audible noise.

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is operated more than 50%. To stabilize the control loop, the slope compensation is needed in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. In LD7522H, the internal slope compensation circuit has been implemented to simplify the external circuit design.

Current Sensing, Leading-Edge Blanking

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD7522H detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set as 0.85V. Thus the MOSFET peak current can be calculated as:

$$I_{Peak(Max.)} = \frac{(0.85)}{R_S}$$

A 350nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. However, the total pulse width of the turn-on spike is decided by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in Figure 21) to avoid the CS pin being damaged by the negative turn-on spike.

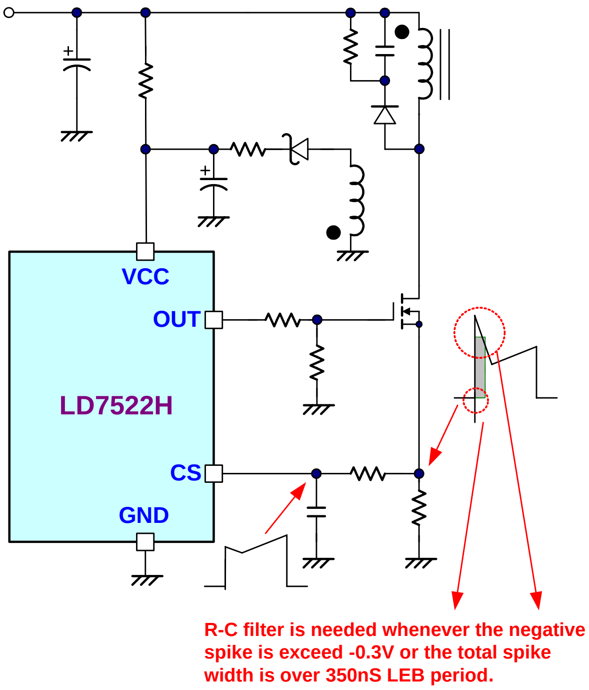


Fig. 21

Soft Start

An internal soft start circuit is implemented in LD7522H to reduce the large component stress during startup. The soft start period is 7.5mS.

Brownout Protection

The major function of BNO pin is to set the brownout protection point. Since the voltage on the BNO pin is proportional to the bulk capacitor voltage thus represented the line voltage. A brownout comparator is implemented to detect the abnormal line condition then shutdown the controller to prevent the damage. Figure 22 shows the operation. When V_{BNO} is lower than 1.25V, the gate output will be kept off even the Vcc already achieves UVLO(on), therefore the Vcc will be hiccup between UVLO(on) and UVLO(off). Until the line voltage is higher enough so that

V_{BNO} is higher than 1.25V, the gate output will start switching when the next UVLO(on) is tripped. A hysteresis is implemented to prevent the false trigger during turn-on and turn-off.

In order to protect BNO pin from being damaged during the dividing resistors floating, an internal zener diode is implemented in BNO pin. Fig. 15 shows the sinking capability of the zener diode. To protect BNO pin, the current flowing in BNO pin must be below 1.5μA, as shown in Fig. 15.

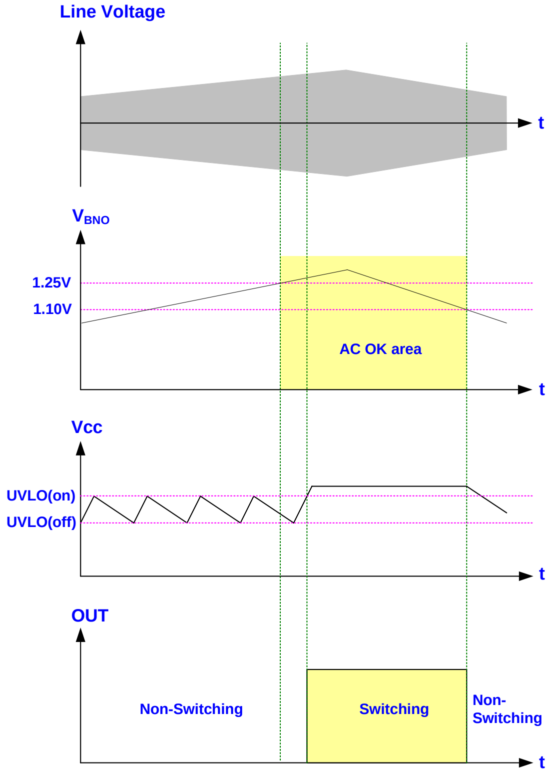


Fig. 22

Over Load Protection (OLP)---Latched Mode

To protect the circuit from the damage during over load condition or short condition, a smart OLP function is implemented in the LD7522H. Under such fault condition, the feedback system will force the voltage loop toward the saturation and thus pull the voltage on COMP pin (VCOMP) to high. Whenever the VCOMP trips the OLP threshold 4.0V and stays longer than 130mS, the protection is activated and then latch off the gate output to stop the switching of power circuit. The 130mS delay time is to prevent the false trigger from the power-on, turn-off transient and peak load condition. Whenever the over load condition is removed, it is necessary to start another AC power-on recycling to get the output back.

Over Voltage Protection (OVP)---Latch Mode

The V_{GS} ratings of the nowadays power MOSFETs are most with maximum 30V. To prevent the component damage from the fault condition, LD7522H is implemented the protection through the OVP pin. Figure 23 and Figure 24 show 2 different configurations to programming the OVP setting point --- zener detection and voltage divider. Figure 23 provided zero bias current under normal operation so that it will not affect the startup timing. But the tolerance of OVP trip point will be higher due to the distribution of the breakdown voltage of zener diode.

On the other hand, the circuit of Figure 24 will get the benefits on the cost and OVP accuracy but the value of R1 and R2 must be very high to avoid affecting the startup timing by the load effect.

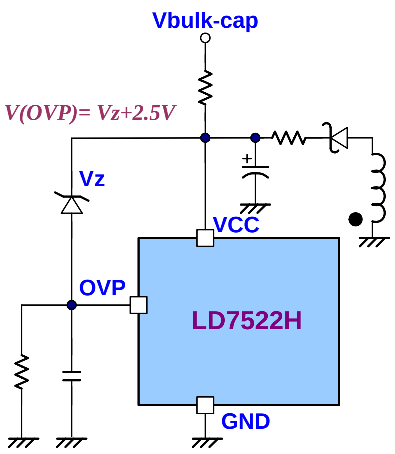


Fig. 23

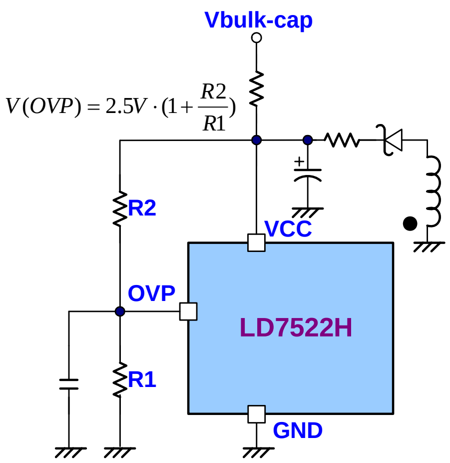


Fig. 24

As similar behavior like OLP, whenever the voltage on the OVP pin is higher than the threshold voltage 2.5V, the output gate drive circuit will be shutdown simultaneous thus to latch off the switching of the power MOSFET. Whenever

the voltage on the OVP pin gets back to lower than 2.5V and start another AC recycling again, then it can be recovery to normal condition.

(-)LATCH Pin and Over Temperature Protection (OTP) --- Latched Mode Protection

Under some abnormal conditions, the ambient temperature may be increased significantly and causes some damage on the components or further inhibits the dangerous. To prevent the power circuit damage from the system abnormal, the OTP is required. The OTP circuit is implemented by sensing the hot-spot of power circuit like power MOSFET or output rectifier. It can be easily achieved by connect a NTC on the (-)LATCH pin of LD7522H. When the device temperature or ambient temperature rises high, the resistance of NTC will be decreased so that the voltage on the (-)LATCH pin will be

$$V_{(-)Latch} = 100\mu A \cdot R_{NTC}$$

When the $V_{(-)LATCH}$ is lower than the threshold voltage (typical 2.5V), LD7522H will shutdown the gate output and then latch-off the power supply. On LD7522H, the controller will be kept latched until the Vcc drop lower than 8V (power down reset) and the fault condition is removed. That means the gate output is still off even the abnormal condition is released. The only way to successfully re-start the circuit needs to meet 2 conditions. One is to cool down the circuit thus NTC resistance is increased then $V_{(-)LATCH}$ is higher than 3.5V. Another condition is to remove the AC power cord and begin another AC power-on recycling. The detail operation is depicted as Figure 25.

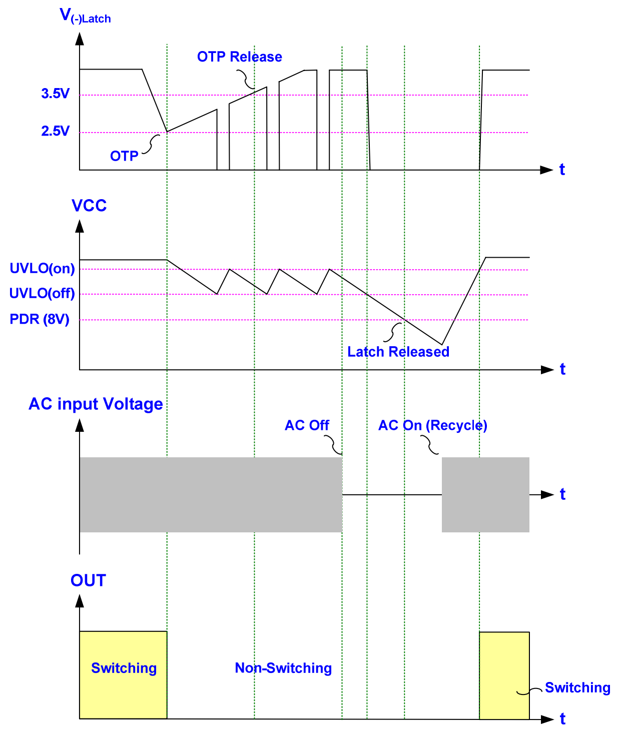
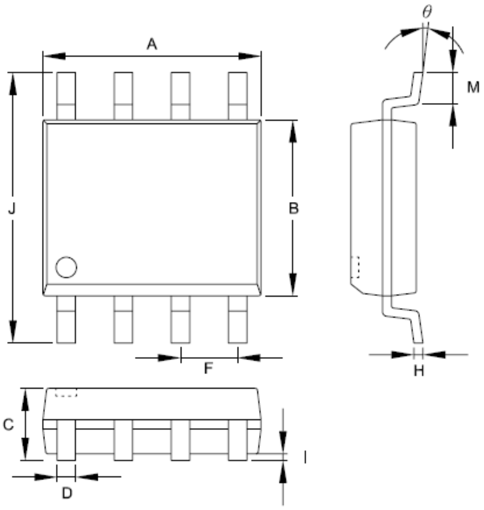

V(-)Latch
OTP Release
3.5V
2.5V
OTP
t
VCC
UVLO(on)
UVLO(off)
PDR (8V)
Latch Released
t
AC input Voltage
AC Off
AC On (Recycle)
t
OUT
Switching
Non-Switching
Switching
t

Fig.25

Package Information

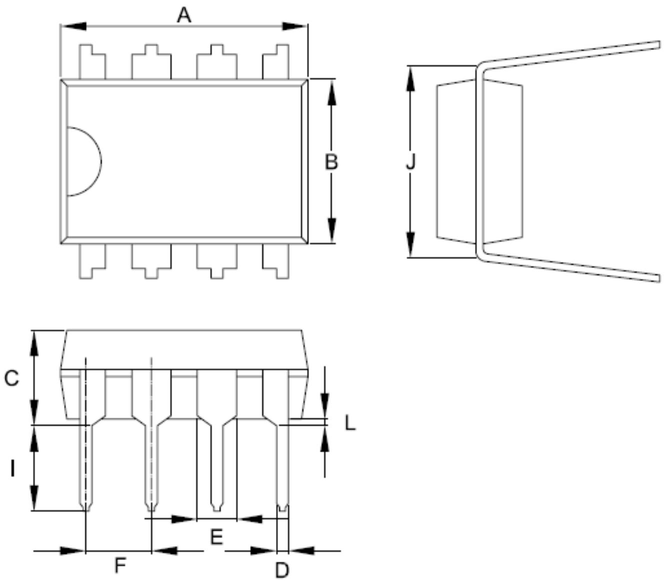
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	12/22/2006	Original Specification.
01	4/4/2007	Block Diagram update
02	6/24/08	OLP Delay Time
02a	7/11/2008	OLP- Latch mode/ …. threshold 4.0V and stays longer than 130mS,…
03	12/3/2008	Additional remark for BNO pin
04	12/18/2008	Leading Edge Blanking Time range