# Advanced Green-Mode PWM Controller with Frequency Triple for Peak Power

*Rev. 00*

## General Description

The LD7533 is an advanced Green Mode PWM controller, which is built-in with frequency triple, multi-protections and EMI-improved solution in a SOT-26/ DIP-8 package. It's ideal for applications requiring a cost-effective solution, and minimum component counts and circuit space, especially ideal for high power density and small size product.

The LD7533 is especially designed for switching power supply with peak power. It incorporates frequency triple function and adjustable OLP timer to handle the peak power with delay time. The frequency triple function can reduce the transformer flux and core size.

Furthermore, the frequency swapping function is to reduce the noise level and thus helps the power circuit designers for EMI suppression with minimum amount of component cost and developing time.

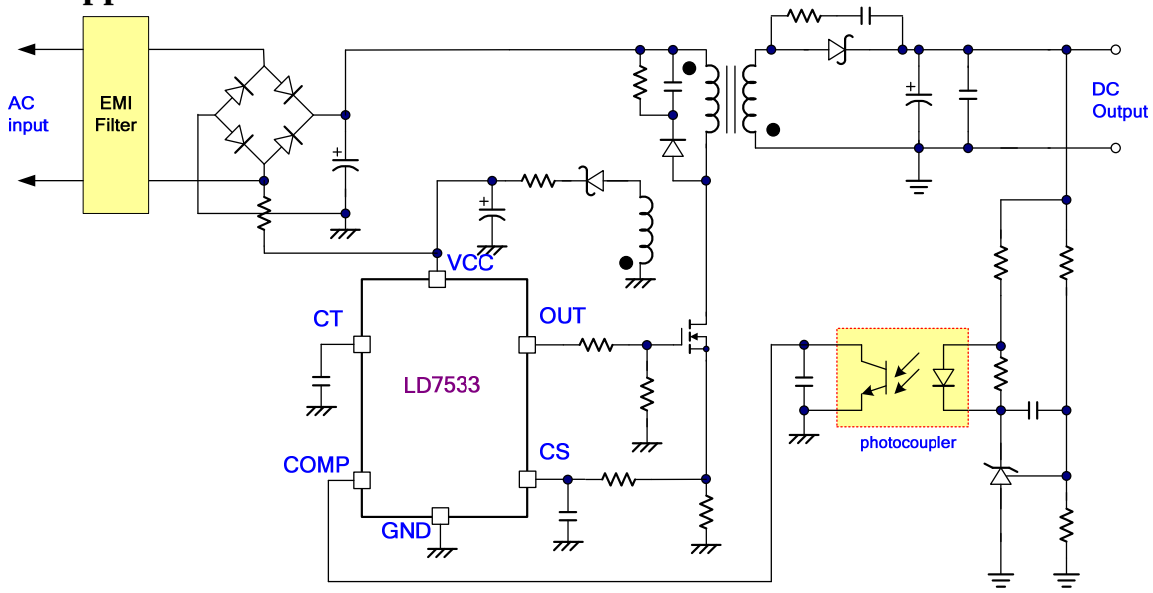
## Features

Frequency Triple for peak power (195kHz)
Very Low Startup Current (<18μA)
Ultra Low Operating Current at Light Load (<1mA)
Adjustable OLP (over load protection) delay timer
Adjustable Soft Start Time
Current Mode Control with Green Mode Operation
Out Pin Clamping
UVLO (Under Voltage Lockout)
LEB (Leading-Edge Blanking) on CS Pin
Internal Frequency Swapping for EMI improved
OVP (Over Voltage Protection) on VCC Pin
ON-Chip OTP (Over Temperature Protection)
300mA Driving Capability

## Applications

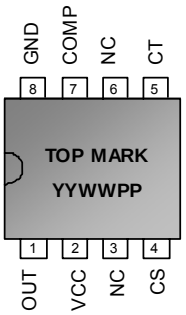
Switching Power Supply with Peak Power
Printer, Storage Power Supply

## Typical Application

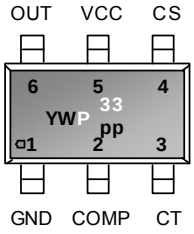


## Pin Configuration

DIP-8 (TOP VIEW)




SOT-26 (TOP VIEW)




YY, Y : Year code (D: 2004, E: 2005…..)
WW, W : Week code
pp : Production code
P33 : LD7533

## Ordering Information

| Part number | Package | | Top Mark | Shipping |
|---|---|---|---|---|
| LD7533 GL | SOT-26 | Green Package | YWP/33 | 3000 /tape & reel |
| LD7533 GN | DIP-8 | Green Package | LD7533 GN | 3600 /tube /Carton |

The LD7533 is ROHS compliant.

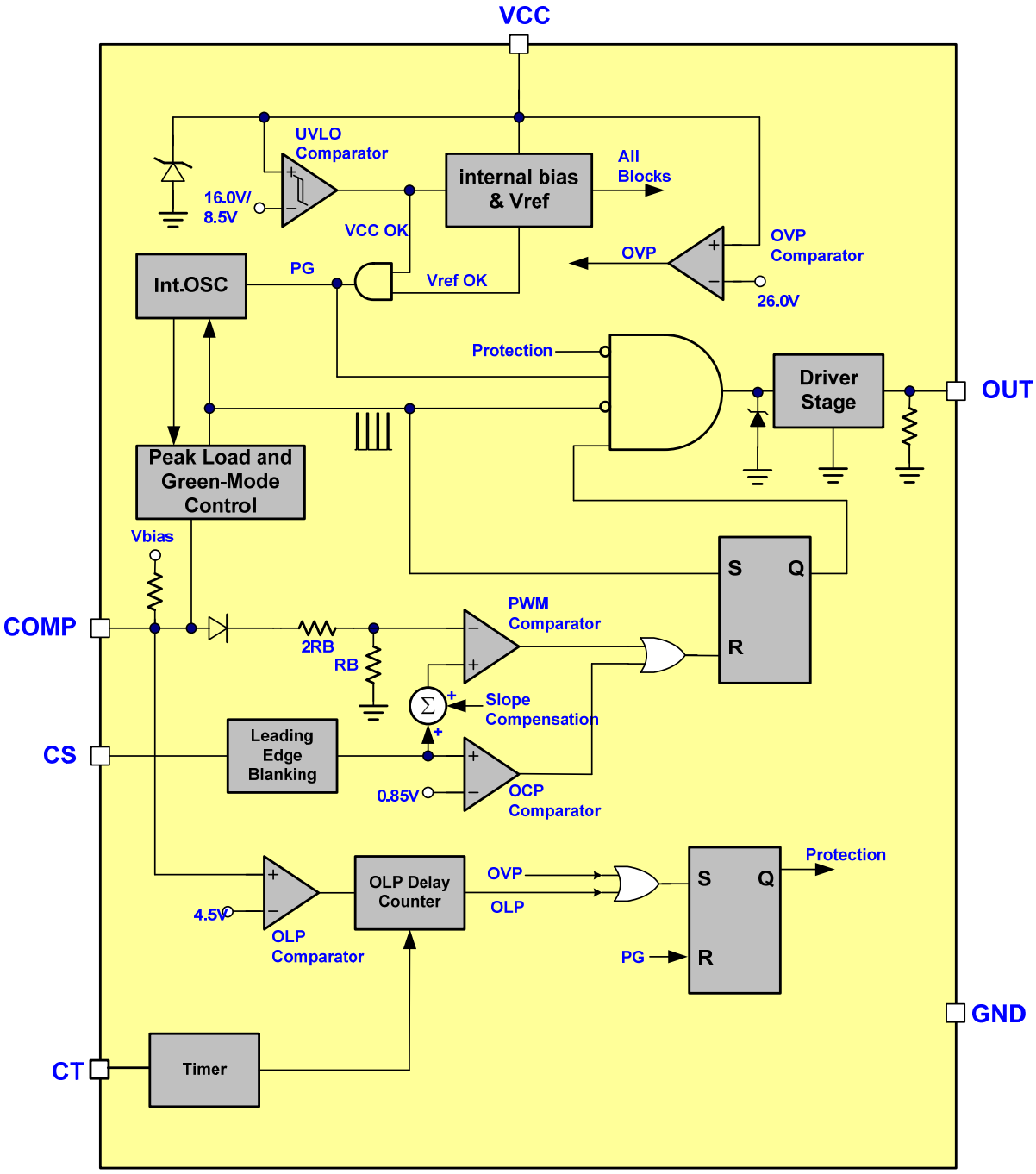
## Protection Mode

| VCC OVP | OLP |
|---|---|
| Auto recovery | Auto recovery |

## Pin Descriptions

| PIN SOT-26 | PIN DIP-8 | NAME | FUNCTION |
|---|---|---|---|
| 1 | 8 | GND | Ground |
| 2 | 7 | COMP | Voltage feedback pin (same as the COMP pin in UC384X). Connect a photo-coupler to close the control loop and achieve the regulation. |
| 3 | 5 | CT | This pin is to program the frequency of the low frequency timer. Connecting a capacitor to ground sets the trembling frequency and OLP delay time. |
| 4 | 4 | CS | Current sense pin, connect it to sense the MOSFET current |
| 5 | 2 | VCC | Supply voltage pin |
| 6 | 1 | OUT | Gate drive output to drive the external MOSFET |

## Block Diagram



## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage VCC | -0.3V ~29V |
| COMP, CT, CS | -0.3V ~6V |
| OUT | -0.3V ~Vcc+0.3V |
| Maximum Junction Temperature | 150°C |
| Operating Ambient Temperature | -20°C to 85°C |
| Operating Junction Temperature | -40°C to 125°C |
| Storage Temperature Range | -65°C to 150°C |
| Package Thermal Resistance (SOT-26, $\theta_{JA}$) | 250°C/W |
| Package Thermal Resistance (DIP-8, $\theta_{JA}$) | 100°C/W |
| Power Dissipation (SOT-26) | 250mW |
| Power Dissipation (DIP-8) | 650mW |
| Lead temperature (Soldering, 10sec) | 260°C |
| ESD Voltage Protection, Human Body Model | 2.5 KV |
| ESD Voltage Protection, Machine Model | 250 V |
| Gate Output Current | 300mA |

**Caution:**

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## Recommended Operating Conditions

| Item | Min. | Max. | Unit |
|---|---|---|---|
| Supply Voltage Vcc | 10 | 24 | V |
| Start-up Resistor Value | 540K | 1.8 M | Ω |
| COMP pin Capacitor Value | 4.7 | 220 | nF |
| CT pin Capacitor Value | 0.047 | 0.47 | μF |

## Electrical Characteristics

($T_A$ = +25°C unless otherwise stated, $V_{CC}$=15.0V)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Supply Voltage (Vcc Pin)** | | | | | |
| Startup Current | | | 12 | 18 | μA |
| Operating Current (with 1nF load on OUT pin) | $V_{COMP}$=0V | | 1.0 | | mA |
| | $V_{COMP}$=4V | | 4.0 | | mA |
| | OLP, OVP Tripped/ Auto | | 0.47 | | mA |
| UVLO (off) | | 7.5 | 8.5 | 9.5 | V |
| UVLO (on) | | 15 | 16 | 17 | V |
| OVP Level | | 25 | 26 | 27 | V |
| **Voltage Feedback (Comp Pin)** | | | | | |
| Short Circuit Current | $V_{COMP}$=0V | | 0.25 | | mA |
| Open Loop Voltage | COMP pin open | | 5.4 | | V |
| Peak Load Mode Threshold Voltage | $F_{SW}$= FREQ1 | | 3.0 | | V |
| Normal Mode Threshold Voltage | $F_{SW}$= FREQ2 | | 2.7 | | V |
| Green Mode Threshold VCOMP | | | 2.25 | | V |
| Zero Duty Threshold VCOMP | | | 1.5 | | V |
| Zero Duty Hysteresis | | | 100 | | mV |
| **Current Sensing (CS Pin)** | | | | | |
| Maximum Input Voltage, $V_{CS\_OFF}$ | | 0.8 | 0.85 | 0.9 | V |
| Leading Edge Blanking Time | | | 230 | | ns |
| Internal Slope Compensation | 0% to $D_{MAX}$. (Linearly increase) | | 300 | | mV |
| Input impedance | | 1 | | | MΩ |
| Delay to Output | | | 100 | | ns |
| **Oscillator for Switching Frequency** | | | | | |
| Peak Load Mode Frequency, FREQ1 | | 180 | 195 | 210 | kHz |
| Normal Mode Frequency, FREQ2 | | 60 | 65 | 70 | kHz |
| Green Mode Frequency, FREQG | | | 22 | | kHz |
| Trembling Frequency | | | ± 6 | | % |
| Temp. Stability | (-20°C ~85°C) | | 5 | | % |
| Voltage Stability | (VCC=10V-25V) | | | 1 | % |

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Gate Drive Output (OUT Pin)** | | | | | |
| Output Low Level | VCC=15V, Io=20mA | | | 1 | V |
| Output High Level | VCC=15V, Io=20mA | 8 | | | V |
| Output Clamp Level | VCC=20V | | 16 | | V |
| Rising Time | Load Capacitance=1000pF | -- | 170 | 350 | ns |
| Falling Time | Load Capacitance=1000pF | | 50 | 100 | ns |
| Max. Duty | | | 75 | | % |
| **OLP (Over Load Protection)** | | | | | |
| OLP Trip Level | | 4.3 | 4.5 | 4.7 | V |
| OLP Delay Time at start up | CT pin=0.047μF | | 39 | | ms |
| OLP Delay Time | CT pin=0.047μF | | 33 | | ms |
| **On Chip OTP (Over Temperature)** | | | | | |
| OTP Level | | | 140 | | °C |
| OTP Hysteresis | | | 30 | | °C |
| **Soft Start Duration** | | | | | |
| Soft Start Duration | CT pin=0.047μF | | 9.4 | | ms |

## Typical Performance Characteristics

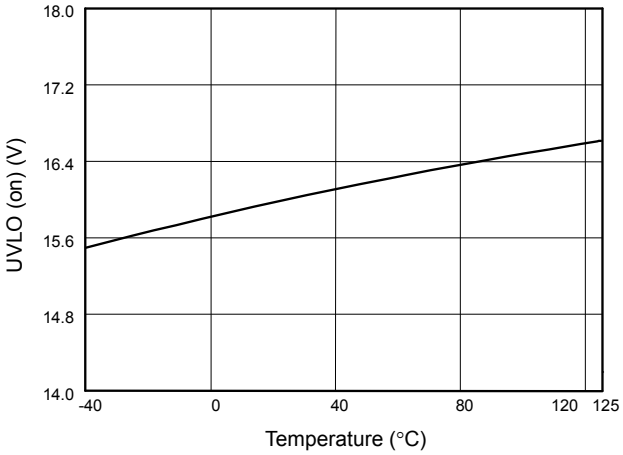



Fig. 1 UVLO (on) vs. Temperature

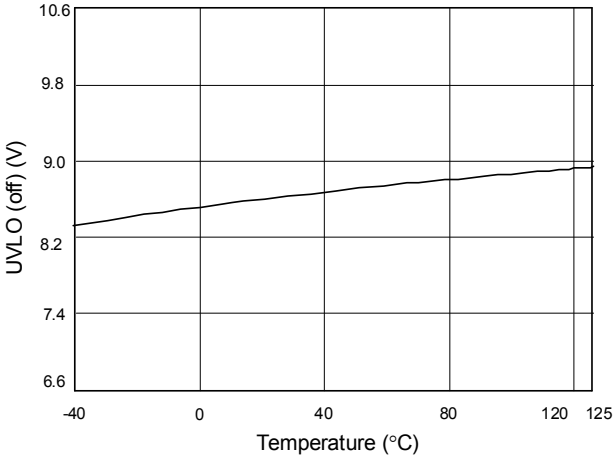



Fig. 2 UVLO (off ) vs. Temperature

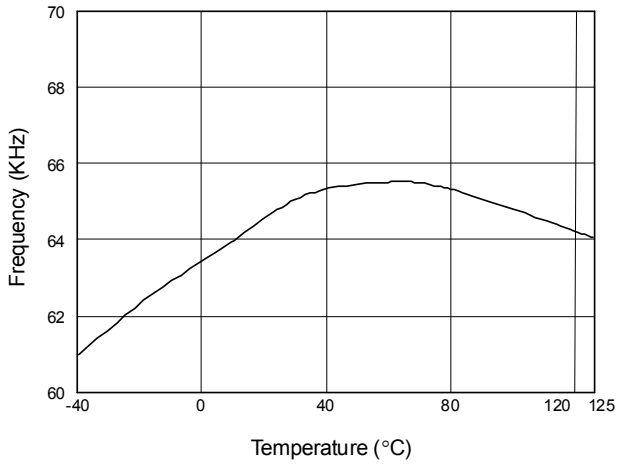



Fig. 3 Normal Mode Frequency vs. Temperature

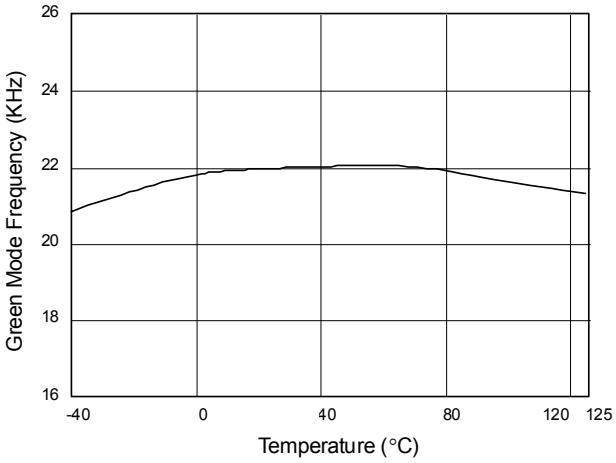



Fig. 4 Green Mode Frequency vs. Temperature

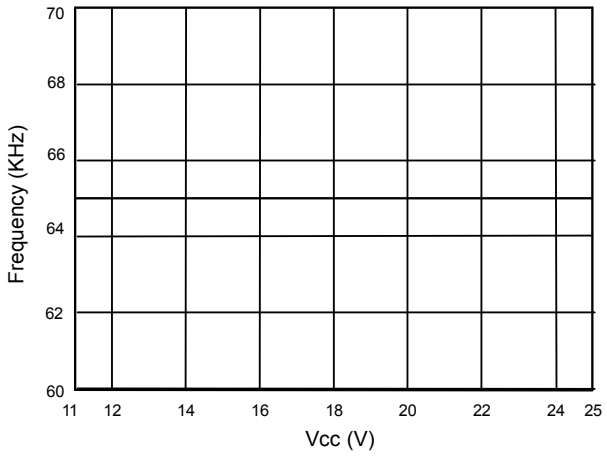



Fig. 5 Frequency vs. Vcc

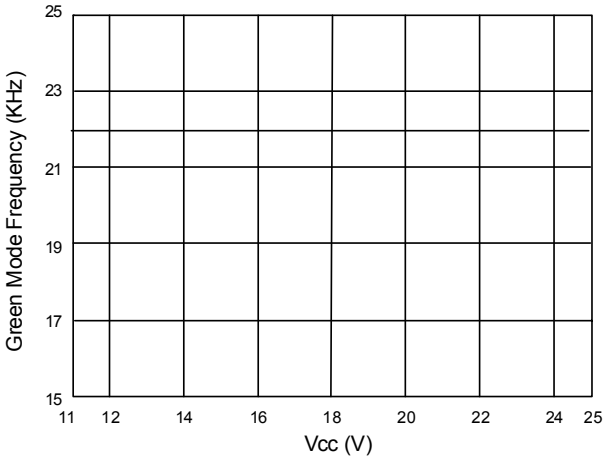



Fig. 6 Green Mode Frequency vs. Vcc

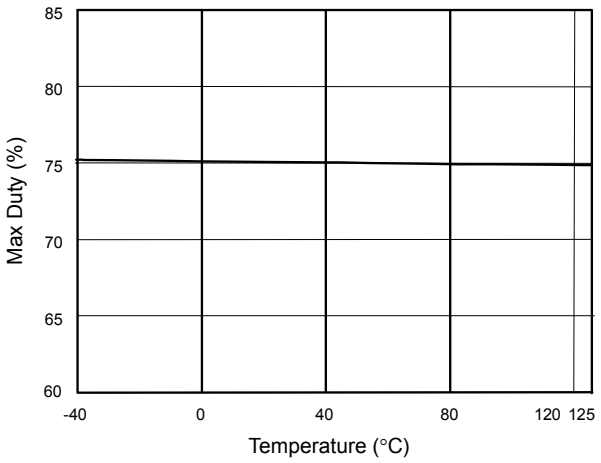



Fig. 7 Max Duty vs. Temperature

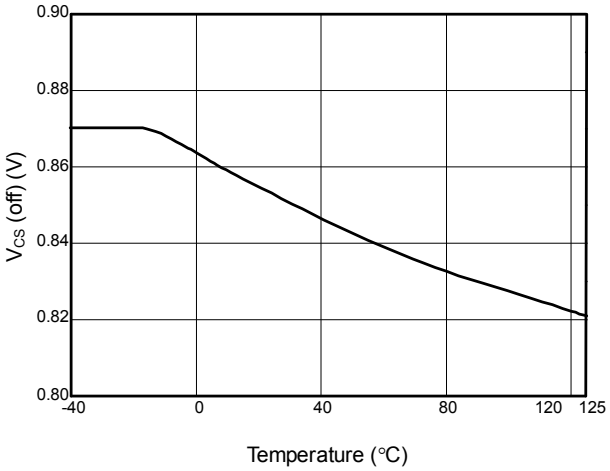



Fig. 8 $V_{CS}$ (off) vs. Temperature

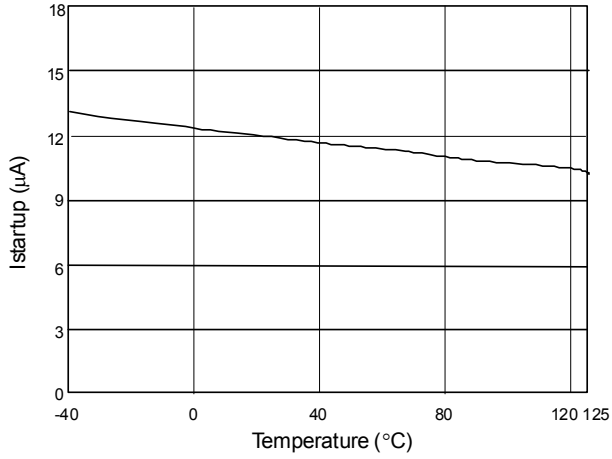



Fig. 9 Startup Current (Istartup) vs. Temperature

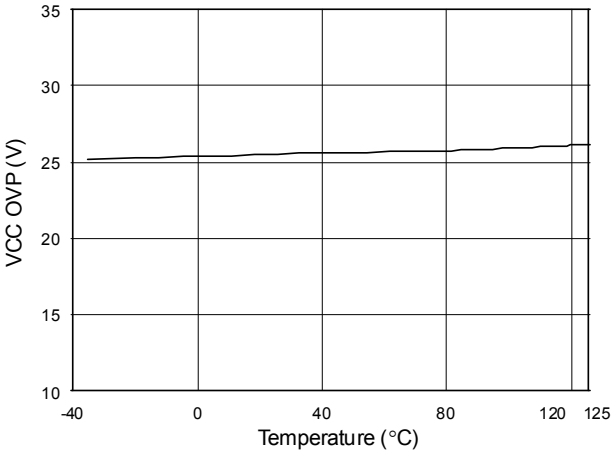



Fig. 10 VCC OVP vs. Temperature

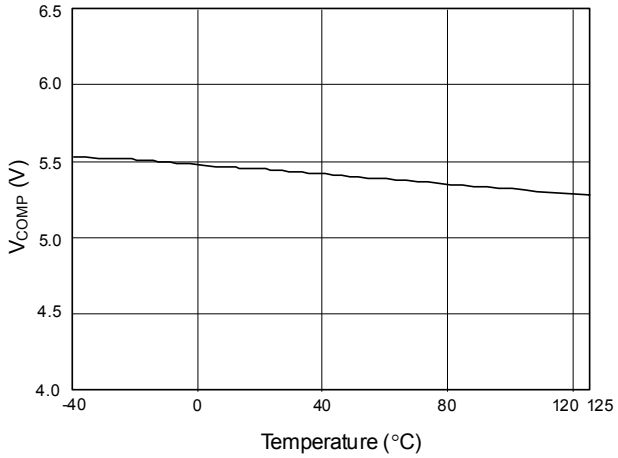



Fig. 11 $V_{COMP}$ open loop voltage vs. Temperature

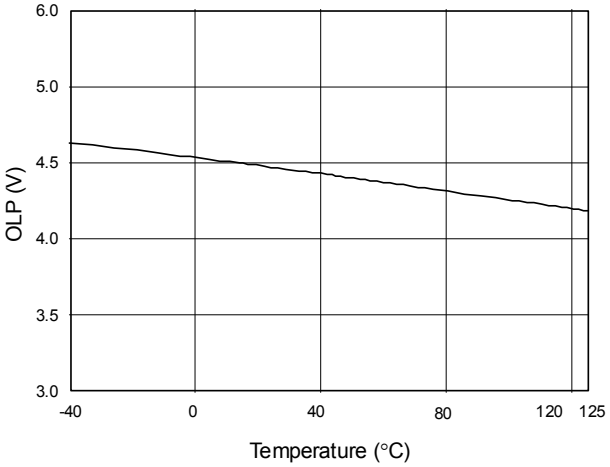



Fig. 12 OLP-Trip Level vs. Temperature

# Application Information

## Operation Overview

The LD7533 is an advanced Green Mode PWM controller built-in with frequency triple, multi-protections and EMI-improved solution in a SOT-26/DIP package. The LD7533 is especially designed for those switching power supplies with peak power. It incorporates frequency triple function and adjustable OLP timer to handle the peak power with delay time. The frequency triple function can reduce the transformer flux and core size. Its major features are described as below.

## Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on VCC pin. It would assure the supply voltage enough to turn on the LD7533 PWM controller and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is built in to prevent the shutdown from the voltage dip during startup.

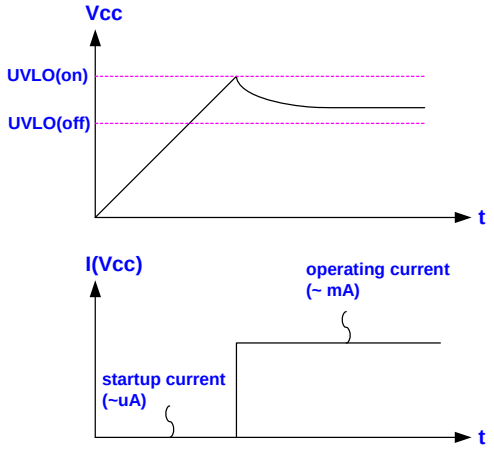



**Fig. 13**

## Startup Current and Startup Circuit

The typical startup circuit to generate VCC is shown in Fig. 14. During the startup transient, VCC is below UVLO threshold. Before it has sufficient voltage to develop OUT pulse to drive the power MOSFET, R1 will provide the startup current to charge the capacitor C1. As soon as VCC obtains enough voltage to turn on the LD7533 and further to deliver the gate drive signal, it will enable the auxiliary winding of the transformer to provide supply current. Lower startup current requirement for the PWM controller will help to increase R1 value and then reduce the power consumption for R1. By using CMOS process and the special circuit design, the maximum startup current for LD7533 is only 18μA.

If a higher resistance value of R1 is chosen, it will usually takes more time to start up. Careful selection for the value of R1 and C1 will optimize the power consumption and startup time.

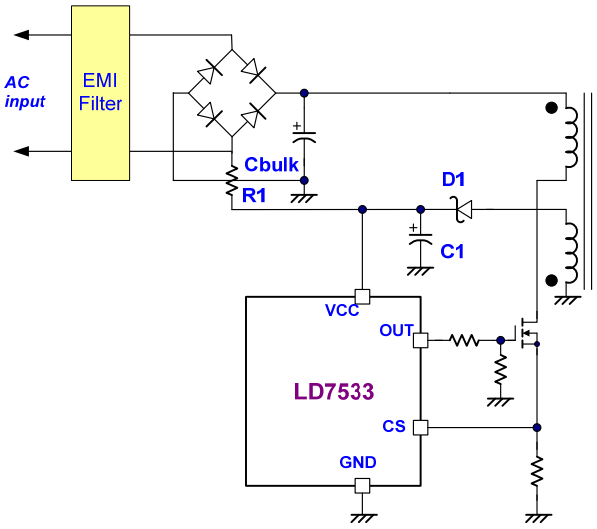



**Fig. 14**

## Oscillator and Switching Frequency

The switching frequency of LD7533 is variable to provide the optimized operations either for peak load, normal load or light load. The LD7533 will increase its switching frequency up to 195 kHz to deliver the peak output power. In light load conditions, the LD7533 operates at a lower frequency to reduce the switching loss. The minimum frequency is limited to 20 kHz to avoid the generation of audible noise.

Fig. 15 shows the characteristics of the switching frequency vs. COMP voltage ($V_{COMP}$). In peak load, $V_{COMP}$ is higher than $V_{IN}$ (2.7V) and the switching frequency will start to linearly increase from 65kHz to 195kHz. In light load, $V_{COMP}$ is lower than $V_{G1}$ (2.25V) and the switching frequency will start to decrease from 65kHz to 20kHz linearly.

The LD7533 can be turned off by pulling COMP pin below 1.5V. Its duty will drop to zero immediately under such condition.

## Frequency Swapping (LD property)

The LD7533 is built in with adjustable Frequency Swapping function, which enables the power supply designers to optimize EMI performance and system cost. The swapping frequency is internally set for ±6% of switching frequency.

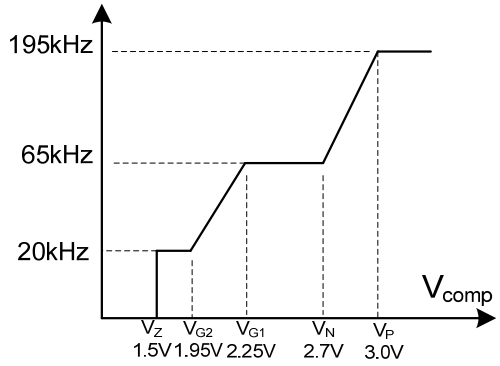



**Fig. 15**

## Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer of typical 300mA driving capability is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of the LD7533 is limited to 75% to avoid the transformer saturation.

## Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both of current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 16, the LD7533 detects the primary MOSFET current on CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

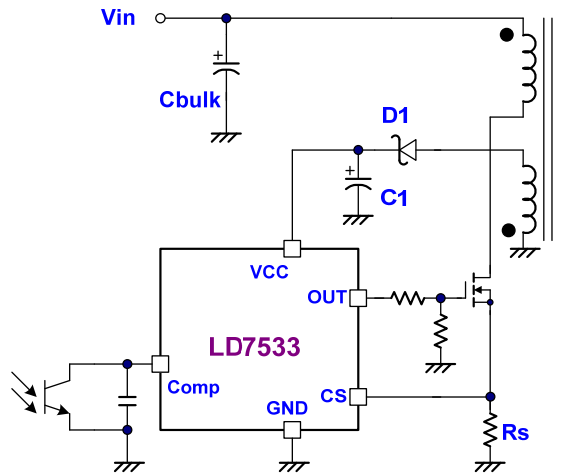



**Fig. 16**

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spikes is less than LEB and the negative spike on the CS pin below -0.3V, the R-C filter is free to eliminate, as shown in Fig.17.

However, the total pulse width of the turn-on spike is determined according to the output power, circuit design and PCB layout. It is strongly recommended to add a smaller R-C filter (as shown in Fig. 18) for larger power application to avoid the CS pin from being damaged by the negative turn-on spike.

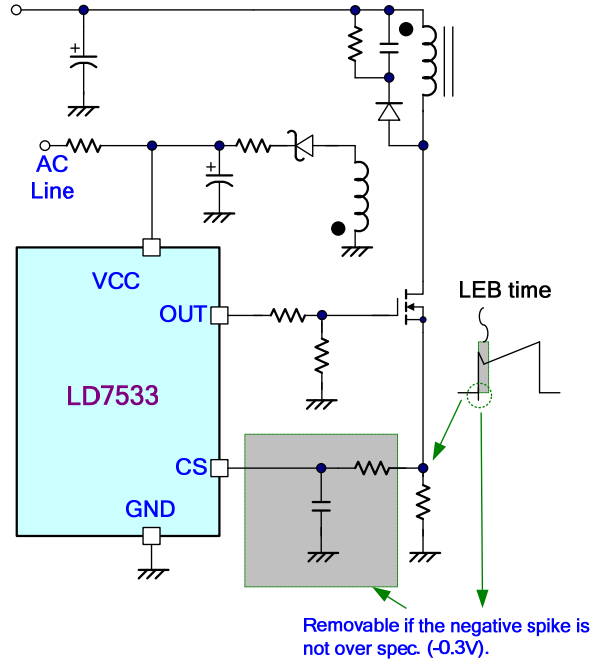



**Fig. 17**

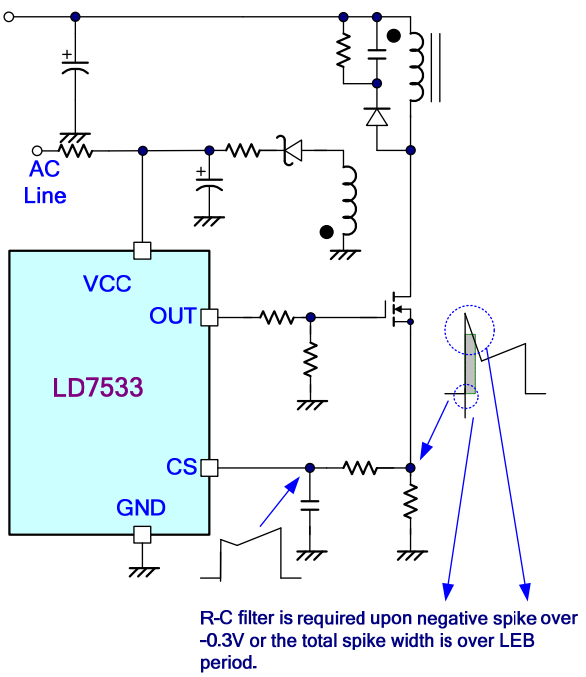



**Fig. 18**

## Voltage Feedback Loop

The voltage feedback signal is provided from the TL431/TL432 at the secondary side through the photo-coupler to the COMP pin of the LD7533. Similar to UC3842, the LD7533 would carry a diode voltage offset at the stage to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{RB}{RA+RB} \times (V_{COMP} - V_F)$$

A pull-high resistor is embedded internally and can be eliminated externally.

## Internal Slope Compensation

In the conventional applications, the problem of the stability is a critical issue for current mode controlling, when it operates over 50% duty-cycle. As UC384X, It takes slope compensation from injecting the ramp signal of the RT/CT pin through a coupling capacitor. It therefore requires no extra design for the LD7533 since it has integrated with it already.

## Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage due to over-load, short or open-loop condition, the LD7533 is implemented with smart OLP function. It also features auto recovery function, as Fig. 19 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (VCOMP). When $V_{COMP}$ ramps up over OLP threshold of 4.5V for more than OLP delay time, it will start the protection to turn off the gate output and stop the switching of power circuit. The OLP delay time, set by CT pin, is to prevent any false-trigger caused by the power-on and turn-off transient. The higher CT value it is, the more OLP delay time it will take.

The equations for OLP delay time are shown as:

$$T_{OLP} = CT_{(\mu F)} \times 825(ms) \quad \text{during start-up}$$

$$T_{OLP} = CT_{(\mu F)} \times 700(ms) \quad \text{after start-up}$$

With the protection, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

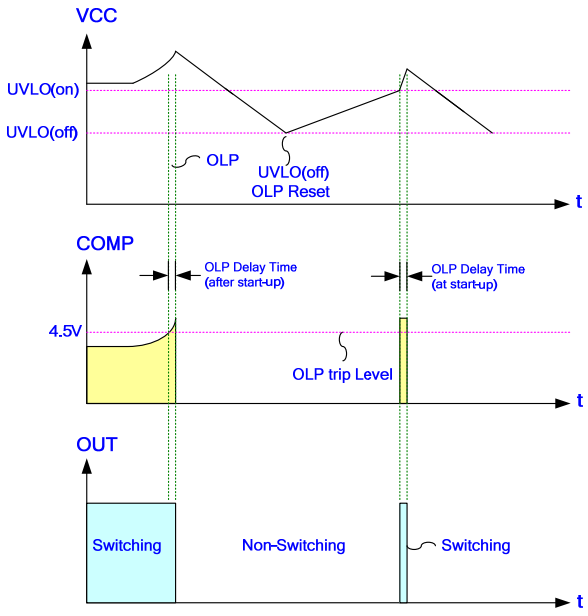



**Fig. 19**

## OVP (Over Voltage Protection) on Vcc - Auto Recovery

The maximum VGS ratings of the power MOSFETs are mostly for 30V. To prevent the VGS from entering fault condition, LD7533 series are implemented with OVP function on VCC. Whenever VCC voltage rises above the OVP threshold, the output gate drive circuit will be shutdown simultaneously and the switching of the power MOSFET is disabled until the next UVLO(on).

VCC and OVP functions are auto-recoverable. If the OVP condition, usually caused by open-loop of feedback, is not released, VCC will trip OVP level again and shutdown the output. VCC works in hiccup mode. Fig. 20 shows its operation.

Soon after OVP condition is removed, VCC level will resume and the output will return to the normal operation.

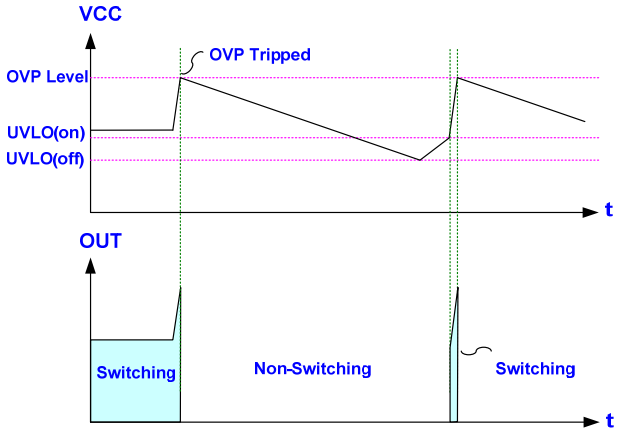



Fig. 20

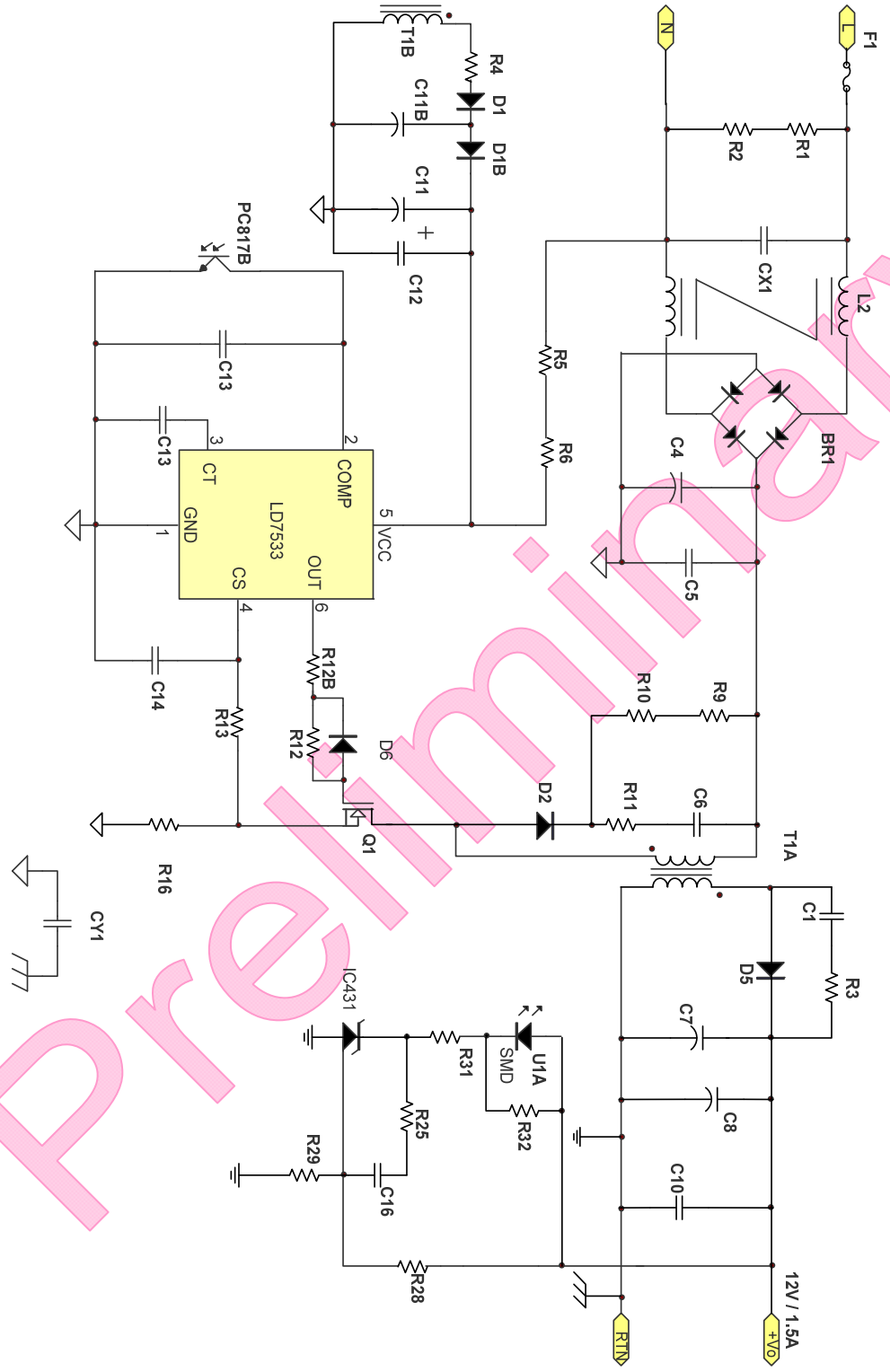
## Fault Protection

There are several crucial protections integrated in the LD7533 to prevent from damage to the power supply. Those damages usually come from open or short conditions.

In case of such conditions listed below, the gate output will turn off immediately to protect the power circuit.

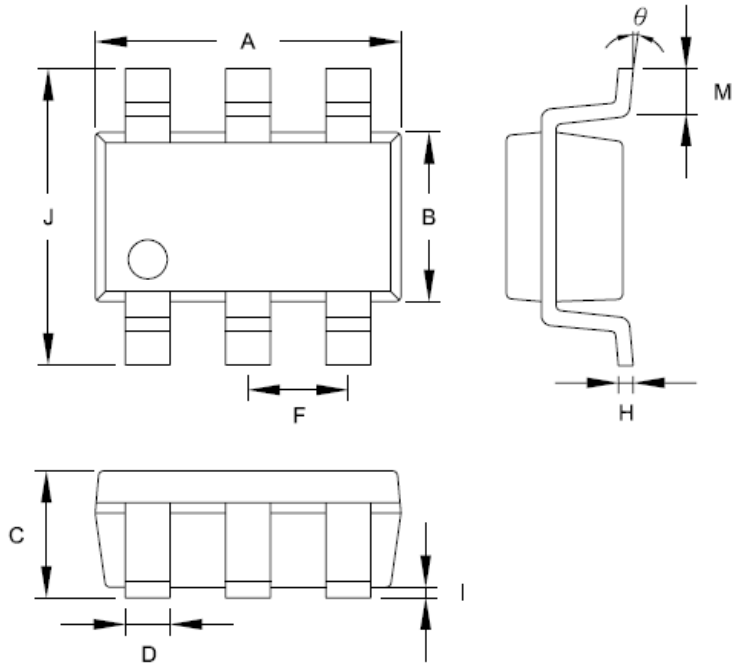
1. CS pin floating
2. COMP pin floating

## Reference Application Circuit --18W (12V/1.5A, Peak 3A), no-load <0.1W



## Package Information

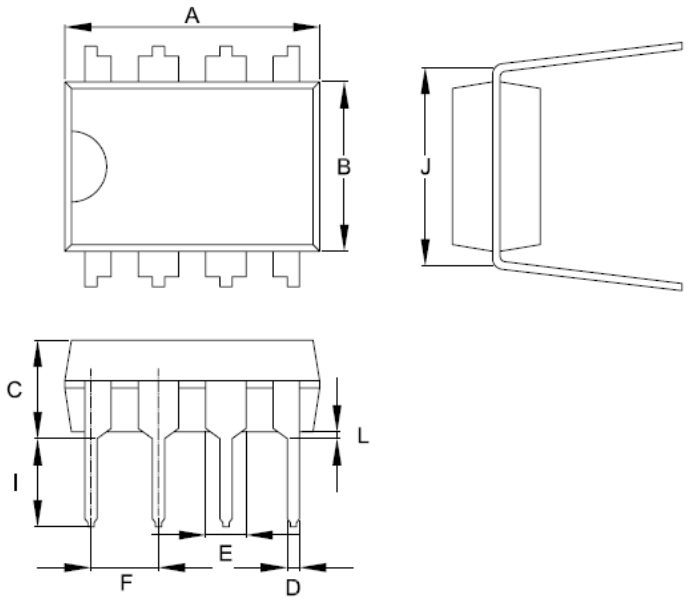
**SOT-26**




| Symbol | Dimension in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 2.692 | 3.099 | 0.106 | 0.122 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| C | ------- | 1.450 | ------- | 0.057 |
| D | 0.300 | 0.500 | 0.012 | 0.020 |
| F | 0.95 TYP | | 0.037 TYP | |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| I | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 2.600 | 3.000 | 0.102 | 0.118 |
| M | 0.300 | 0.600 | 0.012 | 0.024 |
| θ | 0° | 10° | 0° | 10° |

## Package Information

**DIP-8**




| Symbol | Dimension in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 9.017 | 10.160 | 0.355 | 0.400 |
| B | 6.096 | 7.112 | 0.240 | 0.280 |
| C | ----- | 5.334 | ------ | 0.210 |
| D | 0.356 | 0.584 | 0.014 | 0.023 |
| E | 1.143 | 1.778 | 0.045 | 0.070 |
| F | 2.337 | 2.743 | 0.092 | 0.108 |
| I | 2.921 | 3.556 | 0.115 | 0.140 |
| J | 7.366 | 8.255 | 0.29 | 0.325 |
| L | 0.381 | ------ | 0.015 | -------- |

### Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

## Revision History

| Rev. | Date | Change Notice |
|---|---|---|
| 00 | 9/3/2010 | Original Specification |