

## Green-Mode PWM Controller with Frequency Swapping and Integrated Protections

Rev. 00

### General Description

The LD7537S is built-in with several functions, protection and EMI-improved solution in a tiny package. It takes less components counts or circuit space, especially ideal for those total solutions of low cost.

The implemented functions include low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. It also features more protections like OLP (Over Load Protection) and OVP (Over Voltage Protection) to prevent circuit damage occurred under abnormal conditions.

Furthermore, the Frequency Swapping function is to reduce the noise level and thus helps the power circuit designers to easily deal with the EMI filter design by spending minimum amount of component cost and developing time.

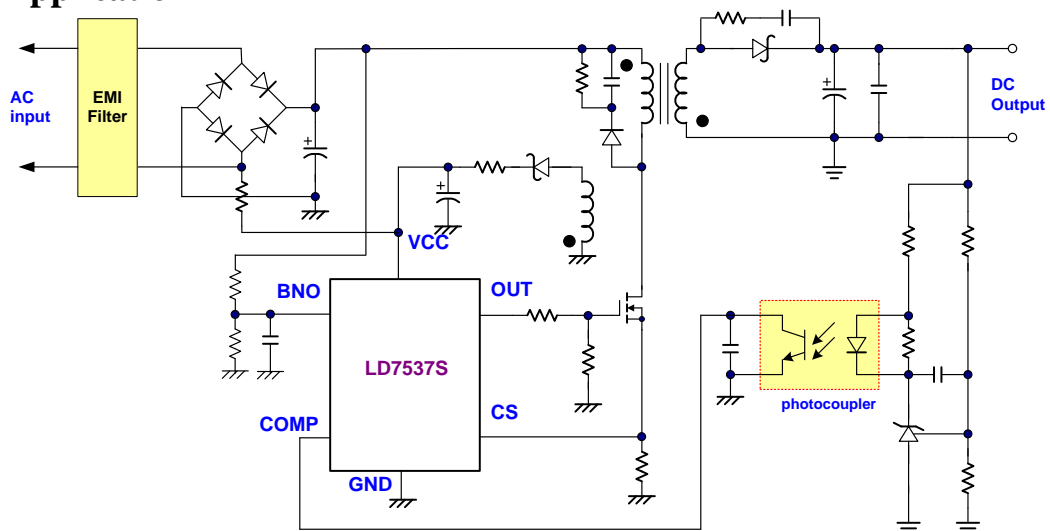
### Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (<20 $\mu$ A)
- Current Mode Control
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Frequency Swapping
- Internal Slope Compensation
- OVP (Over Voltage Protection) on Vcc Pin
- Brownout Protection
- OLP (Over Load Protection)
- 300mA Driving Capability

### Applications

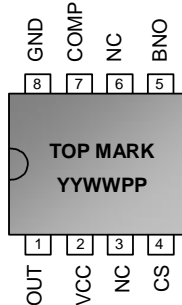
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

### Typical Application

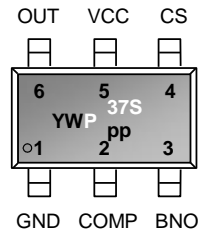


## Pin Configuration

DIP-8 (TOP VIEW)



SOT-26 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005.....)  
 WW, W : Week code  
 PP : Production code  
 P37S : LD7537S

## Ordering Information

Part number	Package	Top Mark	Shipping
LD7537S GL	SOT-26	YWP/37S	3000 /tape & reel
LD7537S GN	DIP-8	LD7537S GN	3600 /tube /Carton

The LD7537S is green packaged.

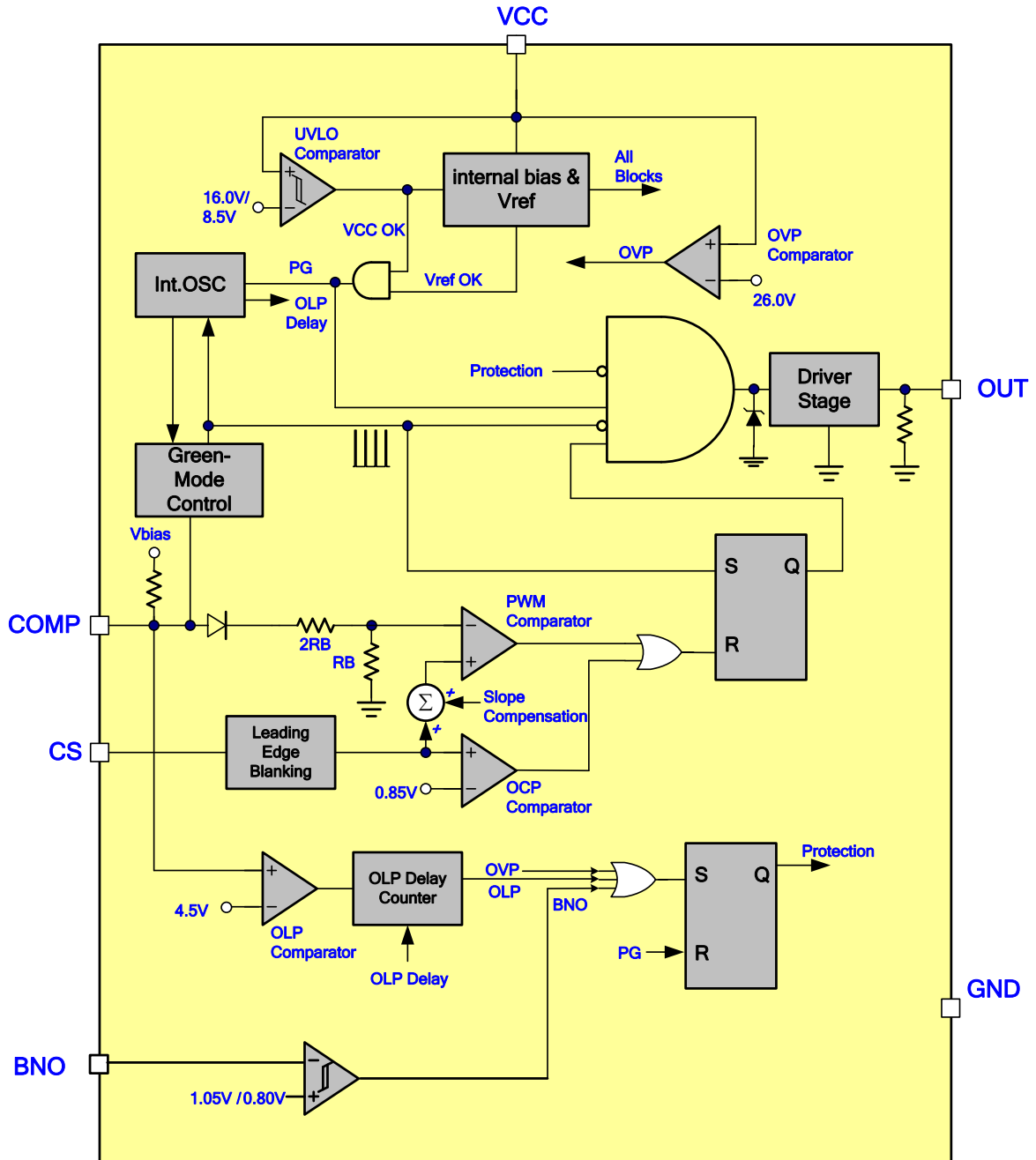
## Protection Mode

Switching Freq.	VCC OVP	OLP	BNO Pin
65kHz	Auto recovery	Auto recovery/ 65ms	Auto recovery

## Pin Descriptions

SOT-26	DIP-8	NAME	FUNCTION
1	8	GND	Ground
2	7	COMP	Voltage feedback pin (same as the COMP pin in UC384X). Connect a photo-coupler to close the control loop and achieve the regulation.
3	5	BNO	Brownout Protection Pin. Connect a resistor divider between this pin and bulk capacitor voltage to set the brownout level. If the voltage is less than threshold voltage, the PWM output will be disabled.
4	4	CS	Current sense pin, connect it to sense the MOSFET current
5	2	VCC	Supply voltage pin
6	1	OUT	Gate drive output to drive the external MOSFET

## Block Diagram



## Absolute Maximum Ratings

Supply Voltage VCC.....	-0.3V ~29V
COMP, BNO, CS.....	-0.3V ~6V
OUT.....	-0.3V ~Vcc+0.3V
Maximum Junction Temperature.....	150°C
Operating Ambient Temperature.....	-20°C to 85°C
Operating Junction Temperature.....	-40°C to 125°C
Storage Temperature Range.....	-65°C to 150°C
Package Thermal Resistance (SOT-26, $\theta_{JA}$ ).....	250°C/W
Package Thermal Resistance (DIP-8, $\theta_{JA}$ ).....	100°C/W
Power Dissipation (SOT-26).....	250mW
Power Dissipation (DIP-8).....	650mW
Lead temperature (Soldering, 10sec).....	260°C
ESD Voltage Protection, Human Body Model.....	2.5 KV
ESD Voltage Protection, Machine Model.....	250 V
Gate Output Current.....	300mA

### Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

## Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage Vcc	10	24	V
Start-up resistor Value	540K	1.8M	$\Omega$

## Electrical Characteristics

( $T_A = +25^\circ\text{C}$  unless otherwise stated,  $V_{CC}=15.0\text{V}$ )

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Supply Voltage (Vcc Pin)</b>					
Startup Current			12	20	$\mu\text{A}$
Operating Current (with 1nF load on OUT pin)	$V_{\text{COMP}}=0\text{V}$		1.0		mA
	$V_{\text{COMP}}=3\text{V}$		2.0		mA
	OLP Tripped/ Auto		0.47		mA
	OVP Tripped/ Auto		0.47		mA
UVLO (OFF)		7.5	8.5	9.5	V
UVLO (ON)		15	16	17	V
OVP Level		25	26	27	V
<b>Voltage Feedback (Comp Pin)</b>					
Short Circuit Current	$V_{\text{COMP}}=0\text{V}$		0.25		mA
Open Loop Voltage	COMP pin open		5.4		V
Green Mode Threshold VCOMP	*		2.4		V
Zero Duty Threshold VCOMP			1.5		V
Zero Duty Hysteresis			100		mV
<b>Current Sensing (CS Pin)</b>					
Maximum Input Voltage, $V_{\text{CS\_OFF}}$			0.85		V
Maximum Input Voltage, $V_{\text{CS\_MIN}}$	For High Line		0.65		V
Leading Edge Blanking Time			230		ns
Internal Slope Compensation	0% to $D_{\text{MAX}}$ . (Linearly increase)		300		mV
Input impedance	*	1			$\text{M}\Omega$
Delay to Output	*		100		ns
<b>Oscillator for Switching Frequency</b>					
Frequency, FREQ		60	65	70	kHz
Green Mode Frequency, FREQG			22		kHz
Trembling Frequency			$\pm 4.0$		kHz
Temp. Stability	$(-20^\circ\text{C} \sim 85^\circ\text{C})$ *		5		%
Voltage Stability	$(V_{\text{CC}}=11\text{V}\sim 25\text{V})$ *			1	%
<b>Gate Drive Output (OUT Pin)</b>					
Output Low Level	$V_{\text{CC}}=15\text{V}$ , $I_o=20\text{mA}$			1	V
Output High Level	$V_{\text{CC}}=15\text{V}$ , $I_o=20\text{mA}$	8			V
Rising Time	Load Capacitance=1000pF		170	350	ns
Falling Time	Load Capacitance=1000pF		50		ns
Output High Clamp Level	$V_{\text{CC}}=20\text{V}$		16		V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Max. Duty	*		75		%
<b>OLP (Over Load Protection)</b>					
OLP Trip Level		4.3	4.5	4.7	V
OLP Delay Time			65		ms
<b>Brownout Protection (BNO Pin)</b>					
Brownout Turn-On Trip Level		1.00	1.05	1.10	V
Brownout Turn-Off Trip Level		0.75	0.80	0.85	V
BNO Pin De-bounce Time			250		us
<b>On Chip OTP (Over Temperature)</b>					
OTP Level	*		140		°C
OTP Hysteresis	*		30		°C
<b>Soft Start Duration</b>					
Soft Start Duration	*		5		ms

\*: These parameters are guaranteed by design.

## Typical Performance Characteristics

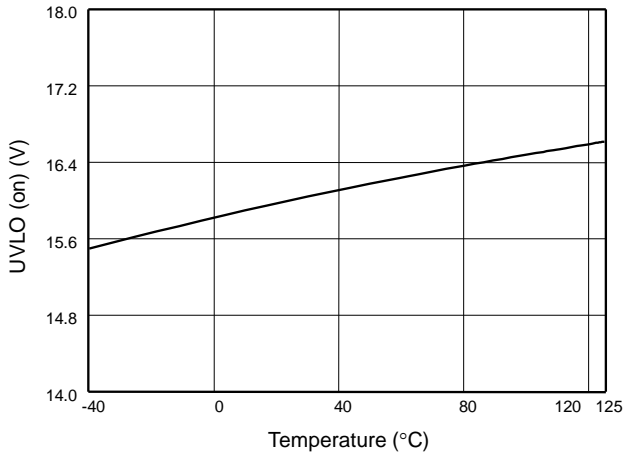


Fig. 1 UVLO (on) vs. Temperature

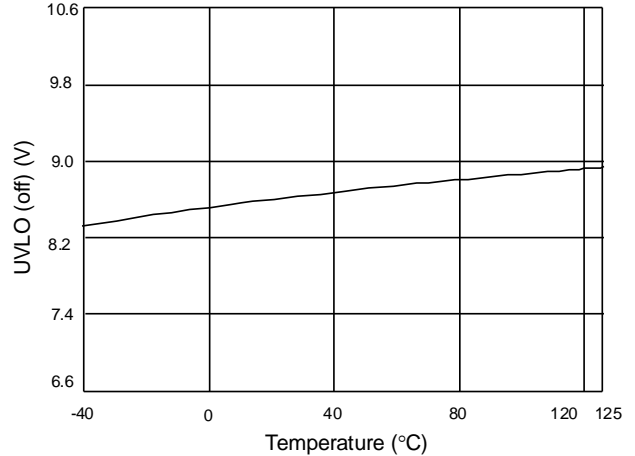


Fig. 2 UVLO (off) vs. Temperature

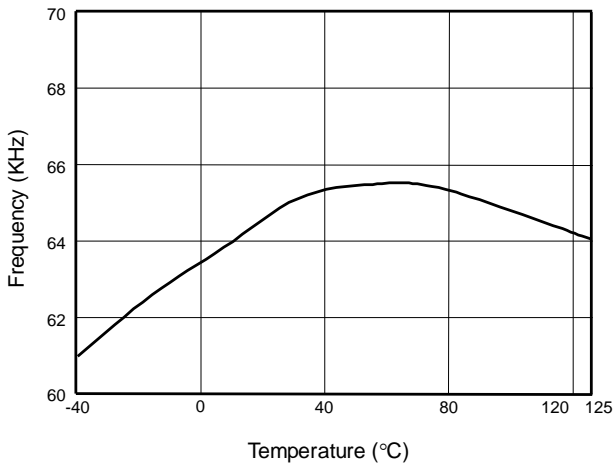


Fig. 3 Frequency vs. Temperature

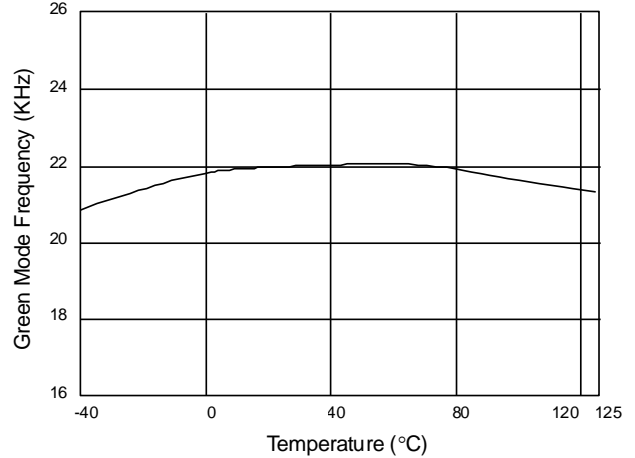


Fig. 4 Green Mode Frequency vs. Temperature

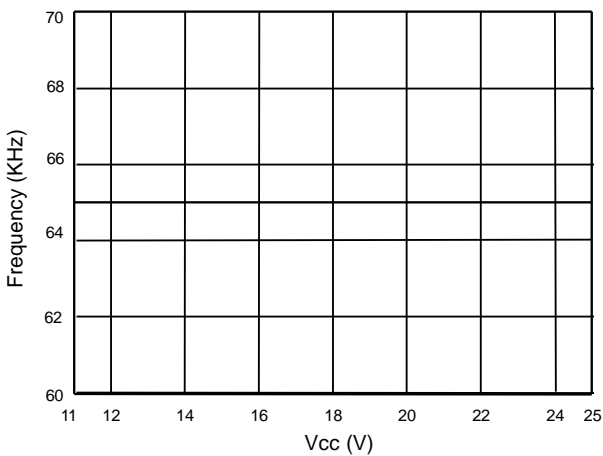


Fig. 5 Frequency vs. Vcc

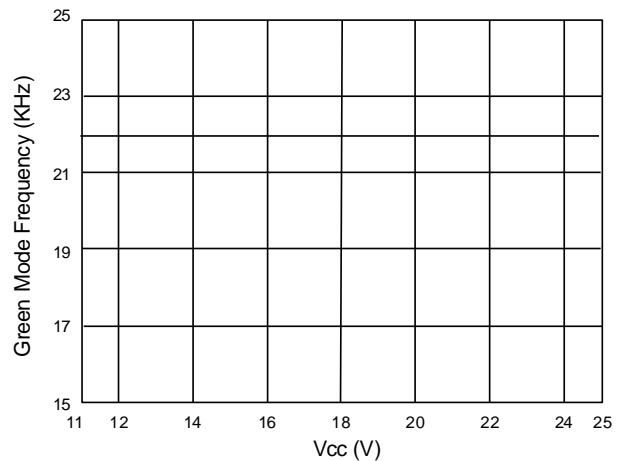


Fig. 6 Green Mode Frequency vs. Vcc

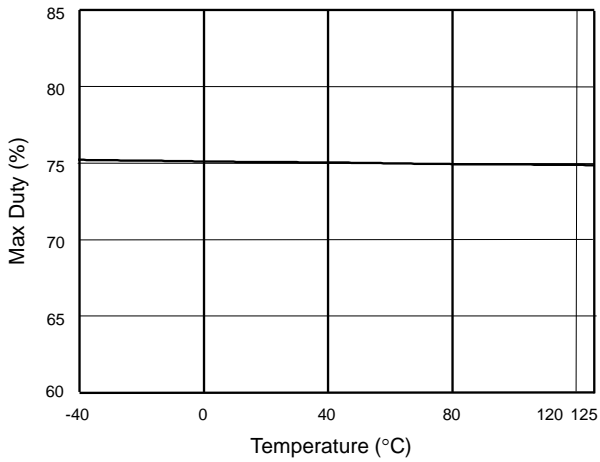


Fig. 7 Max Duty vs. Temperature

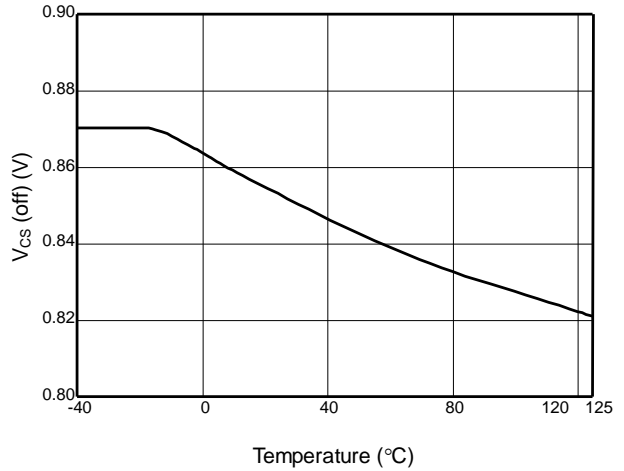


Fig. 8 V<sub>CS</sub> (off) vs. Temperature

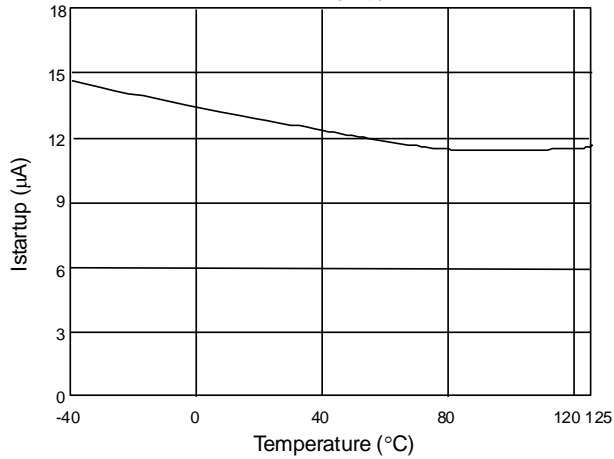


Fig. 9 Startup Current (I<sub>startup</sub>) vs. Temperature

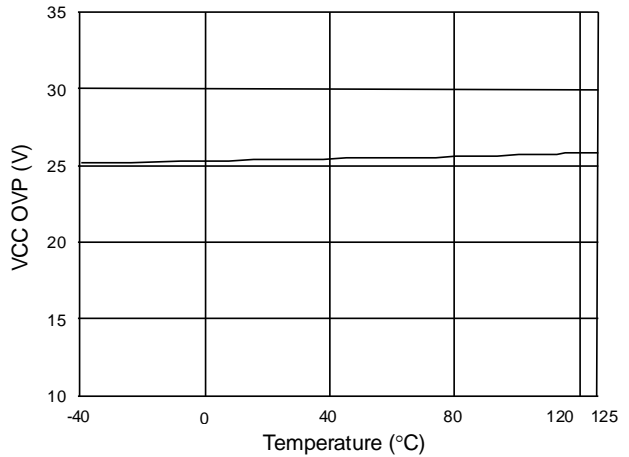


Fig. 10 VCC OVP vs. Temperature

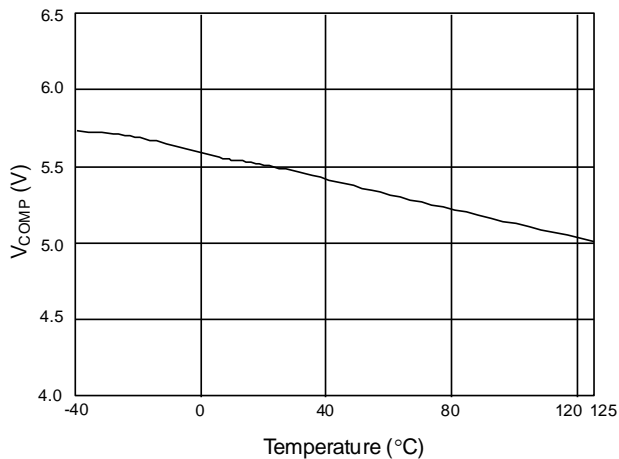


Fig. 11 V<sub>COMP</sub> open loop voltage vs. Temperature

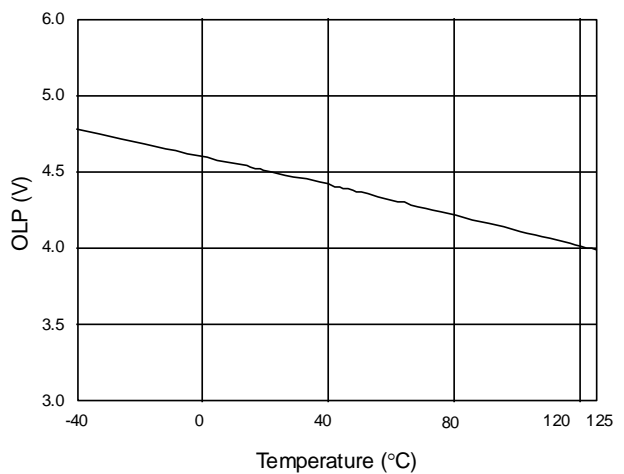


Fig. 12 OLP-Trip Level vs. Temperature



## Application Information

### Operation Overview

The LD7537S meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

### Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage across VCC pin. It would assure the supply voltage enough to turn on the LD7537S PWM controller and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.0V and 8.5V, respectively.

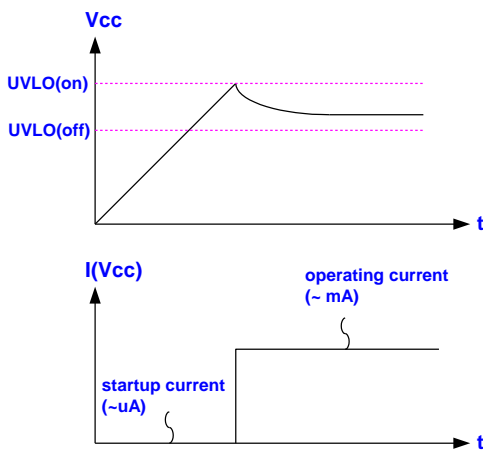
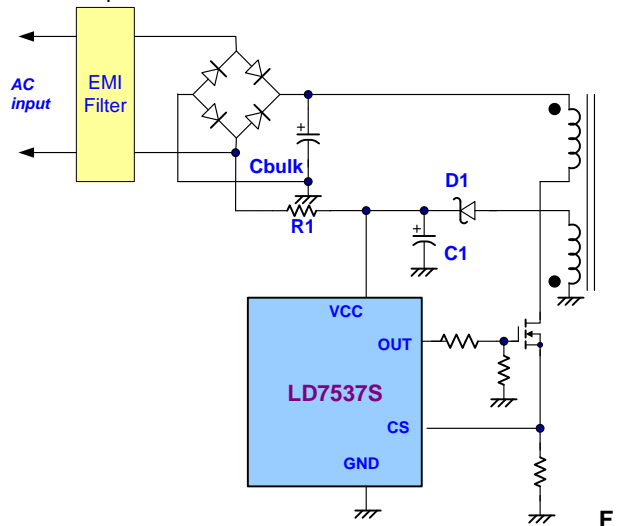


Fig. 13

### Startup Current and Startup Circuit

The typical startup circuit to generate V<sub>CC</sub> of the LD7537S is shown in Fig. 14. During the startup transient, the V<sub>CC</sub> is below UVLO threshold. Before it has sufficient voltage to develop OUT pulse to drive the power MOSFET, R<sub>1</sub> will provide the startup current to charge the capacitor C<sub>1</sub>. Once V<sub>CC</sub> obtains enough voltage to turn on the LD7537S and further to deliver the gate drive signal, it will enable the auxiliary winding of the transformer to provide supply

current. Lower startup current requirement on the PWM controller will help to increase the value of R<sub>1</sub> and then reduce the power consumption on R<sub>1</sub>. By employing CMOS process and the special circuit design, the LD7537S consumes only 20μA for startup current. If a higher resistance value of the R<sub>1</sub> is chosen, it will usually spend more time to start up. To carefully select the value of R<sub>1</sub> and C<sub>1</sub> will optimize the power consumption and startup time.



ig. 14

### Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD7537S detects the primary MOSFET current over CS pin for the peak current mode control and also for the pulse-by-pulse current limit.

In general, the power converter will provide more current when input voltage alters to high due to the signal propagation delay. This can be compensated through LD7537S. It's controlled by varying the current limit with the duty cycles in corresponding to V<sub>cs\_off</sub>. As shown in Fig.15, V<sub>cs\_off</sub> (corresponding to current limit) is in direct proportion to duty ratio in a certain segment and is fixed at

high or low if duty ratio is over or below threshold values, respectively. As a result, the current limit will be lowered at high-line inputs. This compensation control mechanism is developed with patents pending by Leadtrend Technology.

The maximum voltage threshold of the current sensing pin is set at 0.85V for low-line input. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

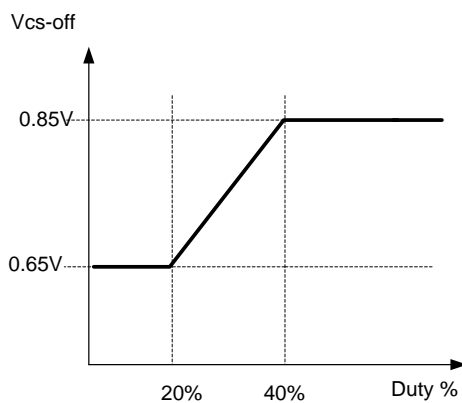


Fig. 15

A 230nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent false-trigger from the current spike. In those low power applications, if the total pulse width of the turn-on spikes is less than 230nS and the negative spike on the CS pin below -0.3V, then, the R-C filter is free to eliminate. (As shown in Fig.16).

However, the total pulse width of the turn-on spike is determined according to output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in Fig. 18) for larger power application to avoid the CS pin being damaged by the negative turn-on spike.

### Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 300mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of

LD7537S is limited to 75% to avoid the transformer saturation.

### Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD7537S. Similar to UC3842, the LD7537S would carry a diode voltage offset at the stage to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{R_B}{R_A + R_B} \times (V_{COMP} - V_F)$$

A pull-high resistor is embedded internally and can be eliminated externally.

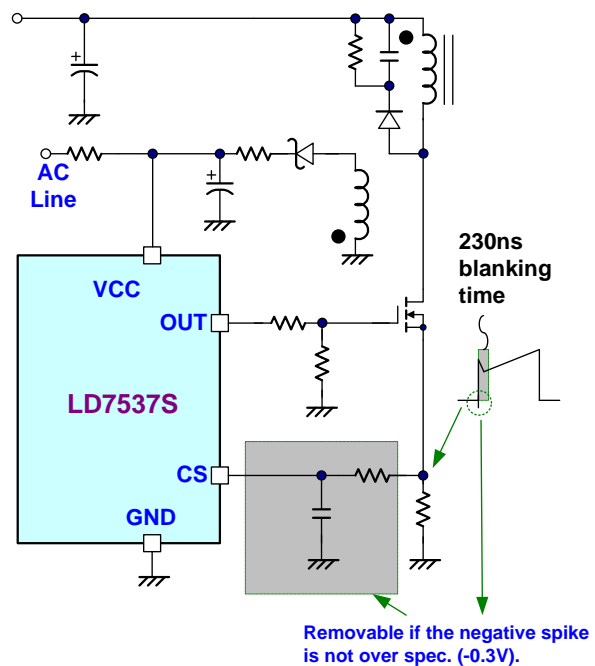


Fig. 16

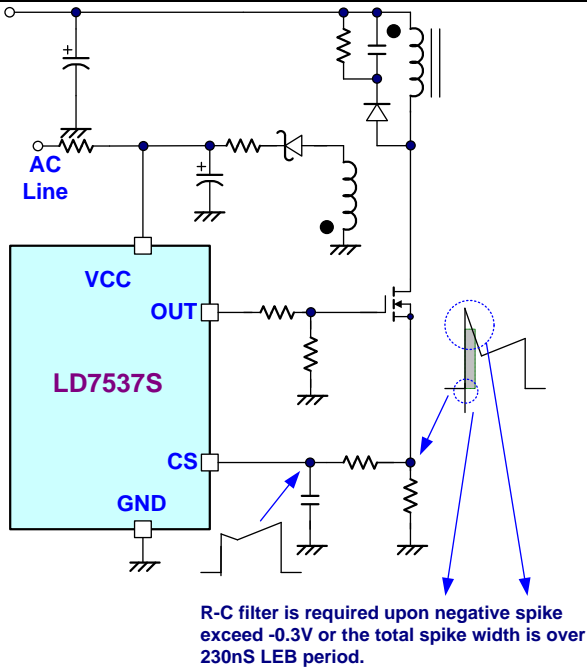


Fig. 17

### Internal Slope Compensation

In the conventional applications, the problem of the stability is a critical issue for current mode controlling, when it operates over 50% duty-cycle. As UC384X, It takes slope compensation from injecting the ramp signal of the RT/CT pin through a coupling capacitor. It therefore requires no extra design for the LD7537S since it has integrated it already.

### On/Off Control

The LD7537S can be turned off by pulling COMP pin below 1.5V. The gate output pin of the LD7537S will be disabled immediately under such condition. The off-mode can be released when the pull-low signal is removed.

### Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage due to over-load condition and short or open-loop condition, the LD7537S is implemented with smart OLP function. It also features auto recovery function; see Fig. 18 for the waveform. In case of fault condition, the feedback system will force the

voltage loop toward the saturation and then pull the voltage high on COMP pin (V<sub>COMP</sub>). When the V<sub>COMP</sub> ramps up to the OLP threshold of 4.5V and continues over OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

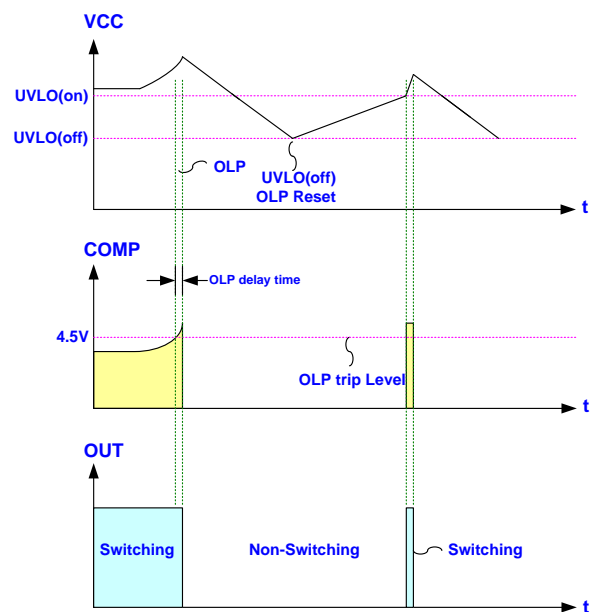


Fig. 18

### OVP (Over Voltage Protection) on V<sub>cc</sub> - Auto Recovery

The maximum V<sub>GS</sub> ratings of the power MOSFETs are mostly for 30V. To prevent the V<sub>GS</sub> enter fault condition, LD7537S is implemented with OVP function on V<sub>cc</sub>. Whenever the V<sub>cc</sub> voltage is higher than the OVP threshold, the output gate drive circuit will be shutdown simultaneously and the switching of the power MOSFET is disabled until the next UVLO(on).

The V<sub>cc</sub> OVP function of LD7537S is auto-recoverable. If the OVP condition, usually caused by open-loop of feedback, is not released, the V<sub>cc</sub> will tripped the OVP level again and re-shutdown the output. The V<sub>cc</sub> works in hiccup mode. Figure 19 shows its operation.

Otherwise, when the OVP condition is removed, the Vcc level will be resumed and the output will automatically return to the normal operation.

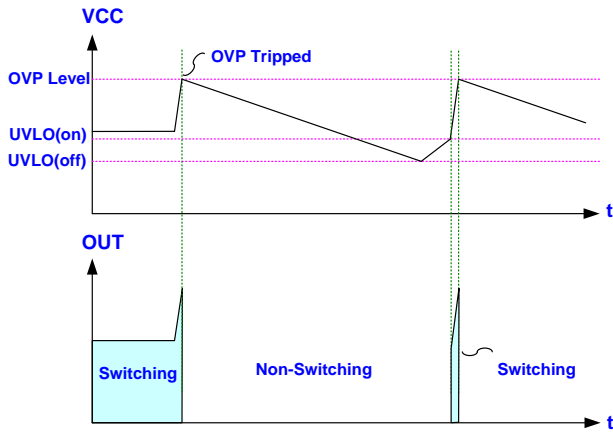


Fig. 19

## Brownout Protection

The LD7537S is programmable to set the brownout protection point through BNO pin. The voltage across the BNO pin is proportional to the bulk capacitor voltage, referred as the line voltage. A brownout comparator is implemented to detect the abnormal line condition. As soon as the condition is detected, it will shut down the controller to prevent the damage. Figure 20 shows the operation. When VBNO falls below 0.80V, the gate output will remain off even Vcc has already achieved UVLO(ON). It therefore makes Vcc hiccup between UVLO(ON) and UVLO(OFF). Unless the line voltage is enough to pull VBNO larger than 1.05V, the gate output will not start switching even when the next UVLO(ON) is tripped. A hysteresis is implemented to prevent the false trigger during turn-on and turn-off. Figure 20 shows the circuit.

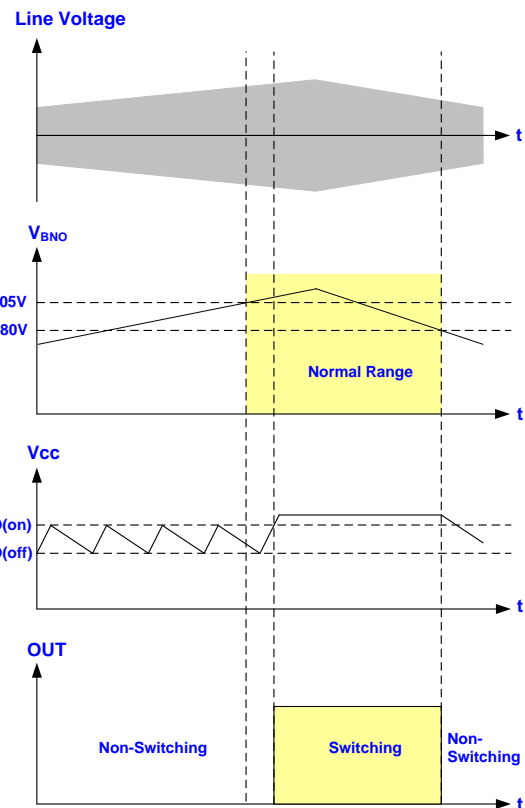


Fig. 20

## Oscillator and Switching Frequency

The LD7537S is implemented with Frequency Swapping which helps the power supply designers to both optimize EMI performance and lower system cost. The switching frequency substantially centers at 65KHz, and swap between a range of  $\pm 4$ KHz.

## Green-Mode Operation

By employing the green-mode control, the switching frequency can be minimized under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property.

## Fault Protection

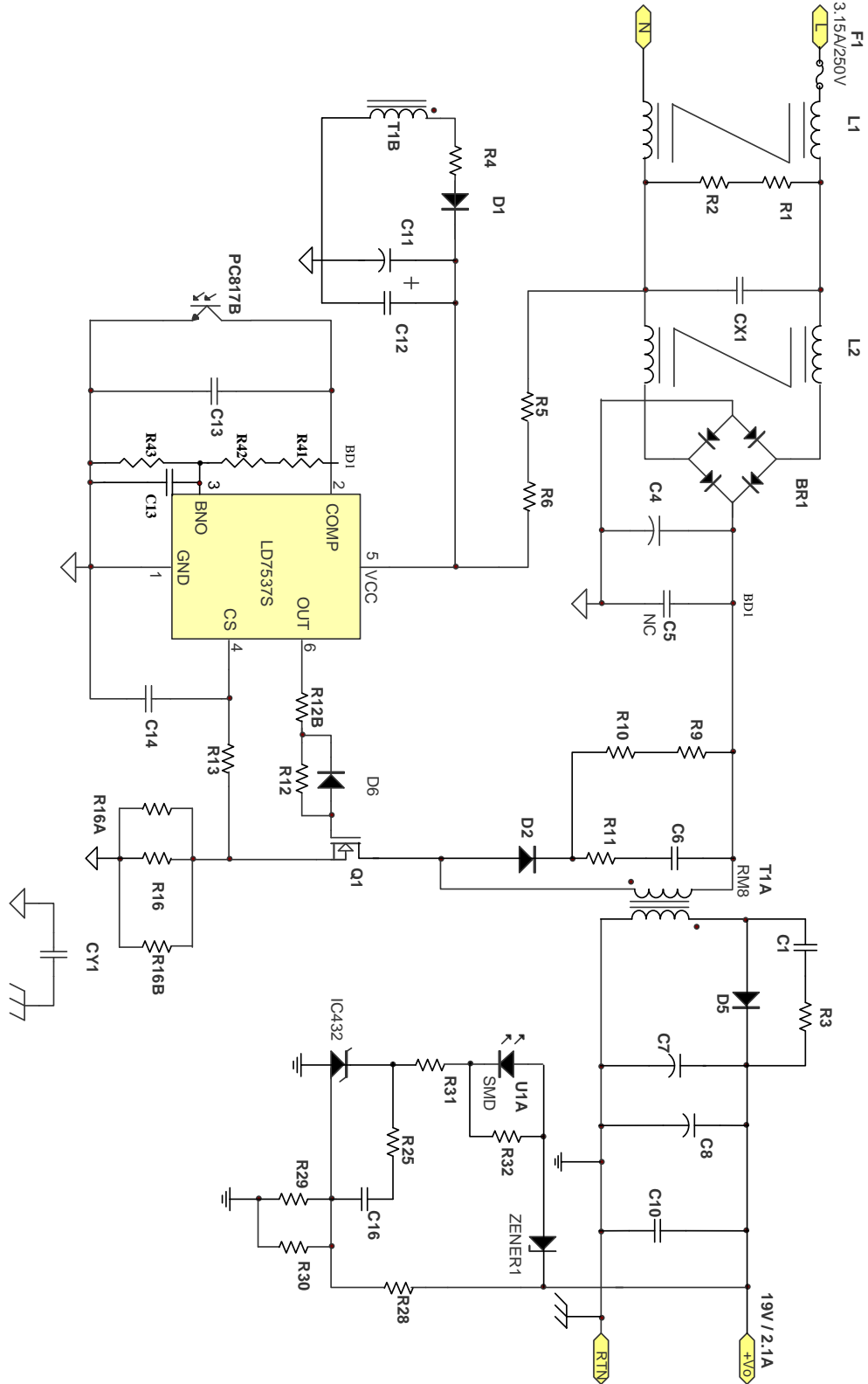
There are several critical protections integrated in the LD7537S to prevent from damage to the power supply.

Those damages usually come from open or short conditions on the pins of LD7537S.

In case under such conditions listed below, the gate output will turn off immediately to protect the power circuit.

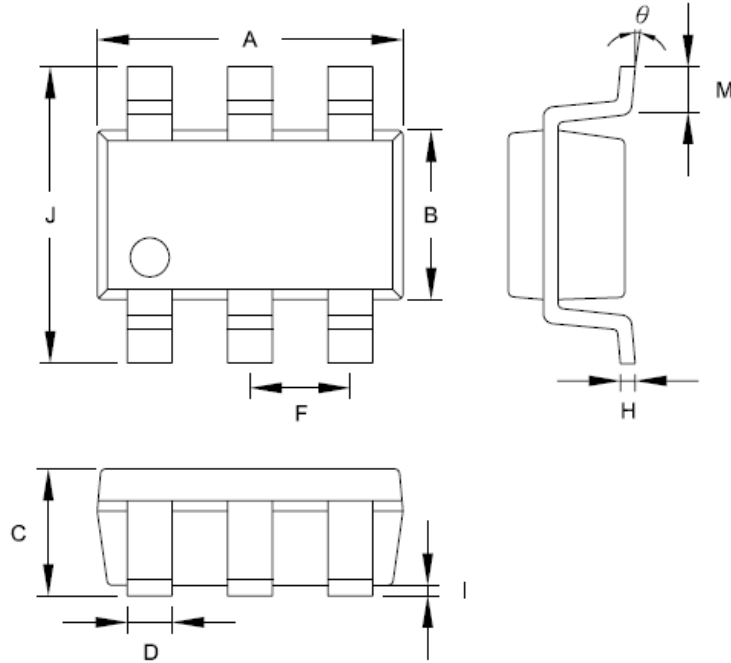
1. CS pin floating
2. COMP pin floating

## Reference Application Circuit --- 40W (19V/2.1A) Adapter



## Package Information

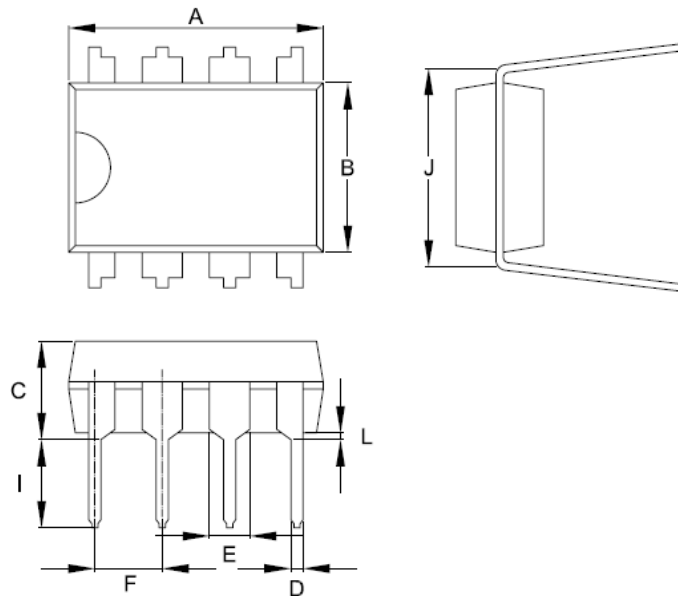
SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-----	1.450	-----	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

## Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	-----	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	-----	0.015	-----

### Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.



**Revision History**

Rev.	Date	Change Notice
00	04/03/2012	Original Specification