# Green-Mode PWM Controller with Frequency Trembling and Integrated Protections

***REV: 00***

## General Description

The LD7551C is built-in with several functions, protections and an EMI-improved solution in a SOT-26 package. It takes less components counts or circuit space, especially ideal for those cost sensitive applications.

The LD7551C integrates low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. It also features protections like OLP (Over Load Protection) and OVP (Over Voltage Protection) to prevent the circuit damage under the abnormal conditions.

Furthermore, the frequency trembling function is to reduce the noise level and help the power circuit designers for the EMI filter design with minimum component cost and developing time.

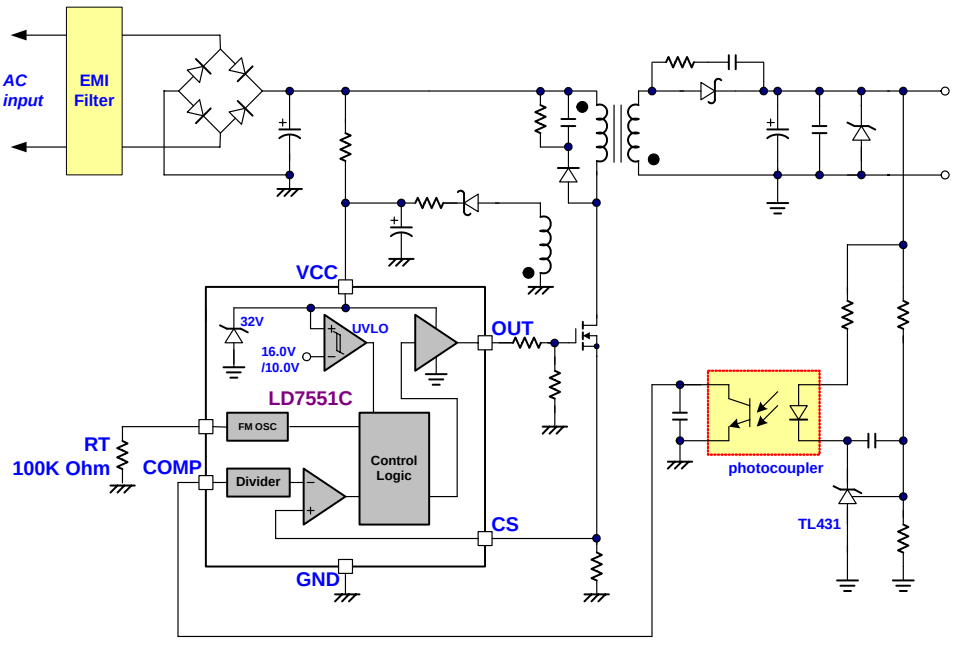
## Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (<20μA)
- Current Mode Control
- Non-audible-noise Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Programmable Switching Frequency
- Internal Trembling (±4KHz)
- Internal Slope Compensation
- OVP (Over Voltage Protection) on Vcc Pin
- OLP (Over Load Protection)
- 500mA Driving Capability

## Applications

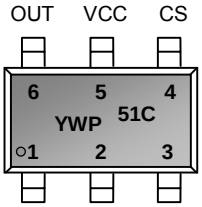
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

## Typical Application



## Pin Configuration

SOT-26 (TOP VIEW)




Y : Year code (F: 2006, G: 2007…..)
W : Week code
P : LD75.. (Product family code)

## Ordering Information

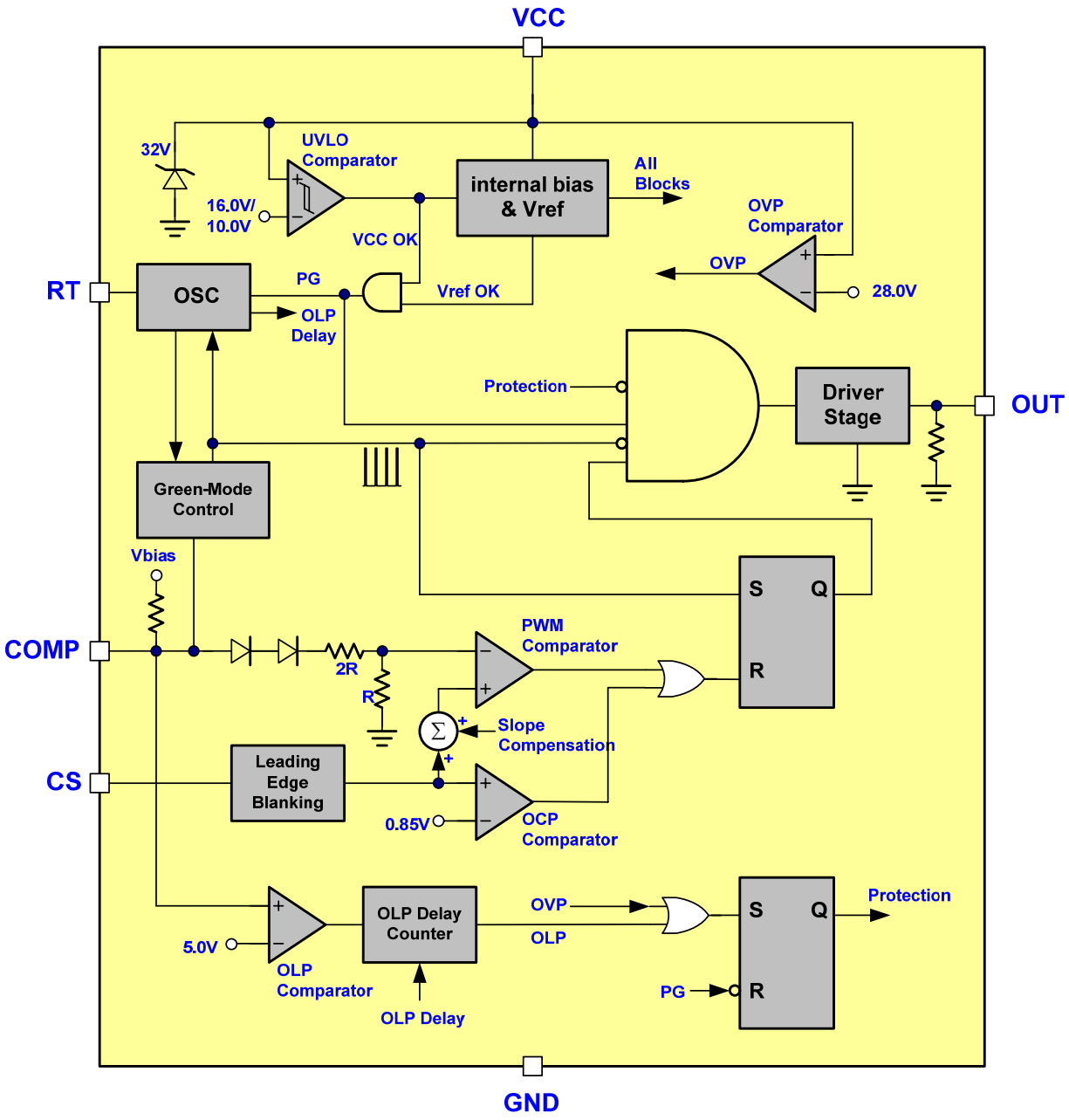
| Part number | Package | | TOP MARK | Shipping |
|---|---|---|---|---|
| LD7551C GL | SOT-26 | Green Package | YWP/51C | 3000 /tape & reel |

Note: The LD7551C is ROHS compliant.

## Pin Descriptions

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | COMP | Voltage feedback pin (same as the COMP pin in UC384X). Connecting it with a photo-coupler to close the control loop and achieve the regulation. |
| 3 | RT | This pin is to program the switching frequency. Connecting it with a resistor to ground can set the switching frequency. |
| 4 | CS | Current sense pin. Connect it to sense the MOSFET current |
| 5 | VCC | Supply voltage pin |
| 6 | OUT | Gate drive output to drive the external MOSFET |

## Block Diagram



## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage VCC | 30V |
| COMP, RT, CS | -0.3 ~7V |
| OUT | -0.3 ~Vcc+0.3 |
| Maximum Junction Temperature | 150°C |
| Operating Ambient Temperature | -40°C to 85°C |
| Operating Junction Temperature | -40°C to 125°C |
| Storage Temperature Range | -65°C to 150°C |
| Package Thermal Resistance (SOT-26) | 250°C/W |
| Power Dissipation (SOT-26, at Ambient Temperature = 85°C) | 250mW |
| Lead temperature (Soldering, 10sec) | 260°C |
| ESD Voltage Protection, Human Body Model | 3.0 KV |
| ESD Voltage Protection, Machine Model | 300 V |
| Gate Output Current | 500mA |

**Caution:**

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## Recommended Operating Conditions

| Item | Min. | Max. | Unit |
|---|---|---|---|
| Supply Voltage Vcc | 11 | 25 | V |
| RT Value | 50 | 130 | KΩ |
| Start-up resistor Value | 1.2 | 4.4 | MΩ |

## Electrical Characteristics

($T_A$ = +25°C unless otherwise stated, $V_{CC}$=15.0V)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Supply Voltage (Vcc Pin)** | | | | | |
| Startup Current | | | 12 | 20 | μA |
| Operating Current (with 1nF load on OUT pin) | $V_{COMP}$=0V | | 2.8 | 3.5 | mA |
| | $V_{COMP}$=3V | | 3.0 | | mA |
| | Protection tripped (OLP) | | 0.6 | | mA |
| | Protection tripped (OVP) | | 0.7 | | mA |
| UVLO (off) | | 9.0 | 10.0 | 11.0 | V |
| UVLO (on) | | 15.0 | 16.0 | 17.0 | V |
| OVP Level | | 26.8 | 28.0 | 29.2 | V |
| **Voltage Feedback (Comp Pin)** | | | | | |
| Short Circuit Current | $V_{COMP}$=0V | | 1.37 | 2.2 | mA |
| Open Loop Voltage | COMP pin open | | 5.9 | | V |
| Green Mode Threshold VCOMP | | | 2.35 | | V |
| **Current Sensing (CS Pin)** | | | | | |
| Maximum Input Voltage, Vcs(off) | | 0.80 | 0.85 | 0.90 | V |
| Leading Edge Blanking Time | | | 240 | | nS |
| Input impedance | | 1 | | | MΩ |
| Delay to Output | | | 100 | | nS |
| **Oscillator for Switching Frequency** | | | | | |
| Frequency | RT=100KΩ | 60 | 65 | 70 | KHz |
| Green Mode Frequency | Fs=65kHz | | 21 | | KHz |
| Trembling Frequency | | | ± 4.0 | | KHz |
| Temp. Stability | (-40°C ~105°C) | | | 5 | % |
| Voltage Stability | (VCC=11V-25V) | | | 1 | % |
| **Gate Drive Output (OUT Pin)** | | | | | |
| Output Low Level | VCC=15V, Io=20mA | | | 1 | V |
| Output High Level | VCC=15V, Io=20mA | 8 | | | V |
| Rising Time | Load Capacitance=1000pF | | 90 | 180 | nS |
| Falling Time | Load Capacitance=1000pF | | 30 | 60 | nS |
| **OLP (Over Load Protection)** | | | | | |
| OLP Trip Level | Vcomp (OLP) | | 5.0 | | V |
| OLP Delay Time | Fs=65kHz | | 50 | | mS |

** RT value is in proportion to OLP delay time.*

## Typical Performance Characteristics

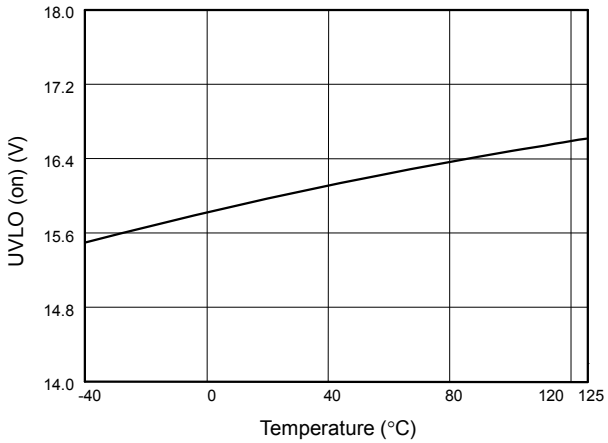



Fig. 1 UVLO (on) vs. Temperature

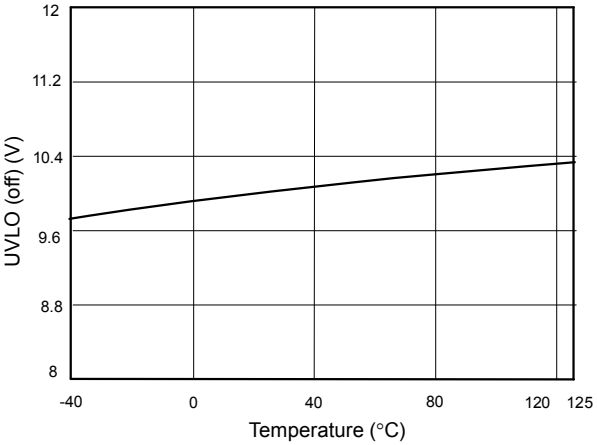



Fig. 2 UVLO (off ) vs. Temperature

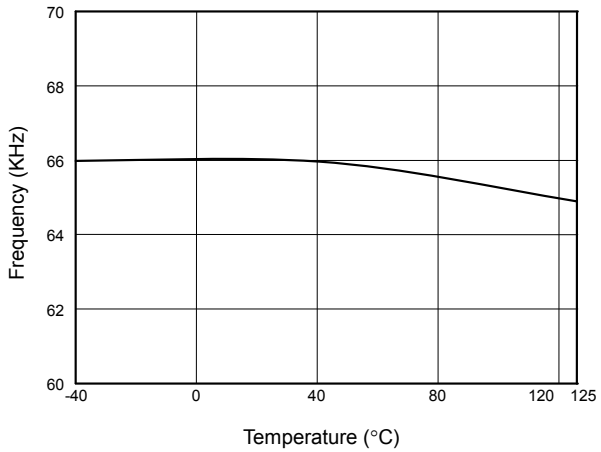



Fig. 3 Frequency vs. Temperature

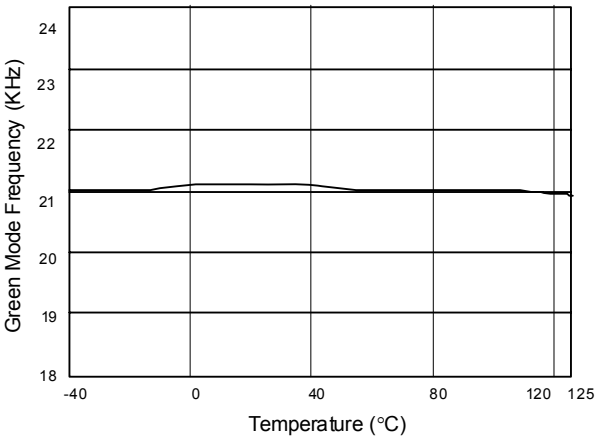



Fig. 4 Green Mode Frequency vs. Temperature

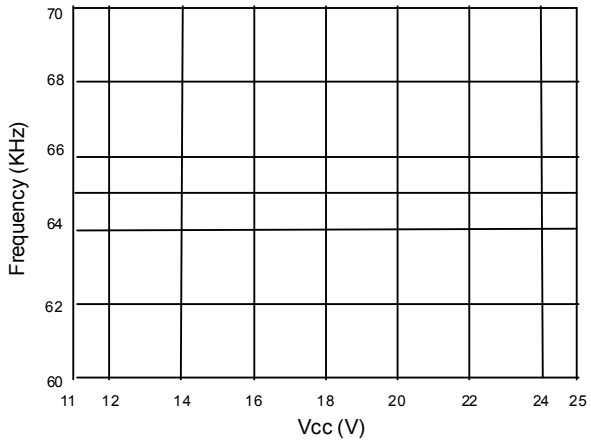



Fig. 5 Frequency vs. Vcc

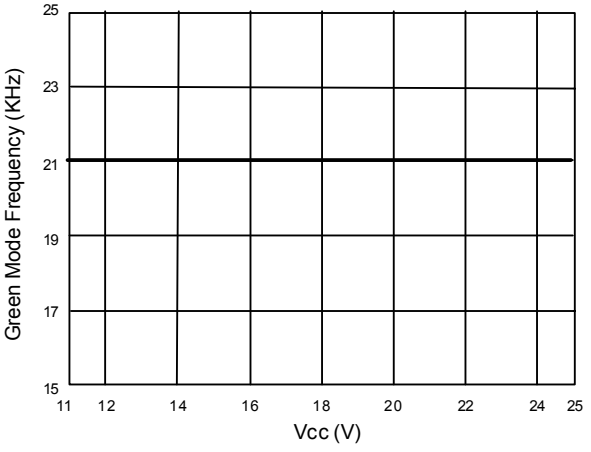



Fig. 6 Green Mode Frequency vs. Vcc

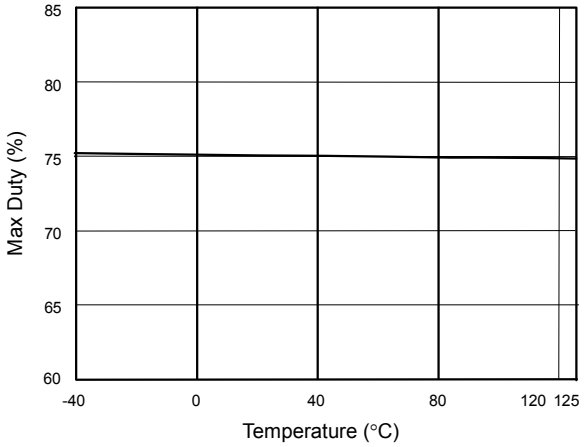



Fig. 7 Max Duty vs. Temperature

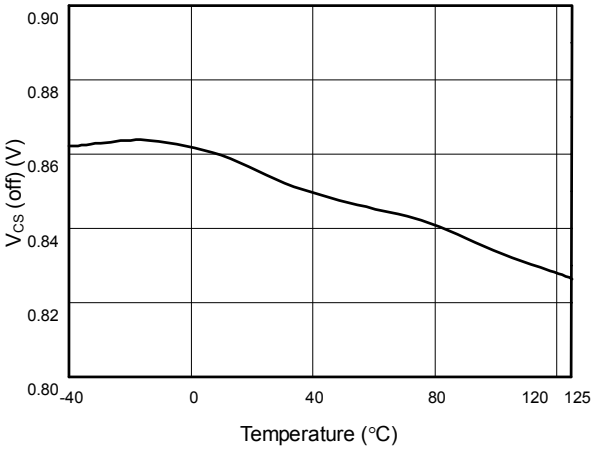



Fig. 8 $V_{CS}$ (off) vs. Temperature

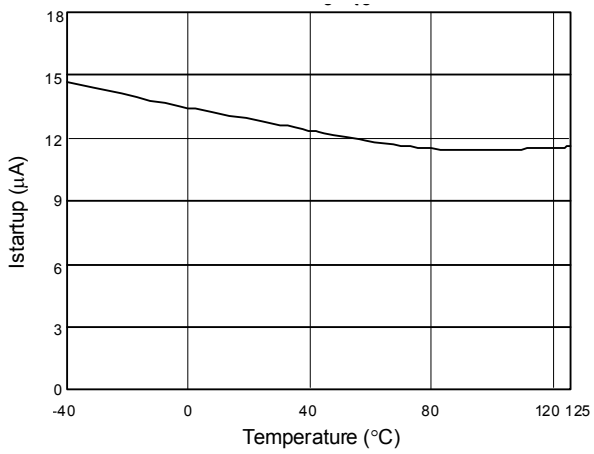



Fig. 9 Startup Current (Istartup) vs. Temperature

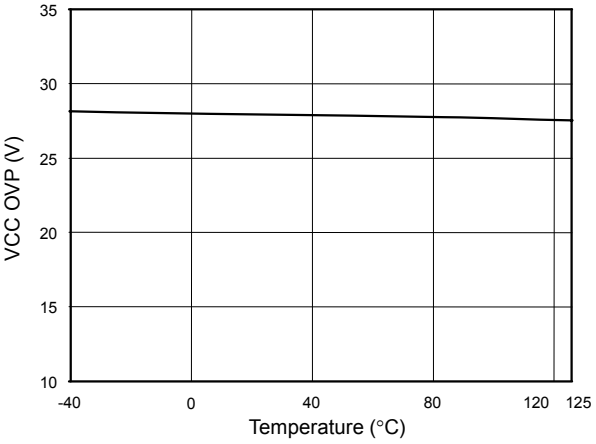



Fig. 10 VCC OVP vs. Temperature

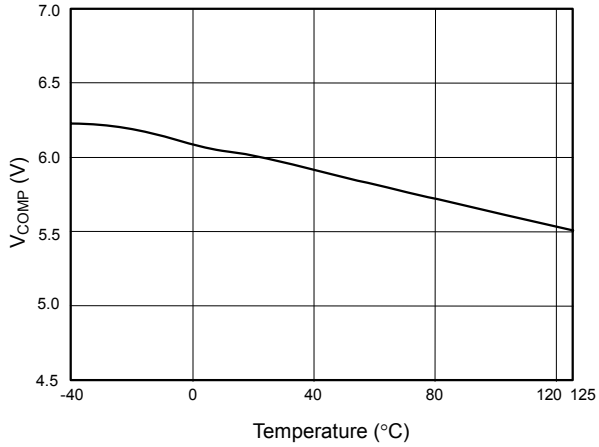



Fig. 11 $V_{COMP}$ open loop voltage vs. Temperature

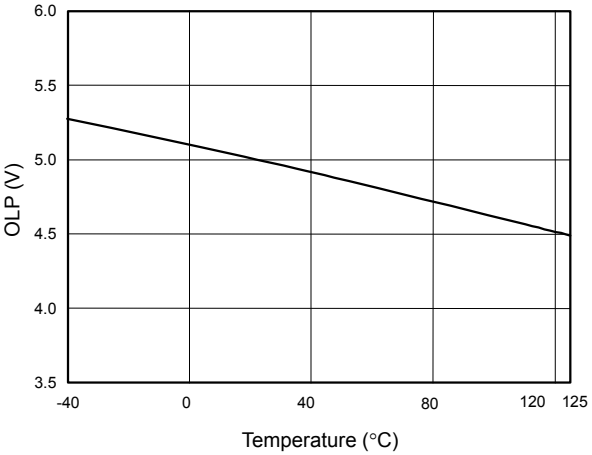



Fig. 12 OLP-Trip Level vs. Temperature

# Application Information

## Operation Overview

The LD7551C meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrates more functions with minimum external components counts and board size. Here following are the descriptions for it.

## Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD7551C PWM controller and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is built-in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.0V and 10.0V, respectively.

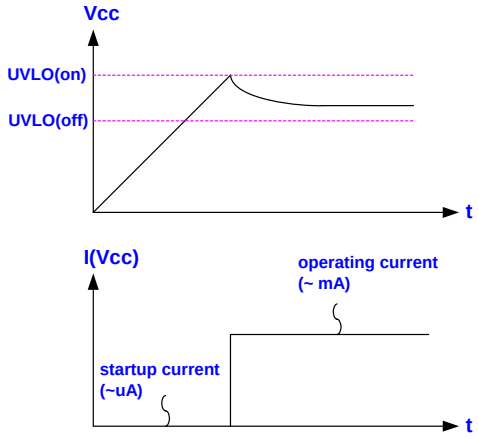



**Fig. 13**

## Startup Current and Startup Circuit

The typical startup circuit to generate the LD7551C Vcc is shown in Fig. 14. During the startup transient, the Vcc is lower than the UVLO threshold thus there is no gate pulse produced from LD7551C to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the Vcc voltage is high enough to turn on the LD7551C and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. Employing CMOS process with special circuit design, the maximum startup current of LD7551C is only 20μA.

If a higher resistance value of the R1 is chosen, it usually takes more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

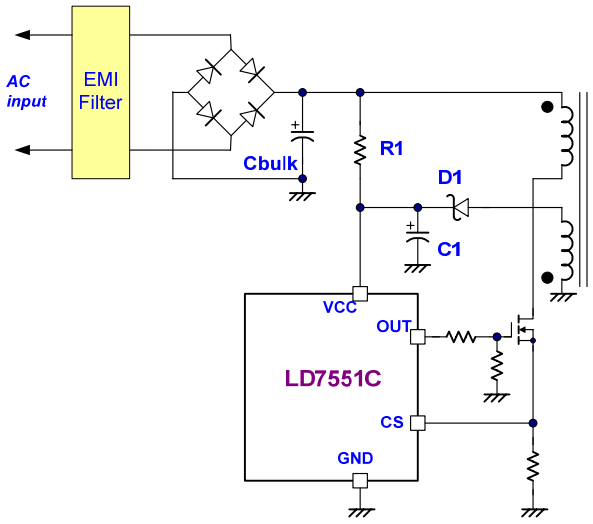



**Fig. 14**

## Current Sensing and Leading-Edge Blanking

The typical current mode of PWM controller feeds back both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 15, the LD7551C detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. Thus, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

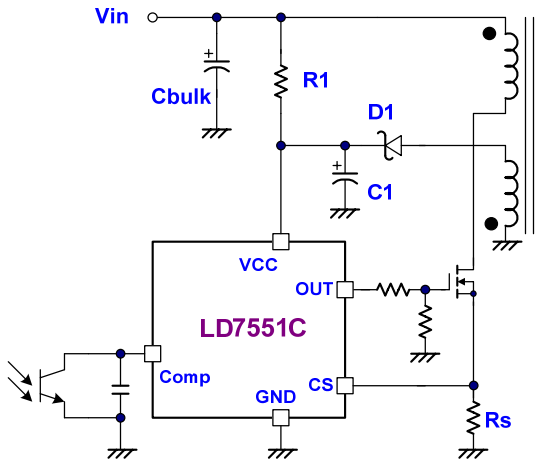



Fig. 15

A 240nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger caused by the current spike. In a low power application, if the total pulse width of the turn-on spikes is less than 240nS and the negative spike on the CS pin doesn't exceed -0.3V, the R-C filter as shown in the figure16 could be eliminated.

However, the total pulse width of the turn-on spike is decided by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter as shown in figure 17 for higher power applications to avoid the CS pin being damaged by the negative turn-on spike.

## Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7551C is limited to 75% to avoid the transformer saturation.

## Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD7551C. Similar to UC3842, the LD7551C would carry 2 diodes voltage offset at the stage before feeding the voltage feedback signal to the voltage divider at the ratio of 1/3, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally to eliminate the requirement of an external one.

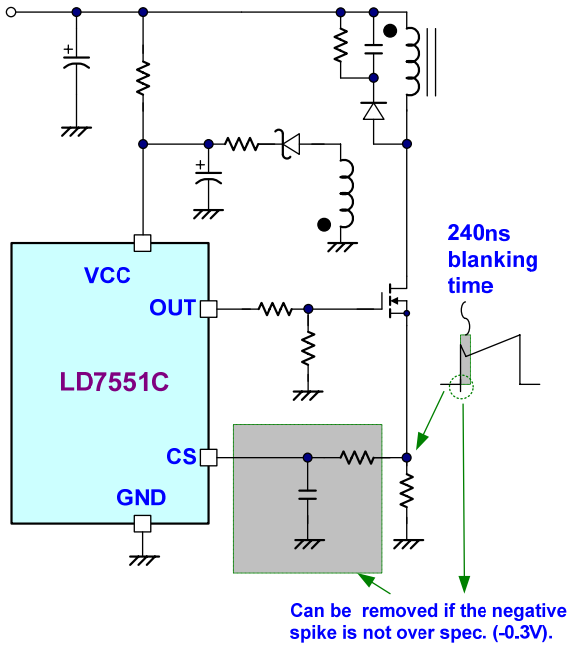



Fig. 16

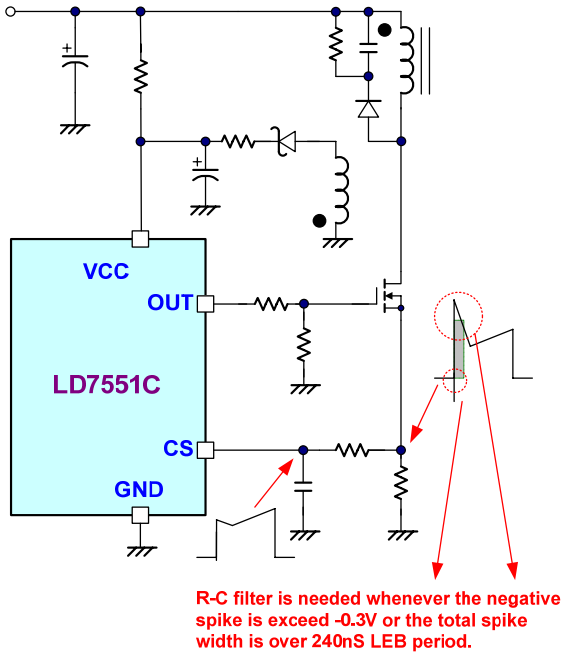



Fig. 17

## Oscillator and Switching Frequency

The switching frequency of LD7551C is programmed as an external resistor on RT to provide the optimized operations

considering the EMI performance, thermal treatment, component sizes and transformer design.

## Internal Slope Compensation

In conventional applications, the problem of the stability is a critical issue for current mode controlling, especially as it operates in the duty-cycle higher than 50%. As UC384X, LD7510C implements slope compensation by injecting the ramp signal of the RT/CT pin through a coupling capacitor. Slope compensation, as being integrated already, therefore requires no extra design for the LD7551C.

## On/Off Control

The LD7551C can be turned off by pulling COMP pin below 1.2V. The gate output pin of the LD7551C will be disabled immediately under such condition. To remove the pull-low signal can release the off-mode.

## Dual-Oscillator Green-Mode Operation

There are many different topologies has been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intends to reduce the switching cycles under light-load or no-load conditions either by skipping some switching pulses or reducing the switching frequency.

By using this dual-oscillator control, the green-mode frequency can be well controlled to further avoid the generation of audible noise.

## OVP (Over Voltage Protection) on Vcc

The $V_{GS}$ ratings of the nowadays power MOSFETs are often limited for up to max. 30V. To prevent the $V_{GS}$ from fault condition, LD7551C is implemented with an OVP function on Vcc. If the Vcc voltage increase above OVP threshold voltage, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(on).

The LD7551C features auto-recovery type of protection for Vcc OVP function. If the OVP condition is not released, which is usually caused by the feedback loop open, the Vcc will trip the OVP level again and re-shutdown the output. The Vcc will then work in hiccup mode. The Figure 18 shows its operation.

On the other hand, if the OVP condition is removed, the Vcc level will resume to normal level and the output to normal operation.

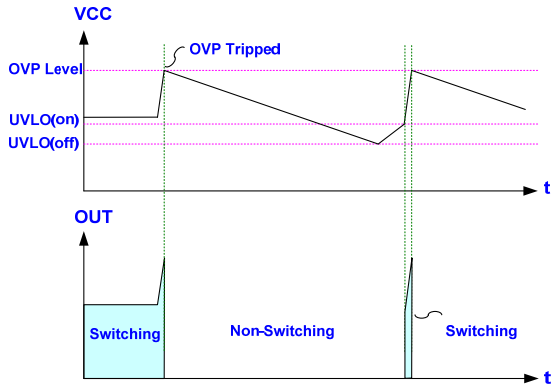



**Fig. 18**

## Over Load Protection (OLP)

To protect circuits from being damaged under over load condition or short condition, a smart OLP function is implemented in the LD7551C. The Figure 19 shows the waveforms of the OLP operation. In this case, the feedback system will force the voltage loop proceeding toward the saturation and then pull up the voltage on COMP pin ($V_{COMP}$). Whenever the $V_{COMP}$ trips up to the OLP threshold 5V and stays longer than the OLP delay time, the protection will be activated to turn off the gate output and stop the switching of power circuit. The OLP delay time is to prevent any false trigger caused by the power-on and turn-off transient. The Higher the CT value, the longer the OLP delay time. By such protection mechanism, the average input power can be reduced to a very low level so that the component temperature and stress can be controlled within the safe operating area.

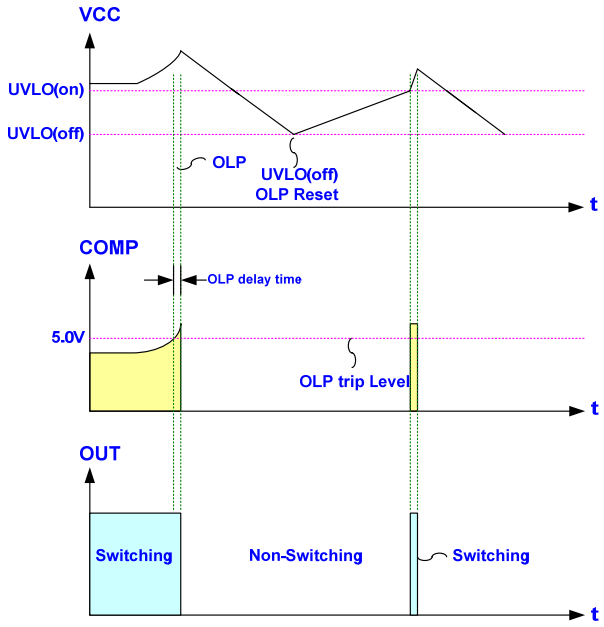



Fig. 19

## Fault Protection

There are several critical protections integrated in the LD7551C to prevent the power supply or adapter from being damaged. Those damages usually come from open or short condition on the pins of LD7551C.

Under the conditions listed below, the gate output will turn off immediately to protect the power circuit ---

1. RT pin short to ground
2. RT pin floating
3. CS pin floating

## Reference Application Circuit --- 50W (12V/4.2A) Adapter

### Schematic

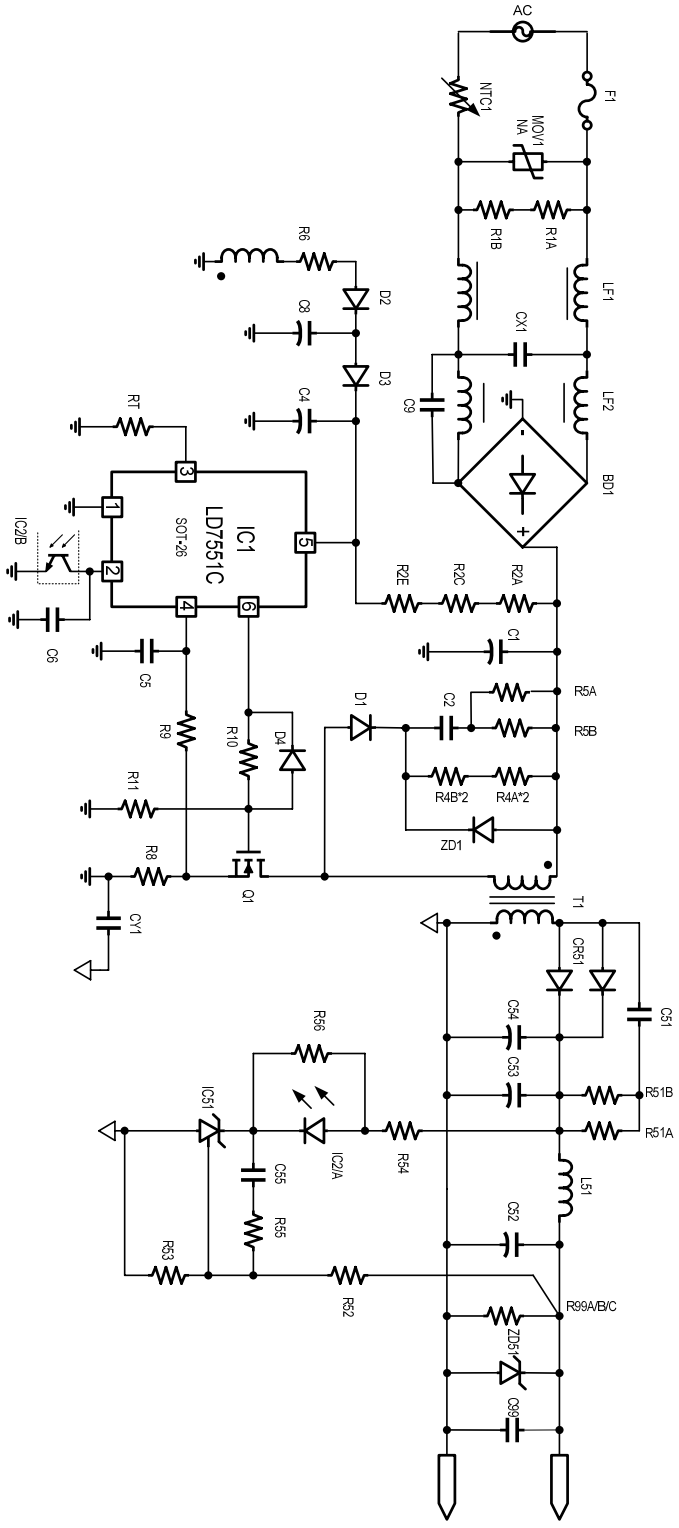



Fig. 20

## Reference Application Circuit --- 50W (12V/4.2A) Adapter

**BOM**

| P/N | Component Value | Note |
|---|---|---|
| R1A | 1MΩ, 1206, 1% | |
| R1B | 1MΩ, 1206, 1% | |
| R2A | 1MΩ, 1206, 1% | |
| R2C | 1MΩ, 1206, 1% | |
| R2E | 1MΩ, 1206, 1% | |
| R4A/1 | 100KΩ, 1206, 1% | |
| R4A/2 | 100KΩ, 1206, 1% | |
| R4B/1 | 100KΩ, 1206, 1% | |
| R4B/2 | 100KΩ, 1206, 1% | |
| R5A | 22Ω, 1206, 1% | |
| R5B | 22Ω, 1206, 1% | |
| R6 | 0Ω, 1206, 5% | |
| R8 | 0.43Ω, 2WS | |
| R9 | 200Ω, 0805, 1% | |
| R10 | 15Ω, 1206, 1% | |
| R11 | 20KΩ, 1206, 1% | |
| RT | 100KΩ, 0805, 1% | |
| R51A | 75Ω, 1206, 1% | |
| R51B | 75Ω, 1206, 1% | |
| R52 | 9.53KΩ, 0805, 1% | |
| R53 | 2.49KΩ, 0805, 1% | |
| R54 | 510Ω, 0805, 1% | |
| R55 | 3KΩ, 0805, 1% | |
| R56 | NA | |
| R99A | 10KΩ, 1206, 1% | |
| R99B | NA | |
| R99C | NA | |
| NTC1 | 3A, 5Ω | |
| LF1 | Leadtrend's Design | |
| LF2 | Leadtrend's Design | |
| T1 | Leadtrend's Design | |
| L51 | Leadtrend's Design | |

| P/N | Component Value | Note |
|---|---|---|
| C1 | 100μF, 400V | TY |
| C2 | 1000pF, 1000V, 1206 | |
| C4 | 3.3μF, 50V | LZG |
| C5 | 220pF, 50V, 0805 | |
| C6 | 3.3nF, 50V, 0805 | |
| C8 | 10μF, 50V | LZG |
| C9 | NA | |
| C51 | 1000pF, 1000V, 1206 | |
| C52 | 220μF, 25V | LZG |
| C53 | 1500μF, 16V | LZG |
| C54 | 1500μF, 16V | LZG |
| C55 | 10nF, 50V, 0805 | |
| C99 | NA | |
| CX1 | 0.33μF, X-cap | |
| CY1 | 2200pF,Y-cap, class1 | |
| D1 | 1N4007 | |
| D2 | PS1010R | |
| D3 | 1N4148, | |
| D4 | 1N4148 | |
| Q1 | 8A, 600V | |
| BD1 | 2A, 600V | |
| CR51 | 10A, 100V | |
| ZD1 | NA | |
| ZD51 | NA | |
| IC1 | LD7551C GL | Leadtrend |
| IC2 | EL817B | |
| IC51 | KA431, 1% | |
| F1 | 250V, T2A | Walter |
| MOV1 | NA | |

## Reference Application Circuit #2 --- 10W Adapter with 2-Stage Startup Circuit

***Pin < 0.25W when Pout = 0W***

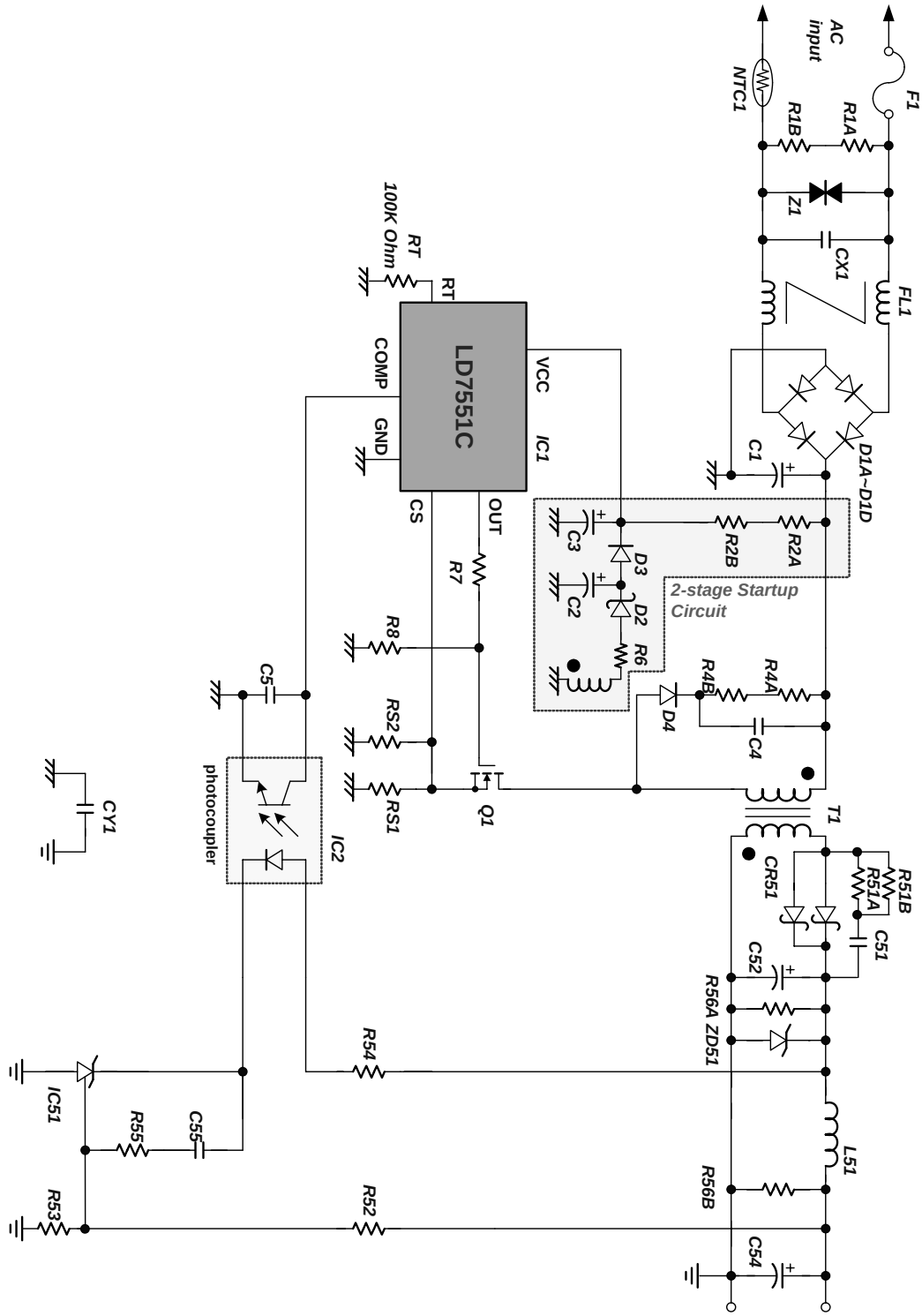



Fig. 21

## Reference Application Circuit #2 --- 10W Adapter with 2-Stage Startup Circuit

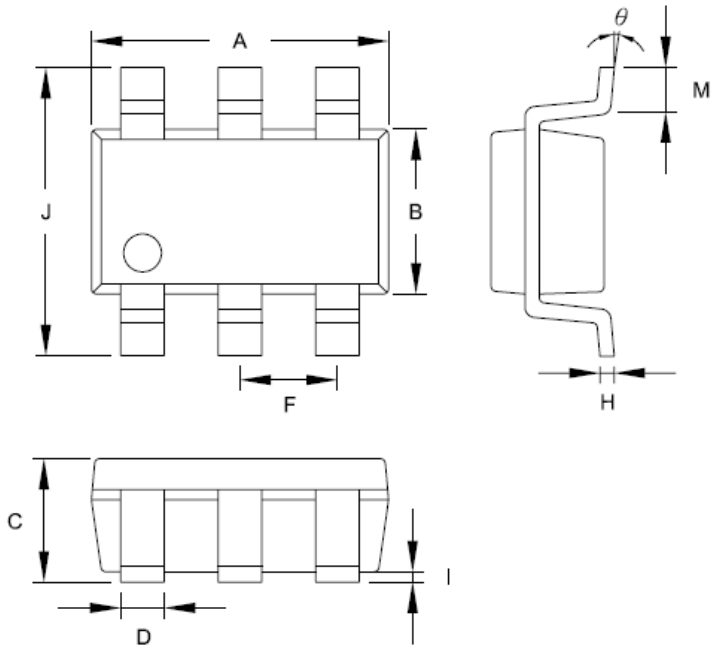
**BOM**

| P/N | Component Value | Original |
|---|---|---|
| R1A | N/A | |
| R1B | N/A | |
| R2A | 2.2MΩ, 1206 | |
| R2B | 2.2MΩ, 1206 | |
| R4A | 39KΩ, 1206 | |
| R4B | 39KΩ, 1206 | |
| R6 | 2.2Ω, 1206 | |
| R7 | 10Ω, 1206 | |
| R8 | 10KΩ, 1206 | |
| RS1 | 2.70Ω, 1206, 1% | |
| RS2 | 2.70Ω, 1206, 1% | |
| R51A | 100Ω, 1206 | |
| R51B | 100Ω, 1206 | |
| R52 | 2.49KΩ, 0805, 1% | |
| R53 | 2.49KΩ, 0805, 1% | |
| R54 | 220Ω, 0805 | |
| R55 | 10KΩ, 0805 | |
| R56A | 1KΩ, 1206 | |
| R56B | N/A | |
| NTC1 | 5Ω, 3A | 08SP005 |
| FL1 | 20mH | UU9.8 |
| T1 | EI-22 | |
| L51 | 2.7μH | |

| P/N | Component Value | Note |
|---|---|---|
| C1 | 22μF, 400V | L-tec |
| C2 | 10μF, 50V | L-tec |
| C3 | 2.2μF, 50V | |
| C4 | 1000pF, 1000V, 1206 | Holystone |
| C5 | 0.01μF, 16V, 0805 | |
| C51 | 1000pF, 50V, 0805 | |
| C52 | 1000μF, 10V | L-tec |
| C54 | 470μF, 10V | L-tec |
| C55 | 0.01μF, 16V, 0805 | |
| RT | 100kΩ, 0805, 1% | |
| CX1 | 0.1μF | X-cap |
| CY1 | 2200pF | Y-cap |
| D1A | 1N4007 | |
| D1B | 1N4007 | |
| D1C | 1N4007 | |
| D1D | 1N4007 | |
| D2 | PS102R | |
| D3 | 1N4148 | |
| D4 | 1N4007 | |
| Q1 | 2N60B | 600V/2A |
| CR51 | SB540 | |
| ZD51 | 6V2C | |
| IC1 | LD7551C GL | SOT-26 |
| IC2 | EL817B | |
| IC51 | TL431 | 1% |
| F1 | 250V, 1A | |
| Z1 | N/A | |

## Package Information

**SOT-26**




| Symbol | Dimension in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 2.692 | 3.099 | 0.106 | 0.122 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| C | x | 1.450 | x | 0.057 |
| D | 0.300 | 0.550 | 0.012 | 0.022 |
| F | 0.838 | 1.041 | 0.033 | 0.041 |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| I | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 2.600 | 3.000 | 0.102 | 0.118 |
| M | 0.300 | 0.600 | 0.012 | 0.024 |
| θ | 0° | 10° | 0° | 10° |

### Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

## Revision History

| Rev. | Date | Change Notice |
|---|---|---|
| 00 | 4/17/2009 | Original specification. |