High Voltage Green-Mode PWM Controller with Shut Down Function

Rev. 00

General Description

The LD7560 integrated several functions of protections, and EMI-improved solution in a SOP-8/or DIP-8 package. It can minimize the component counts and the circuit space, and it's perfect for the low cost of applications.

It provides functions of low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. Also, the LD7560 features more protections like OLP (Over Load Protection), and OVP (Over Voltage Protection), to prevent the circuit being damaged from the abnormal conditions.

Furthermore, the LD7560 features shut down function to minimize the power loss when the LD7560's SD pin pulled low In order to decrease standby power loss (<0.1W) for monitor application.

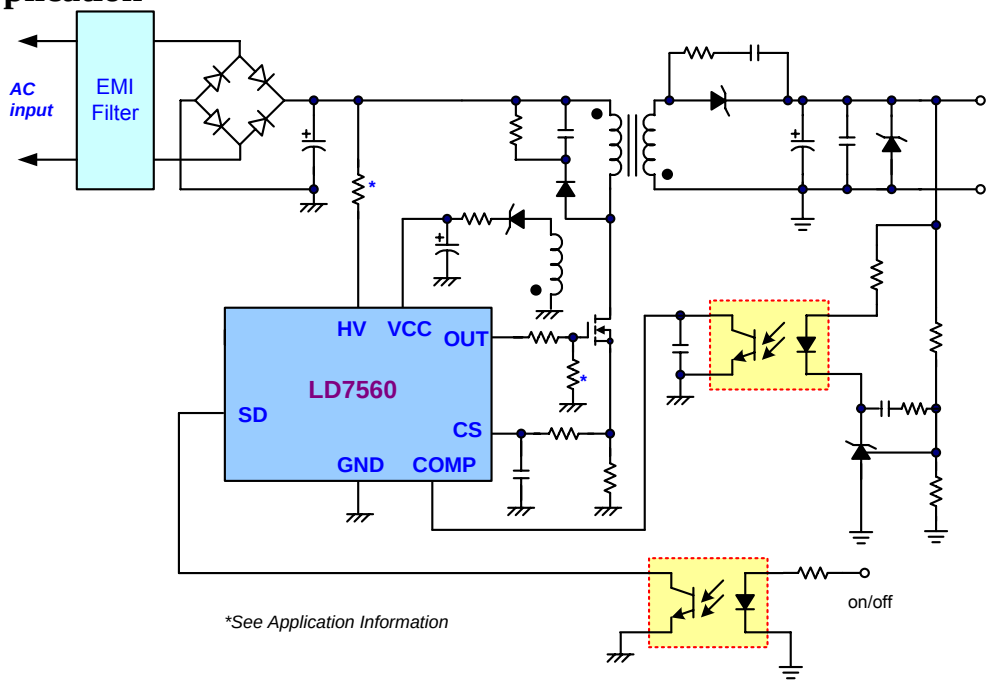
Features

- High-Voltage (500V) Startup Circuit
- Current Mode Control
- Non-Audible-Noise Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Trembling (±4KHz)
- Internal Slope Compensation
- Internal Over Current Protection
- OVP (Over Voltage Protection) on Vcc
- OLP (Over Load Protection)
- Internal OCP Compensation
- Shut Down Function through a Photo Coupler
- Two Step LEB for Light Load Efficiency
- 500mA Driving Capability

Applications

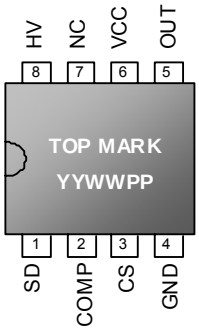
- Switching AC/DC Adaptor
- LIPS for LCD Monitor/TV Power

Typical Application



Pin Configuration

SOP-8 & DIP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

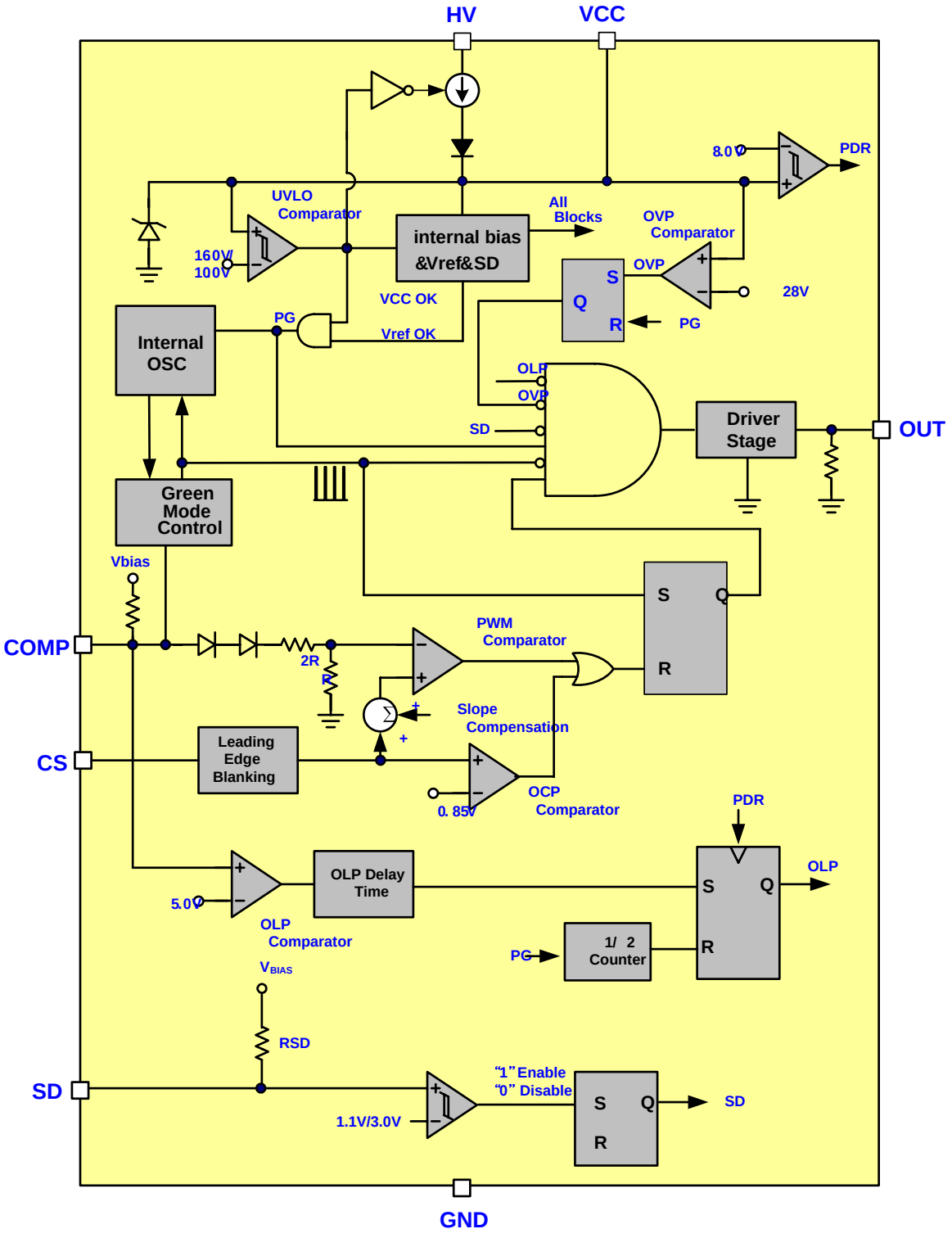
Part number	OVP/OLP	Package	Top Mark	Shipping
LD7560GS	Auto-recover	SOP-8	LD7560GS	2500 /tape & reel
LD7560GN	Auto-recover	DIP-8	LD7560GN	3600 /tube /Carton

The LD7560 is ROHS compliance.

Pin Descriptions

PIN	NAME	FUNCTION
1	SD	Pulling this pin below 1.1V will shutdown the controller to stop OUT pin until the SD pin rises above 3.0V. Keep this pin floating or pulling SD pin high to enable the control chip. A 250μS de-bounce time is built in SD pin to avoid false trigging.
2	COMP	Voltage feedback pin (same as the COMP pin of UC384X). Connecting a photo-coupler to close the control loop will achieve the regulation.
3	CS	Current sense pin. Connect it to sense the MOSFET current
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Supply voltage pin
7	NC	Unconnected Pin
8	HV	Connect this pin to positive terminal of the bulk capacitor to provide the startup current for the controller. When Vcc voltage trips the UVLO(on), this HV loop will be disabled to eliminate the power loss through the startup circuit.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	30V
High-Voltage Pin, HV	-0.3V~600V
COMP,SD, CS	-0.3 ~7V
OUT	-0.3 ~Vcc+0.3
Maximum Junction Temperature	150°C
Operating Ambient Temperature Range	-40°C to 85°C
Operating Junction Temperature Range	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8)	160°C/W
Package Thermal Resistance (DIP-8)	100°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	400mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV Pin)	2.5KV
ESD Voltage Protection, Machine Model	250V
Gate Output Current	500mA

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)					
High-Voltage Current Source	HV=500V	0.5	1	1.5	mA
Off-State Leakage Current	HV=500V	-	8	35	μA
Supply Voltage (VCC Pin)					
Startup Current		-	300	-	μA
Operating Current with 1nF load on OUT pin	V_{COMP}=0V	-	3.3	3.8	mA
	V_{COMP}=3V	-	3.6	4.2	mA
	OLP Protection	-	0.7	-	mA
	OVP Protection	-	0.7	-	mA
	SD<1.1V	-	70	-	μA
UVLO (off)		9.0	10.0	11.0	V
UVLO (on)		15.0	16.0	17.0	V
OVP Level		26.5	28	29.5	V
Voltage Feedback (COMP Pin)					
Short Circuit Current	V_{COMP}=0V	-	1.5	-	mA
Open Loop Voltage	COMP pin open	-	5.8	-	V
Green Mode Threshold VCOMP		-	2.35	-	V
Burst Mode Threshold VCOMP		-	1.4	-	V
Current Sensing (CS Pin)					
Max. Input Voltage,Vcs_off		0.80	0.85	0.90	V
Max. Input Voltage,Vcs_min		-	0.73	-	V
Leading Edge Blanking Time	Vcomp>1.9V	-	250	-	nS
Leading Edge Blanking Time	Vcomp<1.9V	-	750	-	nS
Input impedance		1	-	-	MΩ
Delay to Output		-	100	-	nS

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency					
Frequency		61	65	69	KHz
Green Mode Frequency		-	22	-	KHz
Trembling Frequency	V_{COMP}>2.35V	-	±4	-	KHz
	V_{COMP}<1.85V	-	±2.5	-	KHz
Modulation Frequency		-	100	-	Hz
Temp. Stability	(-20°C ~125°C)	-	4	-	%
Voltage Stability	VCC=11V to 25V	-	1	-	%
Shut Down Protection (SD Pin)					
SD Pin Source Current		8	-	16	μA
Enable Trip Level		3.0	-	-	V
Shut Down Trip Level		-	-	1.1	V
SD Pin Floating		5	-	-	V
SD pin de-bounce time		-	250	-	μS
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA	-	-	1	V
Output High Level	VCC=15V, Io=20mA	9	-	-	V
Rising Time	Load Capacitance=1000pF	-	100	160	nS
Falling Time	Load Capacitance=1000pF	-	30	60	nS
OLP (Over Load Protection)					
OLP Trip Level		-	5.0	-	V
OLP Delay Time		-	60	-	mS

Typical Performance Characteristics

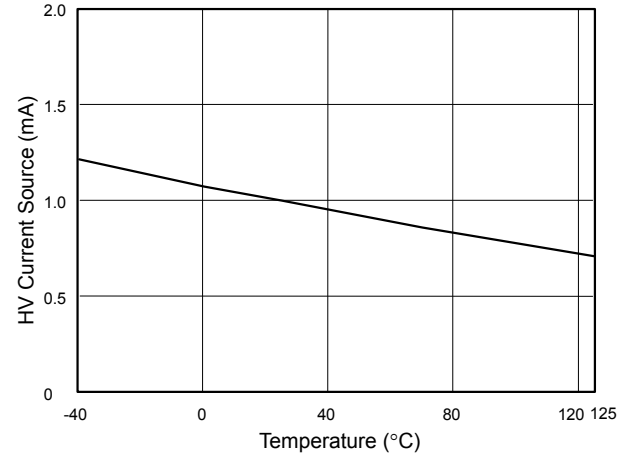


Fig. 1 HV Current Source vs. Temperature (HV=500V, Vcc=0V)

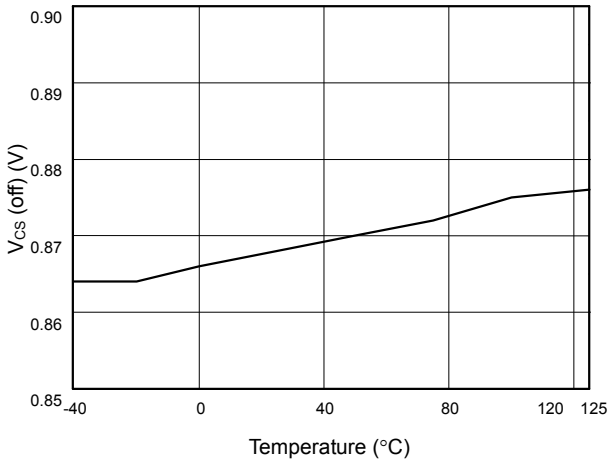


Fig. 2 V_{CS} (off) vs. Temperature

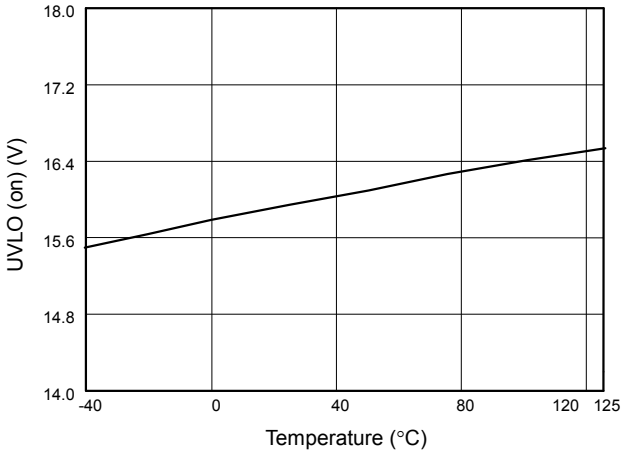


Fig. 3 UVLO (on) vs. Temperature

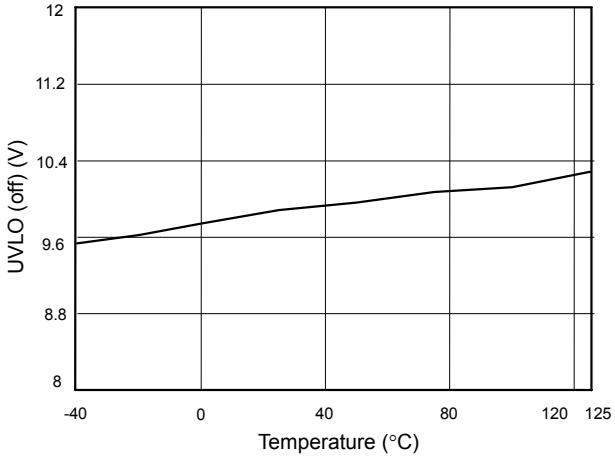


Fig. 4 UVLO (off) vs. Temperature

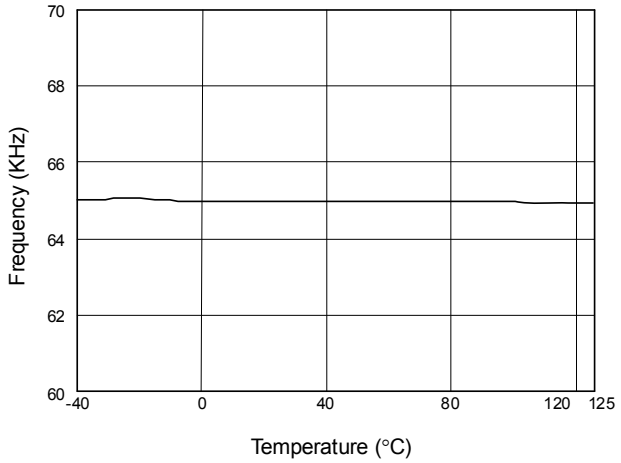


Fig. 5 Frequency vs. Temperature

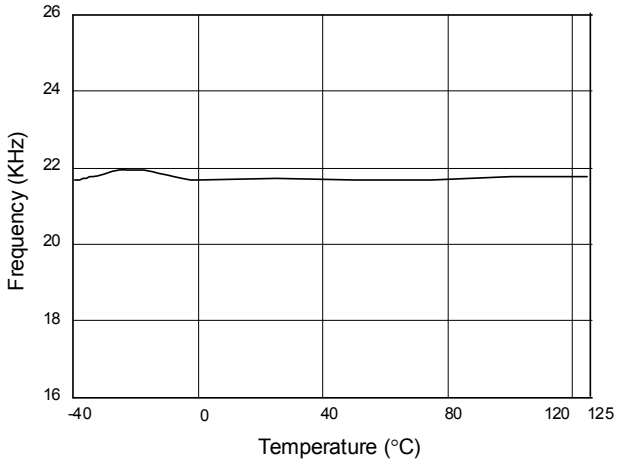


Fig. 6 Green Mode Frequency vs. Temperature

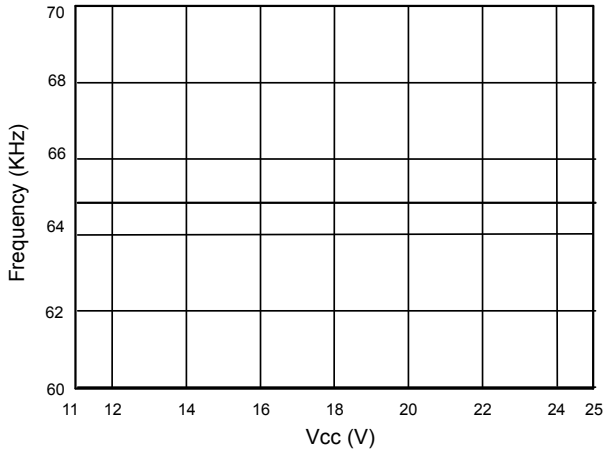


Fig. 7 Frequency vs. Vcc

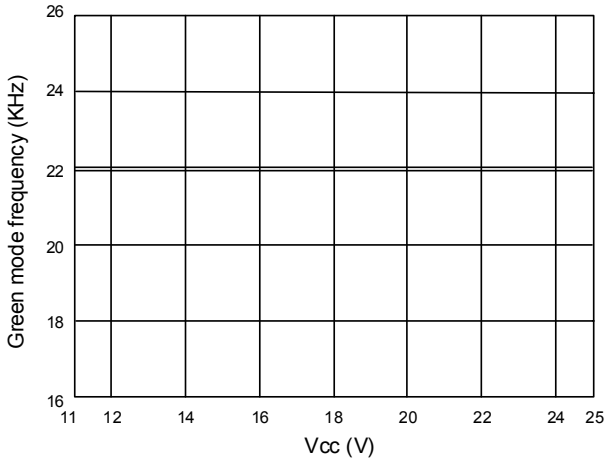


Fig. 8 Green mode frequency vs. Vcc

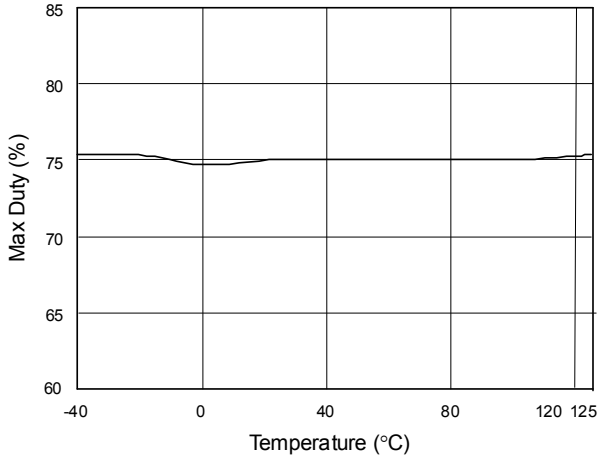


Fig. 9 Max Duty vs. Temperature

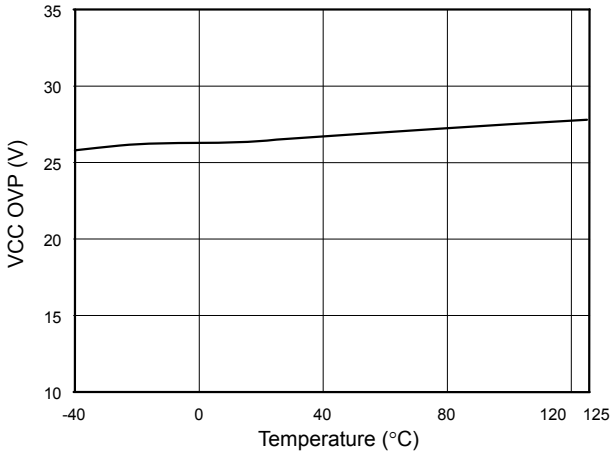


Fig. 10 VCC OVP vs. Temperature

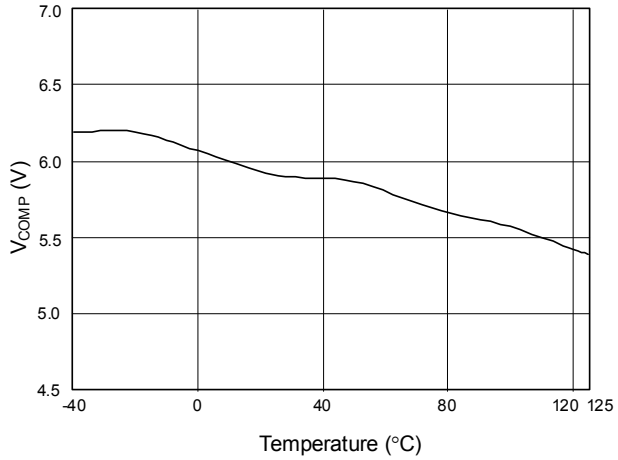


Fig. 11 V_{COMP} open loop voltage vs. Temperature

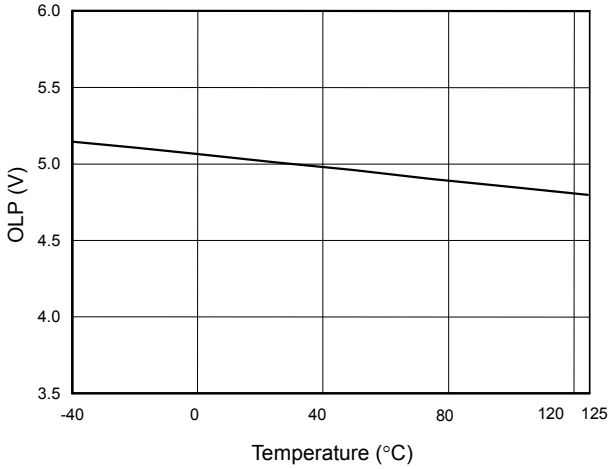


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is becoming more and more important for switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation forces the PWM controllers to powerfully integrate more functions, thereby reducing the external part count. The LD7560 is ideal for these applications to provide an easy and cost effective solution; and its detailed features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

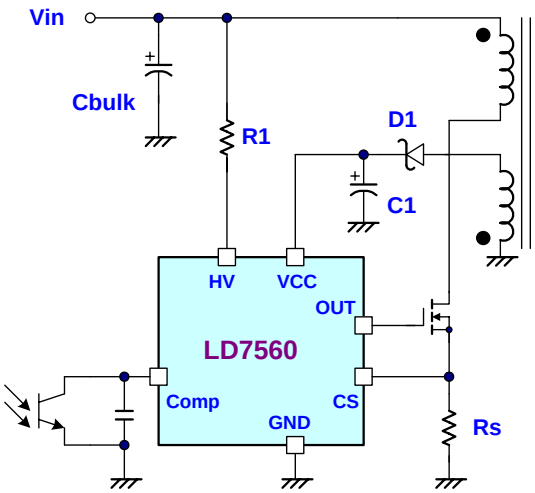


Fig. 13

Traditional circuits' power on the PWM controller through a startup resistor to constantly provide current from a rectified voltage to the capacitor connected to Vcc pin. Nevertheless, this startup resistor was usually of larger resistance, and it therefore required more power and longer time to start up.

To achieve the optimized topology, as shown in figure 13, LD7560 is built in with high voltage startup circuit to optimize the power saving. During startup, a high-voltage current source sinks current from the bulk capacitor to provide the startup current as well as to charge the Vcc capacitor C1. During the initialization of the startup, Vcc voltage is lower than the UVLO(off) threshold thus the current source is on to supply a current of 6mA current. Meanwhile, the Vcc supply current is as low as 300μA such that most of the HV current is adopted to charge the Vcc capacitor. By using such configuration, the turn-on delay time will be almost the same no matter under low-line or high-line condition.

As the Vcc voltage reaches UVLO(on) to power on the LD7560 and further to deliver the gate drive signal, the high-voltage current source is disabled and the supply current is solely provided from the auxiliary winding of the transformer. Therefore, it eliminates the power loss on the startup circuit and performs highly power saving.

An UVLO comparator is embedded to detect the voltage on the Vcc pin and to ensure the supply voltage high enough to power on the LD7560 PWM controller and to drive the power MOSFET. As shown in Fig. 14, a hysteresis is provided to prevent undesired shutdown from the voltage dip during startup. The turn-on and turn-off threshold levels are set at 16V and 10.0V, respectively.

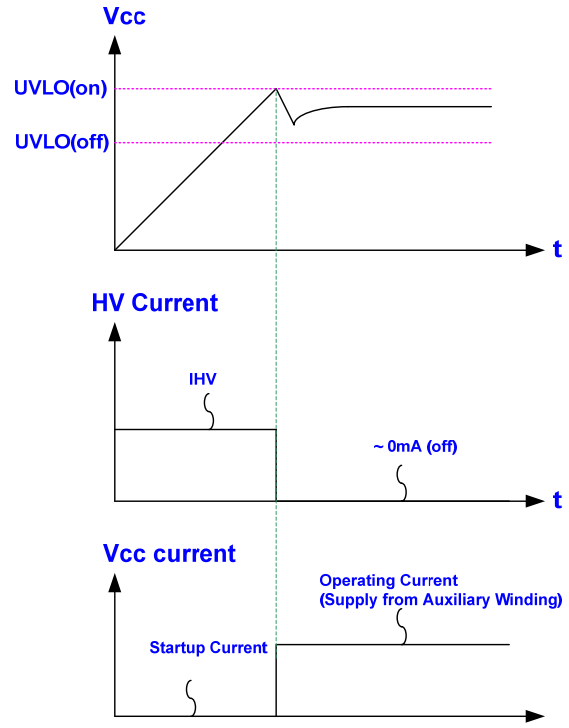


Fig. 14

Current Sensing, Leading-edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feeds back both current signal and voltage signal to close the control loop and achieve regulation. The LD7560 detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A 250nS leading-edge blanking (LEB) time is incorporated in the input of CS pin to prevent the false-trigger caused by any current spike. In low power applications, if the total pulse width of the turn-on spikes is less than 250nS and the negative spike on the CS pin does not exceed -0.3V, the R-C filter (as shown in figure15) can be eliminated.

However, the total pulse width of the turn-on spike is related to output power, circuit design and PCB layout. It is strongly recommended to add a small R-C filter (as shown in figure 16) for higher power applications to avoid the CS pin from being damaged by the negative turn-on spike.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7560 is 75% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 in the secondary side through the photo-coupler to the COMP pin of LD7560. The input stage of LD7560, like the UC384X, is incorporated with 2 diodes voltage offset circuit to feed the voltage divider with 1/3 ratio, that is

$$V_{+(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally. Therefore no extra resistor is required in the external circuit.

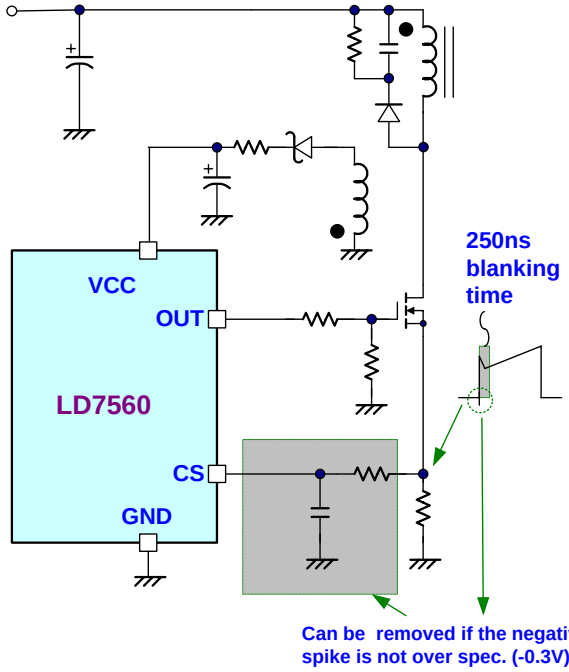


Fig. 15

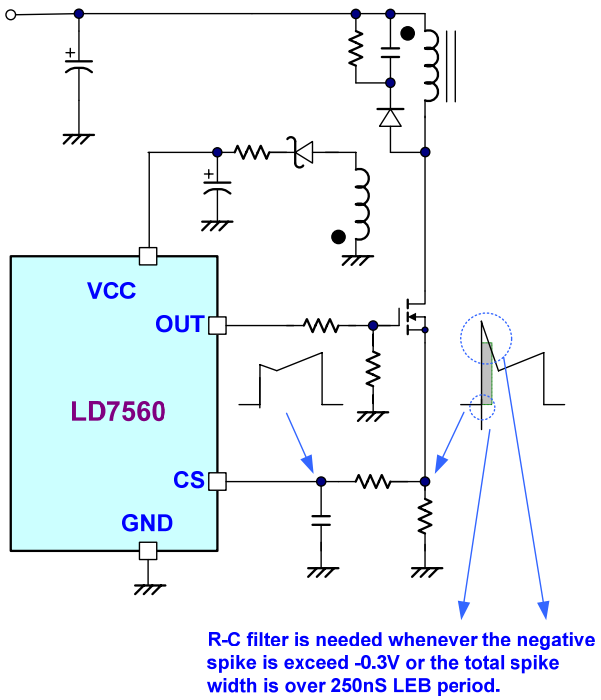


Fig. 16

Oscillator and Switching Frequency

The switching frequency of LD7560 is fixed at 65KHz internally to provide the optimized operations in consideration of the EMI performance, thermal treatment, component sizes and transformer design.

Frequency Trembling

The LD7560 is implemented an adjustable frequency Trembling function which provides the power supply designers to choose the optimized EMI performance and lowest system cost. The Trembling frequency is fixed internally ±4KHz which is incorporated with the 65KHz switching frequency.

Internal Slope Compensation

Stability is crucial for current mode control when it operates at more than 50% of duty-cycle. To stabilize the control loop, the slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. In LD7560, the internal slope compensation circuit has been implemented to simplify the external circuit design.

On/Off Control

Pulling COMP pin below 1.2V will turn off the LD7560 and disable the gate output pin of the LD7560. The off-mode will be released when the pull-low signal at COMP pin is removed.

Dual-Oscillator Green-Mode Operation

Lots of topologies have been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intends to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or by reducing the switching frequency.

What the LD7560 uses to implement the power-saving operation is Leadtrend Technology’s own IP. By using this dual-oscillator control, the burst -mode frequency can be well controlled and further to avoid the generation of audible noise.

Over Load Protection (OLP)

To protect the circuit from being damaged under over load condition or short condition, a smart OLP function is built in with the LD7560, as shown in Figure 17 shows the waveforms of the OLP operation. If output voltage drops, the feedback system tends to force the voltage loop toward the saturation then pulls the voltage of COMP pin to high. Id then pull the voltage high on COMP pin (VCOMP). Whenever the V_{COMP} trips to the OLP threshold 5.0V and continues over 60mS (when switching frequency is 65KHz), the protection will be activated and then turns off the gate output to stop the switching of

power circuit. The OLP delay time s to prevent the false trigger from the power-on and turn-off transient.

A divide-by-2 counter is implemented to reduce the average power under OLP behavior. Whenever OLP is activated, the output is latched off and the divide-by-2 counter starts to count the number Vcc reaches UVLO(off). The latch will be released when Vcc reaches the 2nd time and then the output is recovered to switching again.

By using such protection mechanism, the average input power can be reduced to a very low level so that the component temperature and stress can be controlled within the safe operating area.

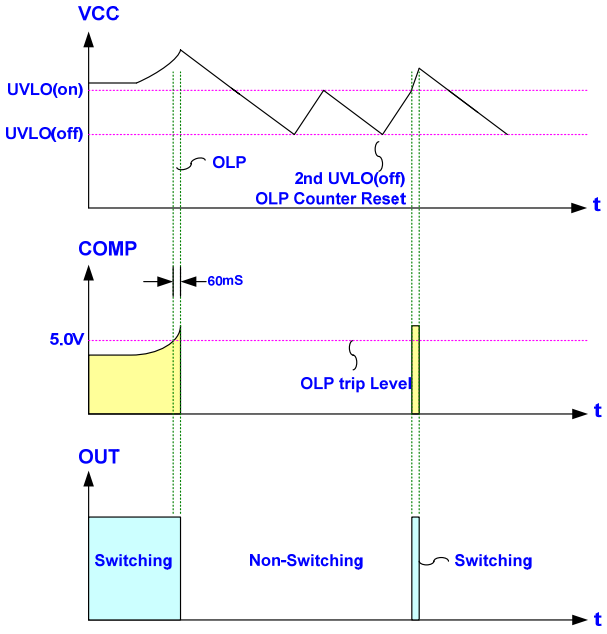


Fig. 17

OVP (Over Voltage Protection) on Vcc

The maximum V_{GS} ratings of the power MOSFETs are mostly for 30V. To prevent the V_{GS} enter fault condition, LD7560 is implemented with OVP function on Vcc. Whenever the Vcc voltage is higher than the OVP threshold, the output gate drive circuit will be shutdown simultaneously and the switching of the power MOSFET is disabled until the next UVLO(on).

The Vcc OVP functions of LD7560 is auto-recoverable. If the OVP condition, usually caused by open-loop of feedback, is not released, the Vcc will trip the OVP level again and re-shutdown the output. The Vcc works in hiccup mode as shown in Figure 18.

On the other hand, the removal of the OVP condition should render the Vcc level back to normal level, causing the output automatically returning to the normal operation

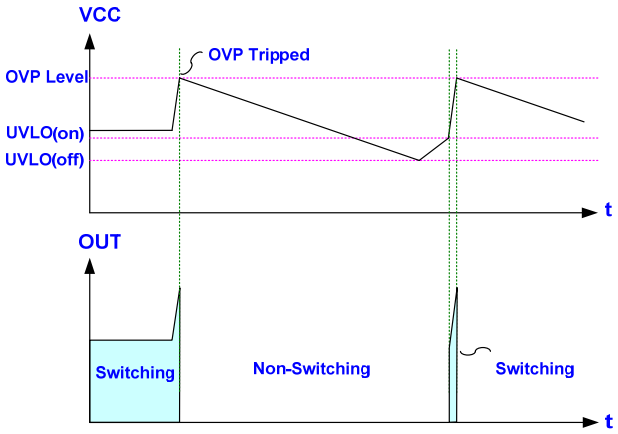


Fig. 18

SD Pin and Shut-Down Protection

For better power saving, the LD7560 will shut down under some light load or no load condition. Upon pulling SD pin to low level through a switch or photo coupler (parallel with SD pin to GND), OUT pin of will stop switching and turn off power circuit.

When SD pin is pulled down (below 1.1V Typ) by a switch or a photo coupler (parallel with SD pin to GND), as shown in Fig. 19. OUT pin of the LD7560 will stop switching immediately and turns off power circuit. At the same time, The LD7560 goes in to shut-down mode after internal de-bounce time (250μS). In such situation, the LD7560's operating current dramatically decreases (less than 100μA) in order to reduce power loss of PWM IC.

As soon as the switch or photo coupler is released, SD pin voltage will rise up due to internally increasing resistance. Meanwhile the LD7560 will be able to turn on the external switch of power circuit. Upon user's applications, the

LD7560 can be shut-down or enabled by connecting or removing the external circuit.

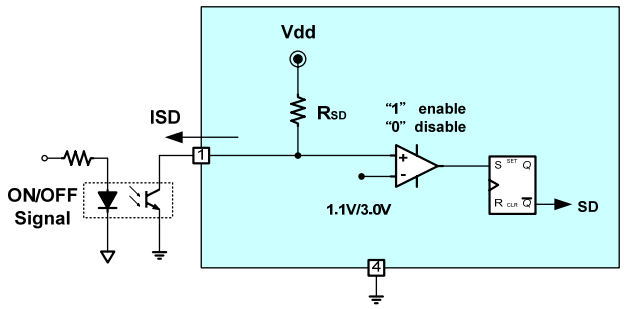


Fig. 19

Pull-Low Resistor on the Gate Pin of MOSFET

The LD7560 is internally equipped with an anti-floating resistor on the OUT pin to protect the output from abnormal operation or false triggering of MOSFET. Even so, we still recommend adding an external one on the MOSFET gate terminal to enhance protection in case of disconnection of gate resistor R_G during power-on (as shown in figure 20).

This external pull-low resistor is to prevent the MOSFET from damage during power-on as the gate resistor is disconnected. In such single-fault condition, as shown in figure 21, the resistor R8 can provide a discharge path to avoid the MOSFET from being falsely-triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the MOSFET should be always pulled low and placed in the off-state even if the gate resistor is disconnected or opened in any case.

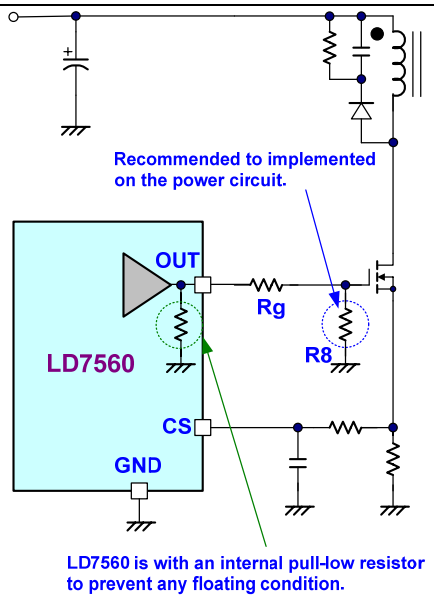


Fig. 20

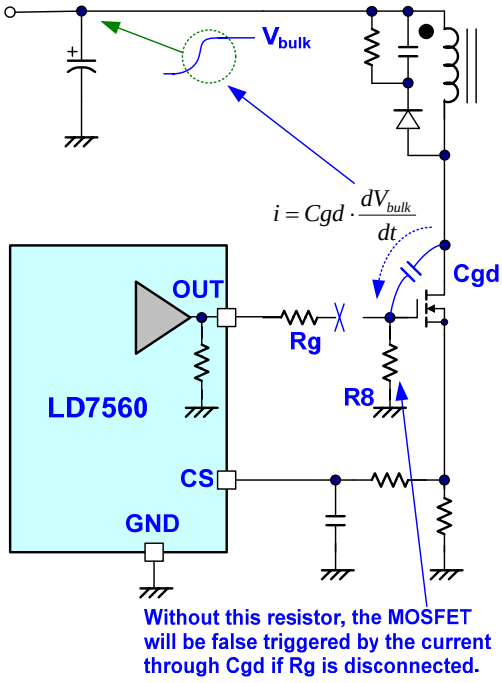


Fig. 21

Protection Resistor on the Hi-V Path

In some other Hi-V processes and designs, there is probably some parasitic SCR caused around HV pin, V_{CC} and GND. As shown in figure 22,, a small negative spike on the HV pin may trigger this parasitic SCR and cause latchup between Vcc and GND. Such latchup will damage

the chip easily because of the equivalent short-circuit induced.

Leadtrend's proprietary of Hi-V technology eliminate parasitic SCR in LD7560. Figure 23 shows the equivalent circuit of LD7560's Hi-V structure. Accordingly, LD7560 is more capable to sustain negative voltage than other similar products. Nevertheless, a 40KΩ resistor is recommended to add in the Hi-V path to play as a current limit resistor whenever a negative voltage is applied.

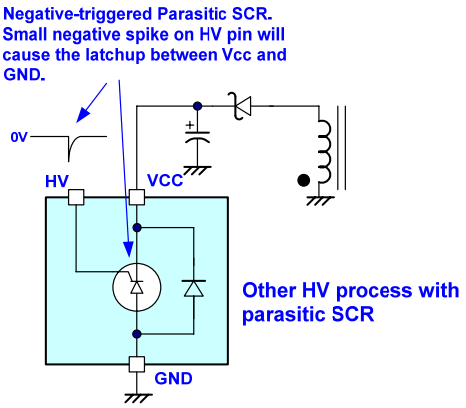


Fig. 22

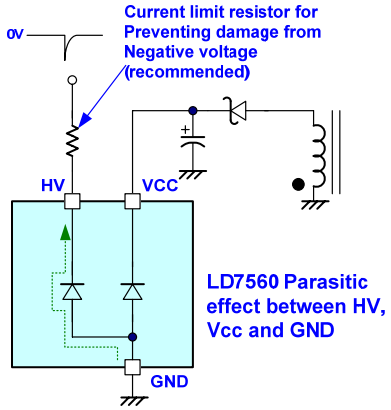
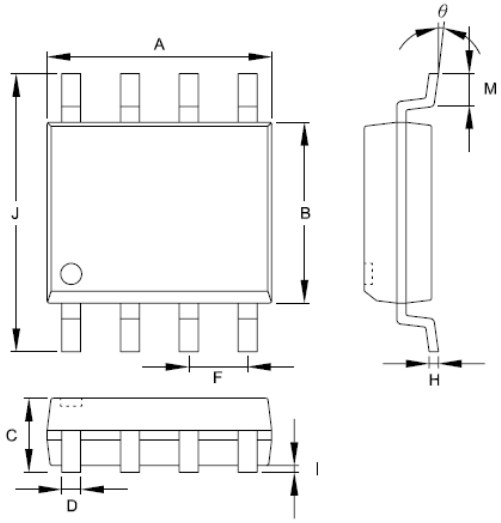


Fig. 23

Package Information

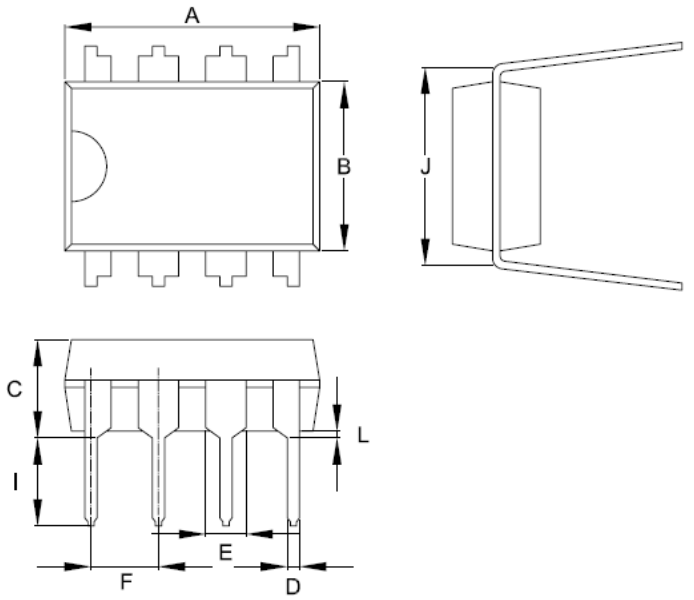
SOP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	7/10/2009	Original Specification