Green-Mode PWM Controller with High-Voltage Start-Up Circuit and Adjustable OLP Delay Time

REV. 00b

General Description

The LD7576A brings high performance, and combines highly integrated functions, protections and EMI-improve solution. It's an ideal solution for those cost-sensitive systems, reducing component count and overall system cost.

The LD7576A features near-lossless high voltage startup circuit, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. They are also equipped with protections, such as OLP (Over Load Protection), OVP (Over Voltage Protection) and OTP (Over Temperature Protection), to prevent circuit damage under abnormal conditions.

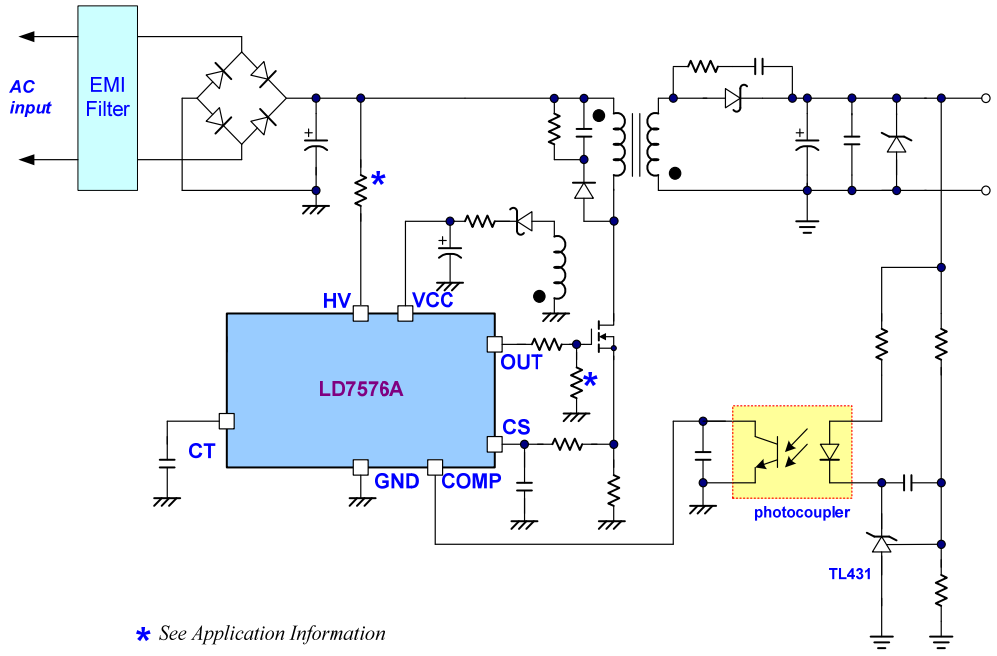
Features

- High-Voltage (500V) Startup Circuit
- Current Mode Control
- Non-Audible-Noise Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Slope Compensation
- OVP (Over Voltage Protection) on Vcc
- On-Chip OTP (Over Temperature Protection)
- OLP (Over Load Protection)
- 500mA Driving Capability
- Adjustable OLP delay time

Applications

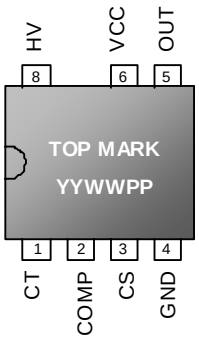
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

Typical Application

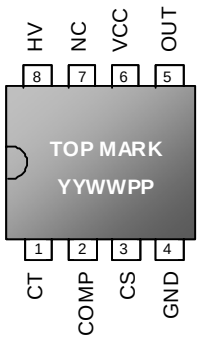


Pin Configuration

SOP-7 (TOP VIEW)



SOP-8, DIP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

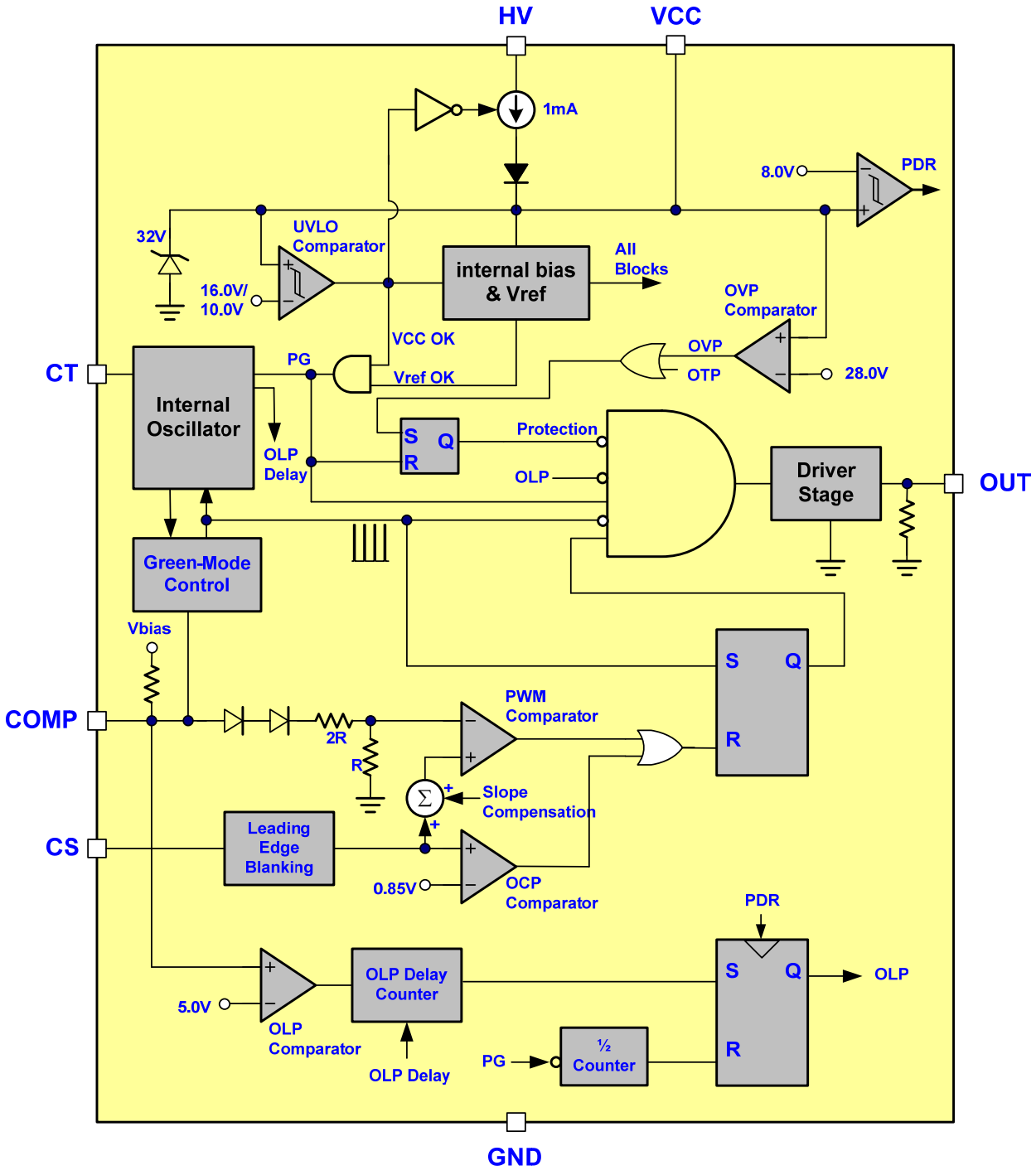
Part number	Package	Top Mark	Shipping
LD7576A GR	SOP-7	LD7576AGR	2500 /tape & reel
LD7576A GS	SOP-8	LD7576AGS	2500 /tape & reel
LD7576A GN	DIP-8	LD7576AGN	3600 /tube /Carton

The LD7576A is ROHS compliant/ Green Package.

Pin Descriptions

PIN	NAME	FUNCTION
1	CT	This pin is to program the frequency of a lower frequency timer. Connecting a capacitor to ground sets the OLP delay time.
2	COMP	Voltage feedback pin (same as the COMP pin in UC384X). Connecting a photo-coupler closes the control loop to achieve the regulation. A high quality ceramic capacitor (X7R), with capacitance of 102pF at least, is required for general applications.
3	CS	Current sense pin, for sensing the MOSFET current.
4	GND	Ground.
5	OUT	Gate drive output to drive an external MOSFET.
6	VCC	Supply voltage pin.
7	NC	Unconnected Pin.
8	HV	Connect this pin to a positive terminal of a bulk capacitor to provide the startup current for the controller. When Vcc voltage trips up to the UVLO(on), this HV loop will be off to save the power loss on the startup circuit.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3~ 30V
COMP, RT, CS	-0.3 ~7V
OUT	-0.3 ~Vcc+0.3
High-Voltage at HV pin	-0.3V~ 600V
Input Voltage for COMP, CT, and CS pins	-0.3 ~7V
Maximum Junction Temperature	150 °C
Operating Ambient Temperature	-40 °C to 85°C
Operating Junction Temperature	-40 °C to 125°C
Storage Temperature Range	-65 °C to 150°C
Package Thermal Resistance (SOP-7, SOP-8)	160 °C/W
Package Thermal Resistance (DIP-8)	100 °C/W
Power Dissipation (SOP-7, SOP-8, at Ambient Temperature = 85°C)	400mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260 °C
ESD Voltage Protection, Human Body Mode (except HV Pin)	3KV
ESD Voltage Protection, Machine Mode	300V
Gate Output Current	500mA

Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item Min	.	Max.	Unit
Supply Voltage V_{CC} 11		25	V
V_{CC} Capacitor	10	47	μF
CT Value	0.047	0.1	μF
COMP Pin Capacitor	1	100	nF

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)					
High-Voltage Current Source	Vcc< UVLO(on),HV=500V 0.5		1.0	1.5	mA
Off-State Leakage Current	Vcc> UVLO(off),HV=500V			35	μA
Supply Voltage (VCC Pin)					
Startup Current				100	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		2.7	3.5	mA
	V_{COMP}=3V		3.1	4.0	mA
	OLP tripped		0.5		mA
	OVP tripped		0.6		mA
	OTP tripped		0.5		mA
UVLO (off)		9.0	10.0	11.0	V
UVLO (on)		15.0	16.0	17.0	V
OVP Level		26.5	28.0	29.5	V
Voltage Feedback (COMP Pin)					
Short Circuit Current	V_{COMP}=0V		1.3	2.2	mA
Open Loop Voltage	COMP pin open		5.6		V
Green Mode Threshold VCOMP			2.35		V
Current Sensing (CS Pin)					
Maximum Input Voltage		0.80	0.85	0.90	V
Leading Edge Blanking Time			230		nS
Input impedance		1			MΩ
Delay to Output			100		nS
Oscillator for Switching Frequency					
Frequency		61.0	65.0	69.0	KHz
Temp. Stability	(-40°C ~105°C)			5	%
Voltage Stability	(VCC=11V-25V)			1	%
Low Frequency Timer (CT Pin)					
Low Frequency Period	CT=0.047μF		4.7		mS
Temp. Stability	(-40°C ~105°C)			5	%
Voltage Stability	(VCC=11V-25V)			1	%

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER CONDITIONS		MIN	TYP	MAX	UNITS
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA			1	V
Output High Level	VCC=15V, Io=20mA	8			V
Rising Time	Load Capacitance=1000pF		50	160	nS
Falling Time	Load Capacitance=1000pF		30	60	nS
OLP (Over Load Protection)					
OLP Trip Level			5.0		V
OLP Delay Time	CT=0.1μF		110		mS
	CT=0.047μF		45		mS
OTP (Over Temperature)					
OTP Level			140		°C
OTP Hysteresis			30		°C

Typical Performance Characteristics

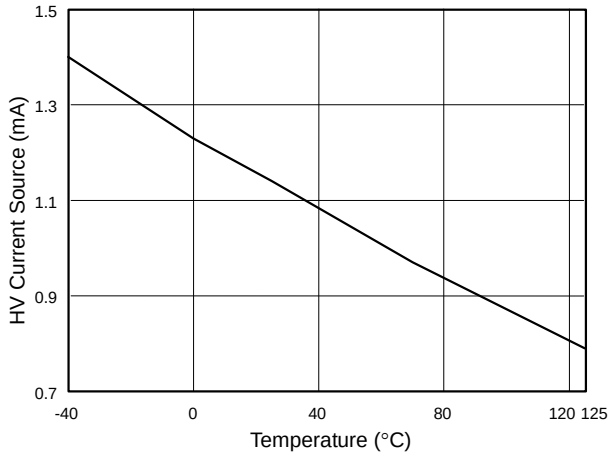


Fig. 1 HV Current Source vs. Temperature (HV=500V, Vcc=0V)

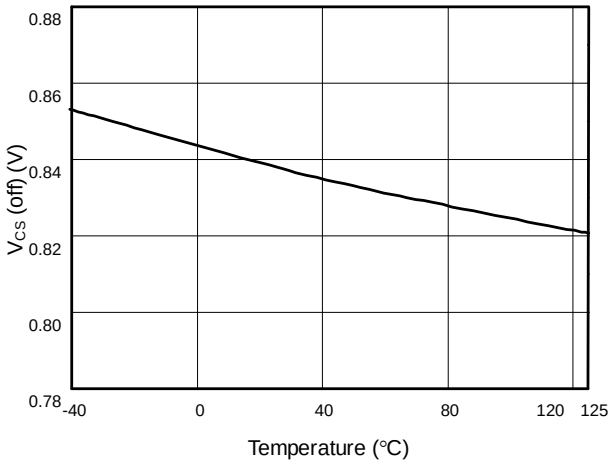


Fig. 2 V_{CS} (off) vs. Temperature

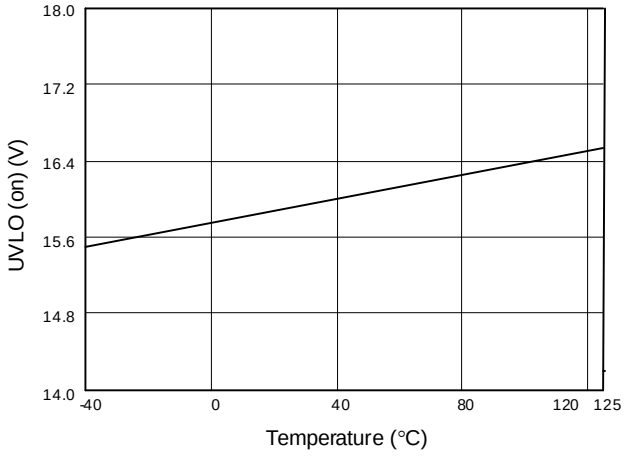


Fig. 3 UVLO (on) vs. Temperature

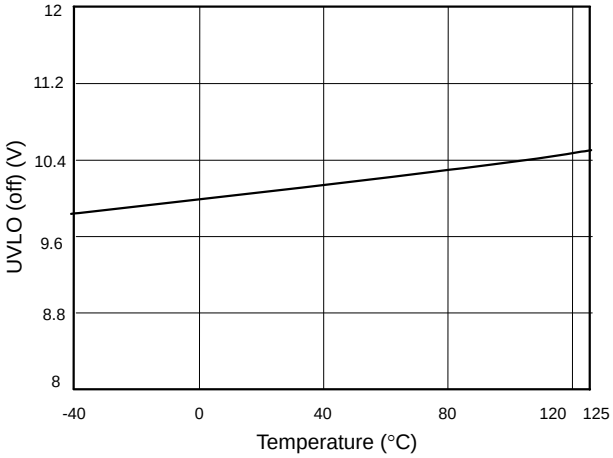


Fig. 4 UVLO (off) vs. Temperature

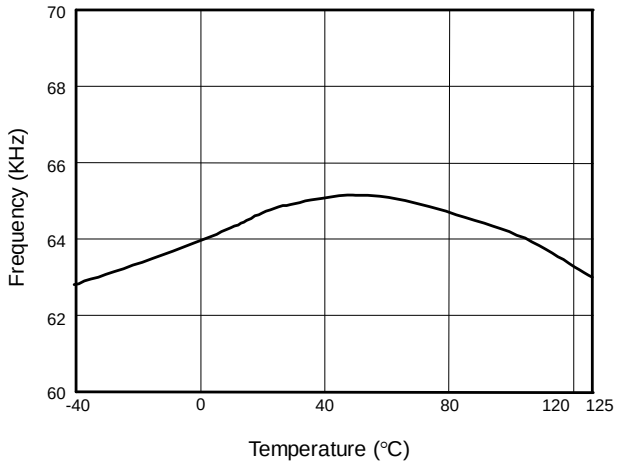


Fig. 5 Frequency vs. Temperature

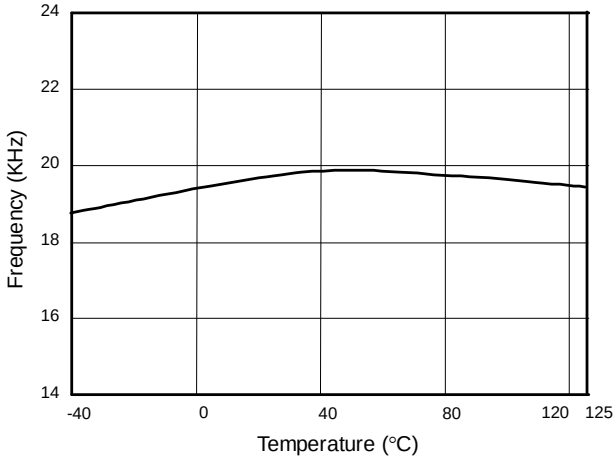


Fig. 6 Green Mode Frequency vs. Temperature

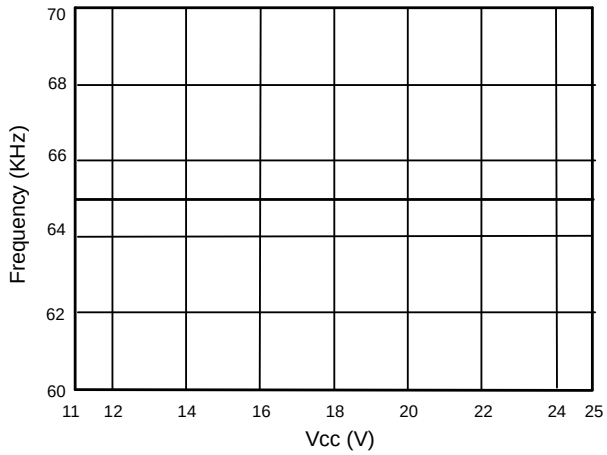


Fig. 7 Frequency vs. Vcc

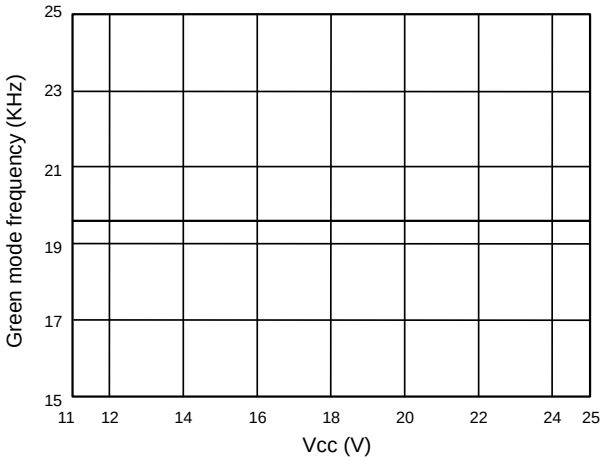


Fig. 8 Green mode frequency vs. Vcc

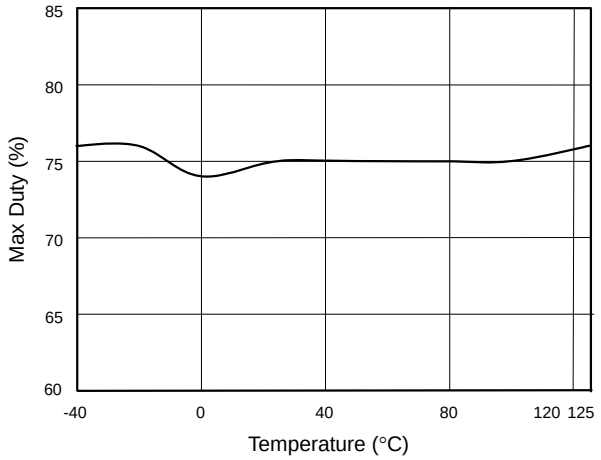


Fig. 9 Max Duty vs. Temperature

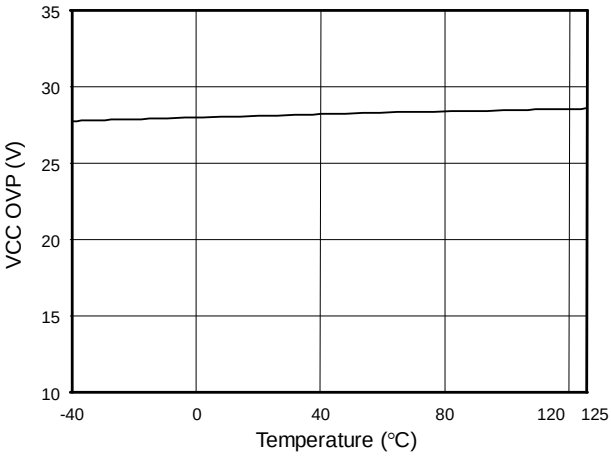


Fig. 10 VCC OVP vs. Temperature

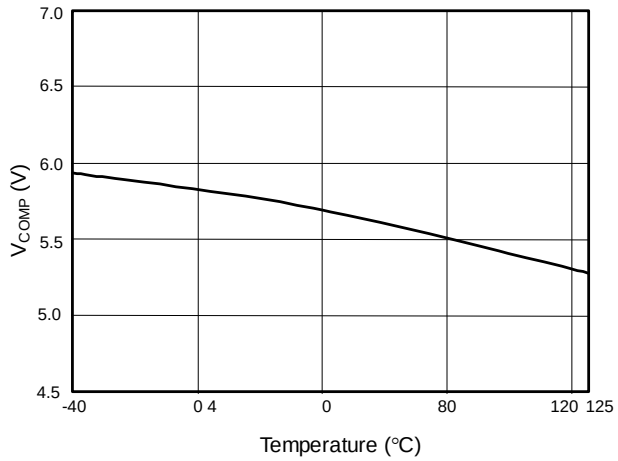


Fig. 11 V_{COMP} open loop voltage vs. Temperature

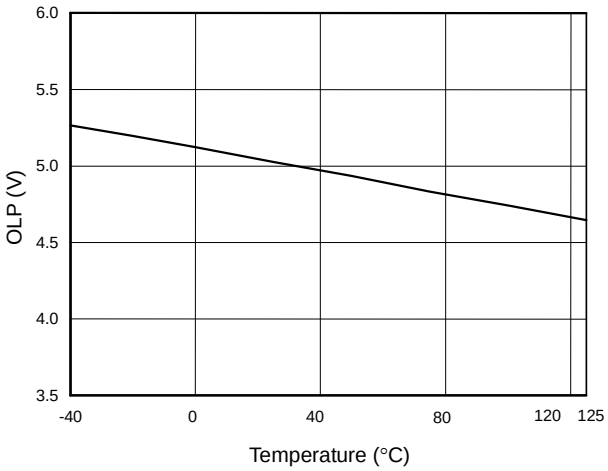


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is getting more and more important for switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation forces the PWM controllers to powerfully integrate more functions, thereby reducing the external part count. The LD7576A is ideal for these applications to provide an easy and cost effective solution; and its detailed features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

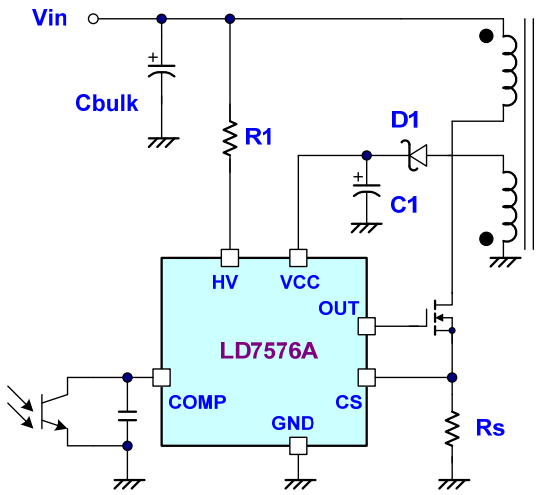


Fig. 13

Traditional circuits provide the startup current through a startup resistor to power up the PWM controller. Nevertheless, it consumes too significant power to meet the current power saving requirement. In most cases, startup resistors carry large resistance, which causes longer startup time.

To achieve the optimized topology, as shown in figure 13, LD7576A is implemented with a high-voltage startup circuit for such requirement. During startup, a high-voltage current source sinks current from the bulk capacitor to provide the startup current as well as to charge the Vcc capacitor C1. During the startup transient when the Vcc is lower than the UVLO threshold, the high-voltage current source is enabled to supply 1mA current. Meanwhile, the Vcc supply current is as low as 100μA such that most of the HV current is adopted to charge the Vcc capacitor. By using such configuration, the turn-on delay time will be almost the same no matter under low-line or high-line condition.

As the Vcc voltage rises higher than UVLO(on) to power on the LD7576A and further to deliver the gate drive signal, the high-voltage current source is disabled and the supply current is solely provided from the auxiliary winding of the transformer. Therefore, it eliminates the power loss on the startup circuit and performs highly power saving. An UVLO comparator is embedded to detect the voltage on the Vcc pin and to ensure the supply voltage high enough to power on the LD7576A PWM controller and to drive the power MOSFET. As shown in Fig. 14, a hysteresis is provided to prevent undesired shutdown from the voltage dip during startup. The turn-on and turn-off threshold levels are set at 16V and 10.0V, respectively

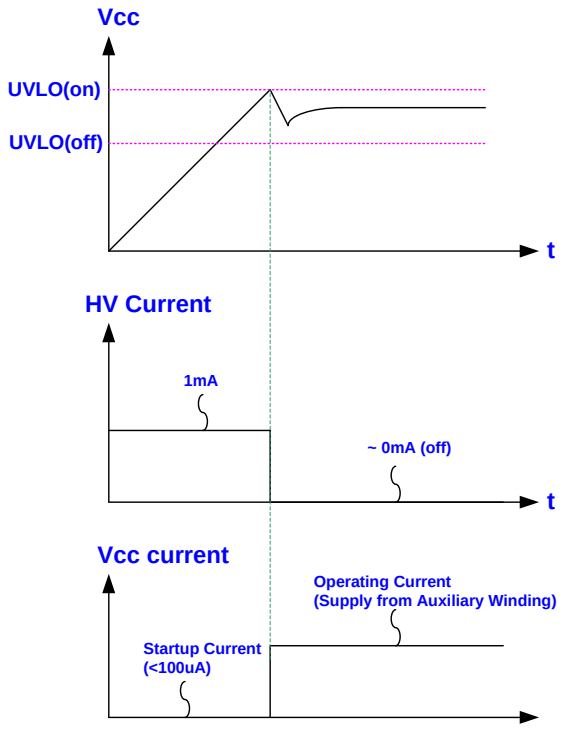


Fig. 14

Current Sensing, Leading-Edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feeds back both current signal and voltage signal to close the control loop and achieve regulation. The LD7576A detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A 230nS leading-edge blanking (LEB) time is provided in the input of CS pin to prevent false-triggering from a current spike. In low power applications, if the total pulse width of the turn-on spikes is less than 230nS and the negative spike on the CS pin does not exceed -0.3V, the R-C filter (as shown in figure15) can be eliminated. However, the total pulse width of the turn-on spike is related to output power, circuit design and PCB layout. It is strongly recommended to add a small R-C filter (as shown in figure 16) for higher power applications to avoid the CS pin from being damaged by the negative turn-on spike.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 500mA driving capability, is incorporated to drive a power MOSFET directly. The maximum duty-cycle of LD7576A is 75% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 on the secondary side through the photo-coupler to the COMP pin of LD7576A. The input stage of LD7576A, like the UC384X, is with 2 diodes voltage offset to feed the voltage divider with 1/3 ratio, that is,

$$V_{+(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally. Generally, an external capacitor in parallel to photo-coupler is required in application.

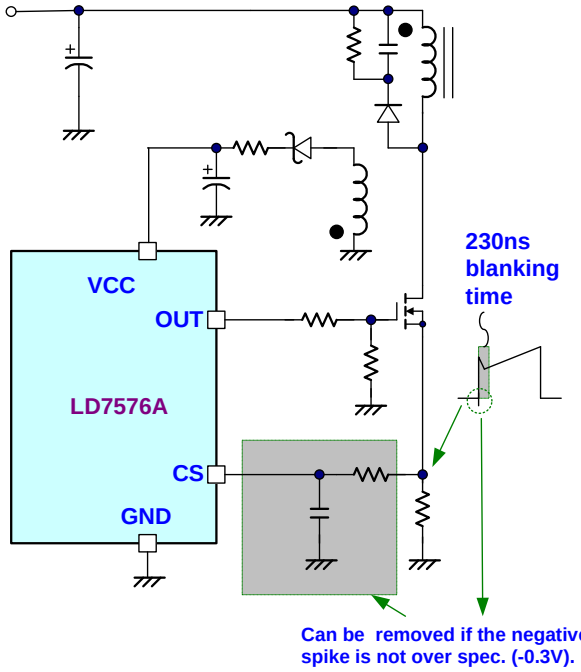


Fig. 15

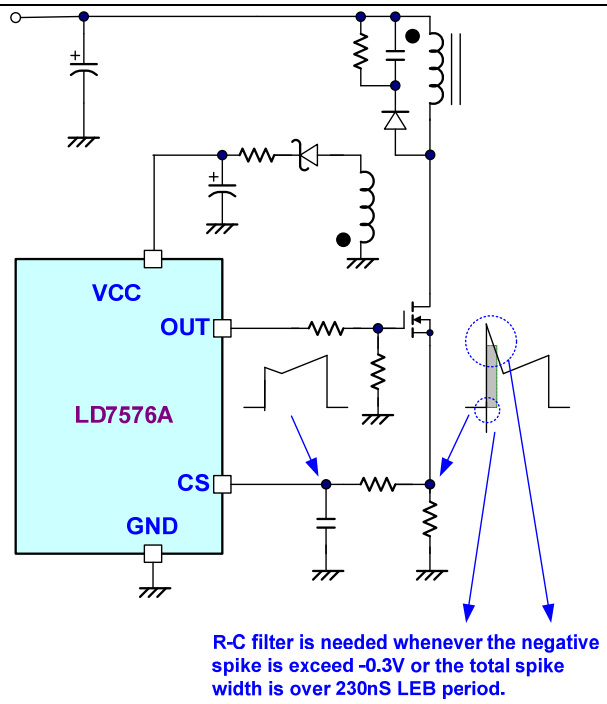


Fig. 16

Oscillator and Switching Frequency

The switching frequency of LD7576A is fixed at 65KHz internally to provide the optimized operations in consideration of the EMI performance, thermal treatment, component sizes and transformer design.

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is more than 50%. To stabilize the control loop, slope compensation is needed in the traditional UC 384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. In LD7576A, the internal slope compensation circuit has been implemented to simplify the external circuit design.

On/Off Control

By pulling COMP pin lower than 1.2V will disable the gate output pin of LD7576A immediately. The off mode can be released when the pull-low signal is removed.

Dual-Oscillator Green-Mode Operation

There are many different topologies has been implemented in different chips for the green-mode or power saving requirements such as “burst- mode control”, “skipping-cycle mode”, “variable off-time control “…etc.

The basic operation theory of all these approaches intended to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reduce the switching frequency.

By using LD proprietary dual-oscillator technique, the green-mode frequency can be well controlled to avoid the generation of audible noise.

Over Load Protection (OLP) - Auto Recovery

To protect the circuit from being damaged during over load condition and short or open loop condition, the LD7576A is implemented with smart OLP function. LD7576A features auto recovery function, the waveform of which is exemplified in figure 17. In the example of the fault condition, the feedback system tends to force the voltage loop toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the V_{COMP} ramps up to the OLP threshold of 5V and stays for longer than the OLP delay time, the protection will be activated to turn off the gate output and to stop the switching of power circuit. The OLP delay time, set by the capacitor connected to CT pin, is to prevent the false triggering from the power-on and turn-off transient. The higher capacitance of the capacitor in CT pin, the longer OLP delay time. The recommended capacitance will be 0.1μF for a OLP delay time around 110mS and 0.047μF for around 45mS.

A divide-by-2 counter is implemented to reduce the average power under OLP behavior. Whenever OLP is activated, the output is latched off and the divide-by-2 counter starts to count the number Vcc reaches UVLO(off). The latch will be released when Vcc reaches the 2nd time and then the output is recovered to switching again.

With the protection mechanism, the average input power will be minimized, so that the component temperature and stress can be controlled within a safe operating area.

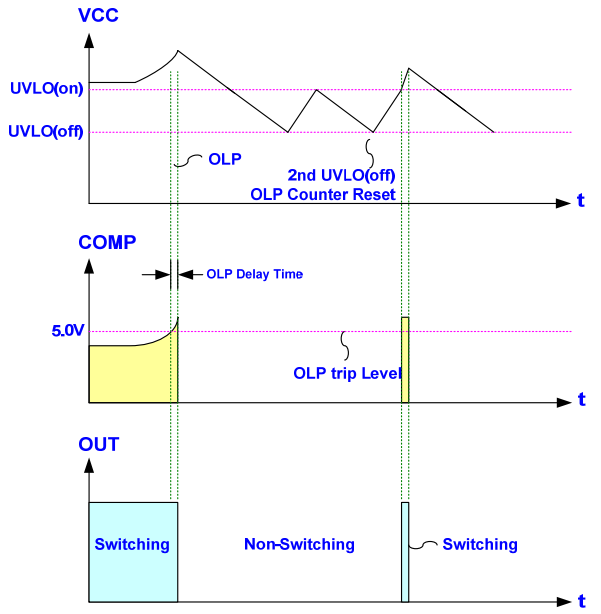


Fig. 17

OVP (Over Voltage Protection) on Vcc - Auto Recovery

The maximum V_{GS} ratings of the power MOSFETs are mostly for 30V. To prevent the V_{GS} enter fault condition, LD7576A is implemented with OVP function on Vcc. Whenever the Vcc voltage is higher than the OVP threshold, the output gate drive circuit will be shutdown simultaneously and the switching of the power MOSFET is disabled until the next UVLO(on).

The Vcc OVP functions of LD7576A is auto-recoverable. If the OVP condition, usually caused by open-loop of feedback, is not released, the Vcc will trip the OVP level again and re-shutdown the output. The Vcc works in hiccup mode as shown in Figure 18.

Otherwise, when the OVP condition is removed, the Vcc level will be resumed and the output will automatically return to the normal operation.

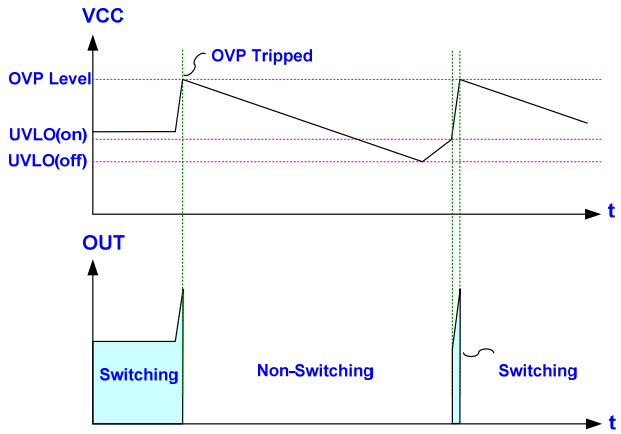


Fig. 18

Pull-Low Resistor on the Gate Pin of MOSFET

The LD7576A is internally equipped with an anti-floating resistor on the OUT pin to protect the output from abnormal operation or false triggering of MOSFET. Even so, we still recommend adding an external one on the MOSFET gate terminal to provide more protection in case of disconnection of gate resistor R_G during power-on in Fig. 19.

In such single-fault condition, as shown in figure 20, the resistor R8 can provide a discharge path to avoid the MOSFET from being falsely-triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the MOSFET is always pulled low and placed in the off-state even if the gate resistor is disconnected or opened in any case.

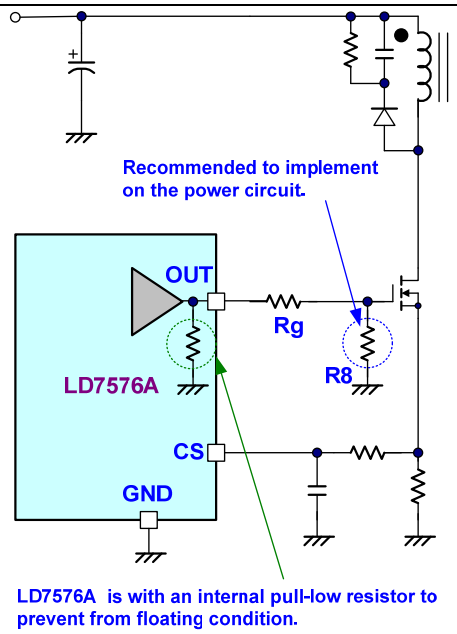


Fig. 19

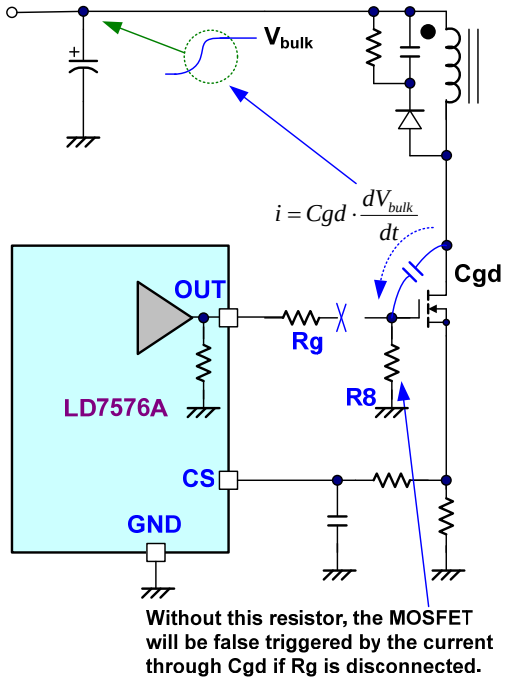


Fig. 20

Protection Resistor on the Hi-V Path

In some other Hi-V process and design, there may be a parasitic SCR caused around HV pin, Vcc and GND. As shown in figure 21, a small negative spike on the HV pin may trigger this parasitic SCR and cause latchup between Vcc and GND. It will intend to damage the chip because of the equivalent short-circuit induced by such latch up behavior.

Leadtrend's proprietary of Hi-V technology eliminate parasitic SCR in LD7576A. Figure 22 shows the equivalent circuit of LD7576A of Hi-V structure. Accordingly, LD7576A is more capable to sustain negative voltage than other similar products. Nevertheless, a 40KΩ resistor is recommended to be added on the Hi-V path to play as a current limit resistor whenever a negative voltage is applied.

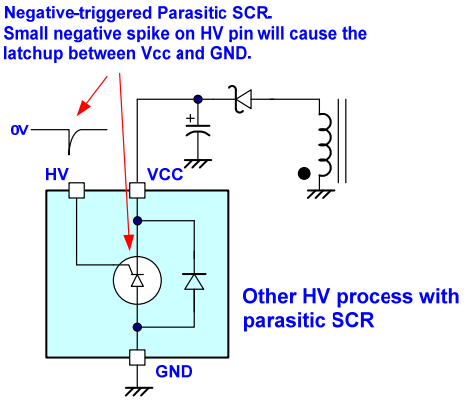


Fig. 21

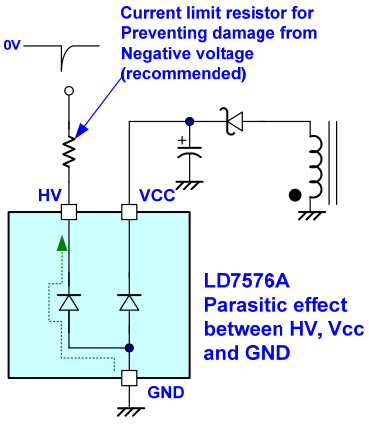


Fig. 22

Frequency Trembling

The LD7576A is built in with adjustable frequency trembling function, which provides the power supply designers to optimize EMI performance and system cost. The Trembling frequency was internally set for ±4KHz when incorporating with 65KHz switching frequency. On

the other hand, the modulating frequency can be set by adjusting the capacitance value on the CT pin. The best value for the CT capacitance is from 0.047μF to 0.1μF, typically generating modulating frequency of 200Hz ~100Hz. It is a tradeoff to select proper CT value between the EMI performance and OLP delay time. In theory, higher CT value will accompany with longer OLP delay time.

It is strongly recommended to use higher quality capacitor (low temperature coefficient and low initial tolerance) like X7R type ceramic capacitor to avoid the variation on the EMI performance under different temperature conditions. As show in figure 23, short layout loop from CT to GND is prefer to prevent any unexpected parasitic effect or coupling noises. And beware not to connect any extra loading to CT pin except of the capacitor to minimize the affect on modulating frequency.

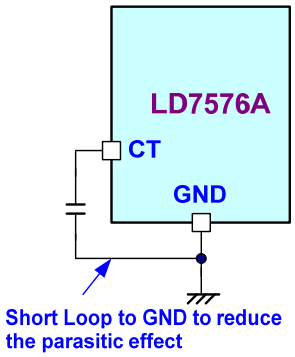
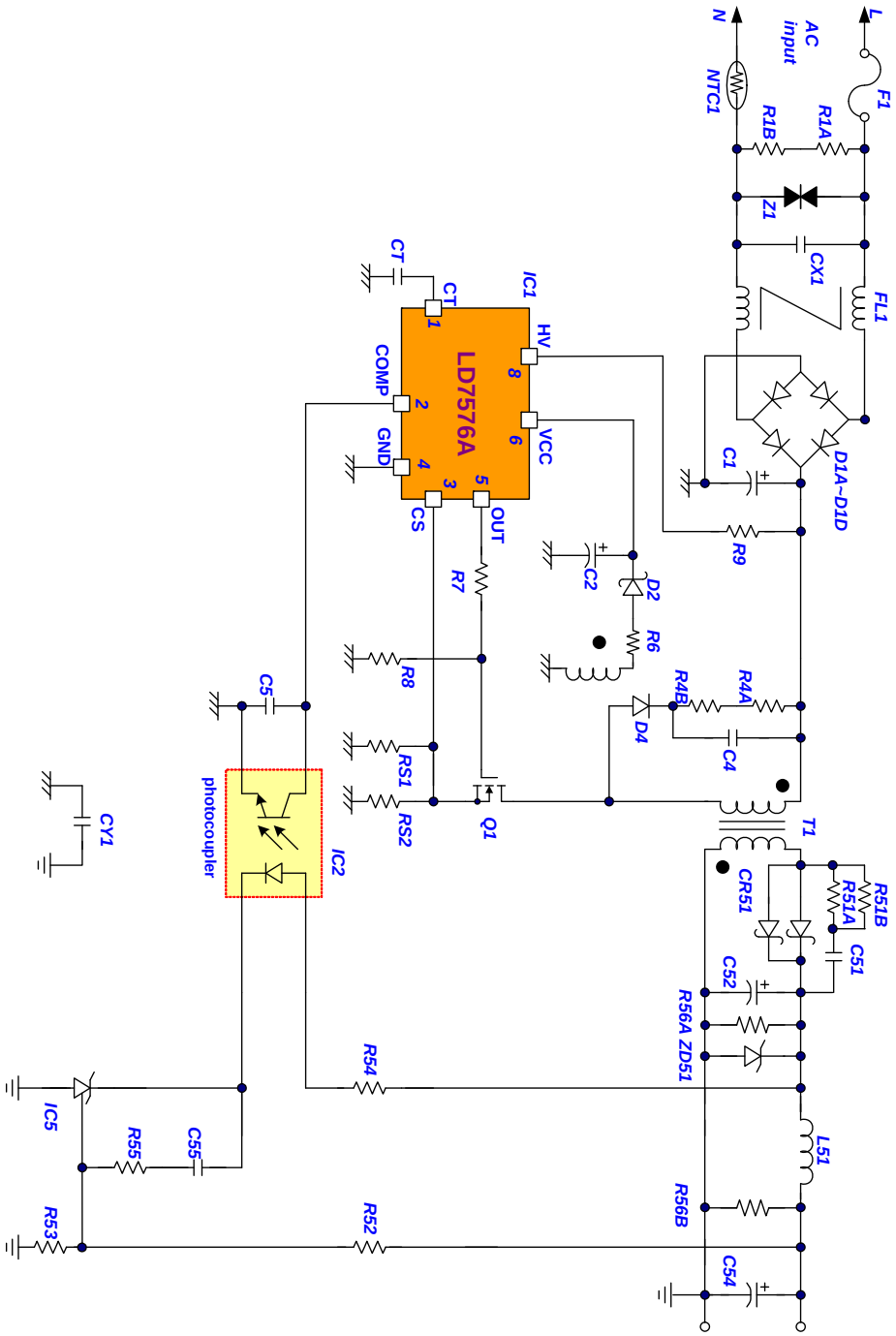


Fig. 23

On-Chip OTP

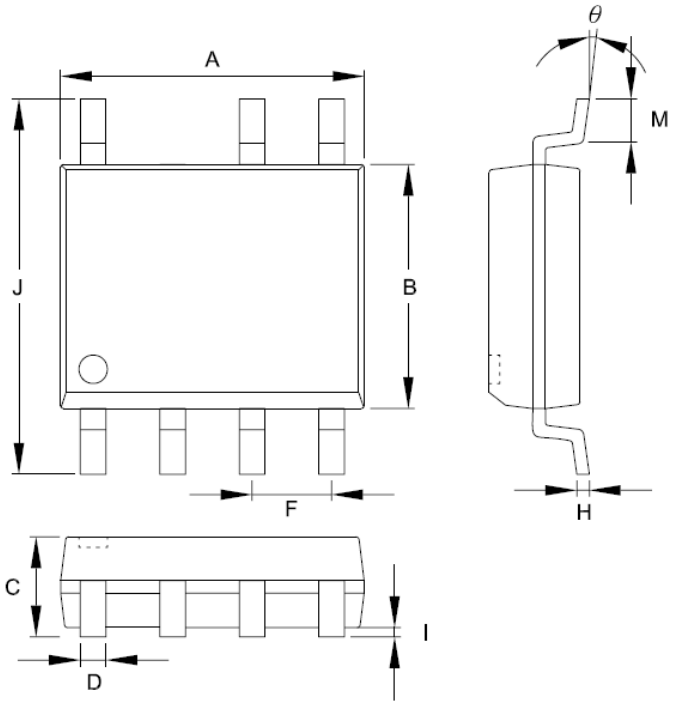
An internal OTP circuit is embedded inside the LD7576A to provide the worst-case protection for this controller. When the chip temperature rises higher than the trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window.

Reference Application Circuit --- 10W (5V/2A) Adapter



Package Information

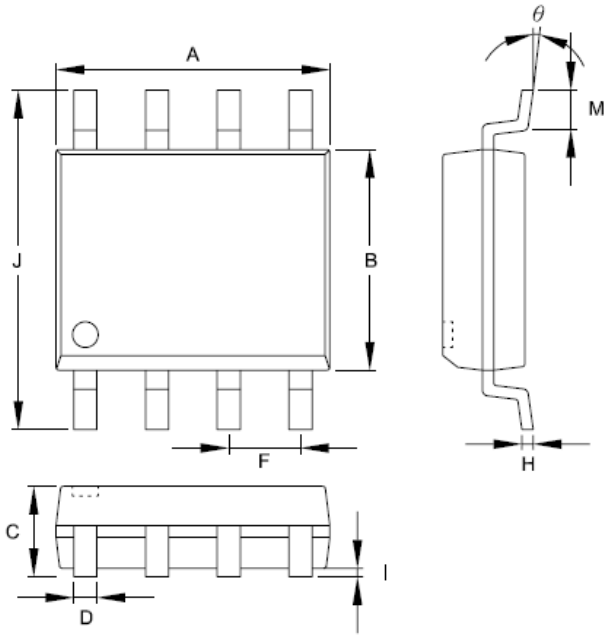
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

SOP-8



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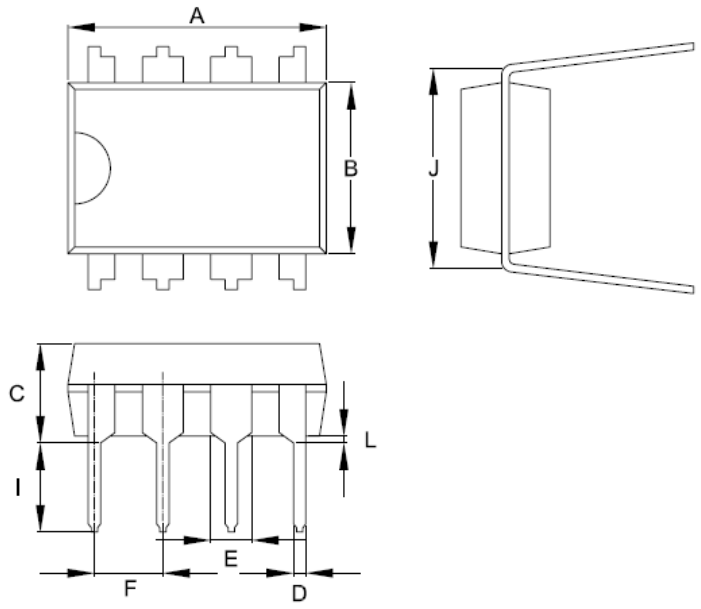
Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A 9.017		10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.290	0.325
L 0.381		------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	3/17/2009	Original Specification.
00a	5/26/2009	Package option: SOP-7
00b	11/29/2009	Implementation: Absolute Maximum Rating