Transition-Mode PFC Controller with Fault Condition Protection

REV. 00

General Description

The LD7591T is a voltage mode PFC controller operating on transition mode, with several integrated functions of protection, such as OVP, OCP, and Brown-in protection. It reduces the components counts and is available in a SOP-8 or DIP-8 package. Those make it an ideal design for low cost applications.

It provides functions of low startup current, over voltage protection, open feedback protection, disable function, over current protection, under voltage lockout and integrated LEB of current sensing. Unlike the traditional current mode PFC controller, LD7591T is free from extra rectified AC line voltage information to minimize the power loss.

The LD7591T will be disabled if INV pin voltage falls below 0.45V and the operating current rises over 65μA

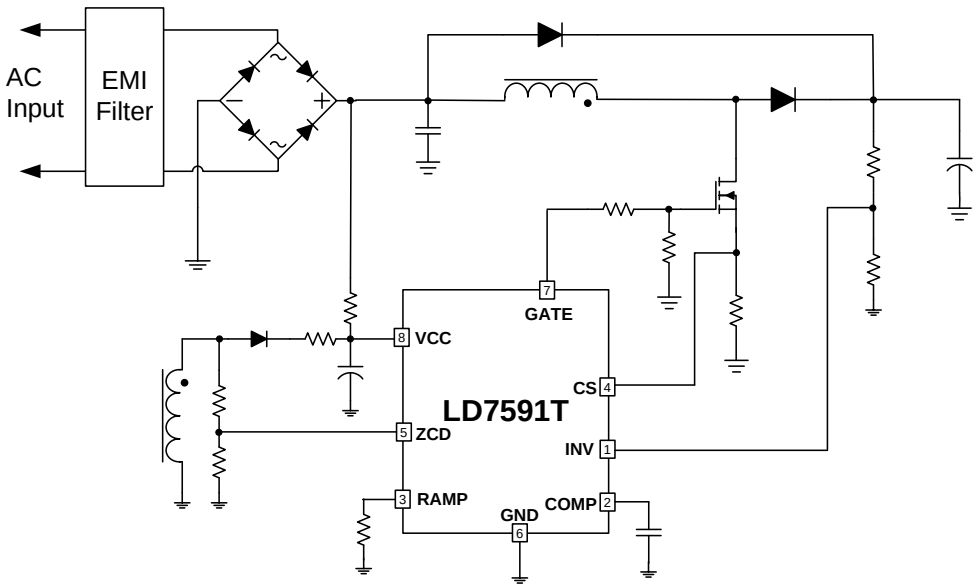
Features

- Transition mode of PFC pre-regulator
- Voltage mode control
- Programmable max. on-time
- Low Startup Current (<30μA)
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Open-Feedback Protection and Disable Function
- OVP (Over Voltage Protection)
- OCP (Cycle by cycle current limiting)
- 800/-1200mA Driving Capability
- Internal OTP function

Applications

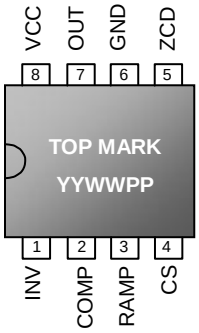
- Adaptor of Output above 65W.
- Open Frame Switching Power Supply
- LCD TV Power Supply
- LED Power Supply

Typical Application for Boost PFC



Pin Configuration

SOP-8 & DIP-8 (TOP VIEW)



YY: Year code (D:2004, E:2005…)
WW: Week code
PP: Production code

Ordering Information

Part number	Package	Top Mark	Shipping
LD7591T GS	SOP-8	LD7591TGS	2500 /tape & reel
LD7591T GN	DIP-8	LD7591TGN	3600 /tube /Carton

The LD7591T is ROHS compliant/ Green Packaged.

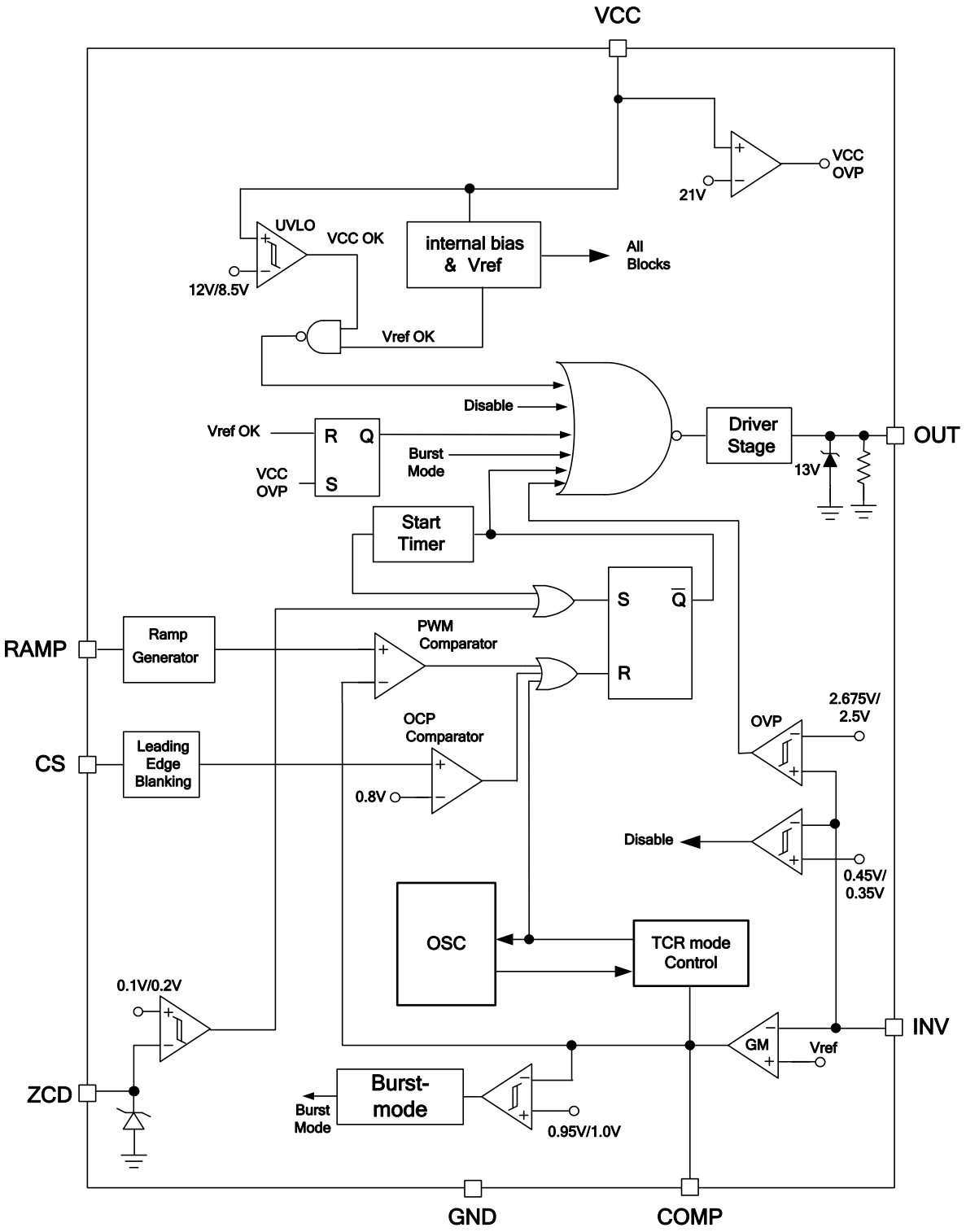
Pin Descriptions

Pin	NAME	FUNCTION
1	INV	Output voltage feed back control
2	COMP	Output of the error amplifier for voltage loop compensation to achieve stable
3	RAMP	Ramp generator, connecting a resistor to GND pin to set the saw tooth signal
4	CS	Current sense pin, connect to sense the MOSFET current for OCP
5	ZCD	Detecting zero crossing of input signal
6	GND	Ground
7	OUT	Gate drive output to drive the external MOSFET
8	VCC	Power source VCC pin

Recommended Operating Conditions

Item	Min.	Max.	Unit
Vcc pin capacitor	22	47	μF
Comp pin capacitor	0.1	4.7	μF
RAMP pin resistor	4.7k	100k	Ω

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3 ~26V
OUT	-0.3 ~VCC +0.3V
COMP, INV, CS, RAMP, ZCD	-0.3 ~7V
Maximum Junction Temperature	150°C
Operating Junction Temperature Range	-40°C to 125°C
Operating Ambient Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SO-8, θ_{JA})	160°C/W
Package Thermal Resistance (DIP-8, θ_{JA})	100°C/W
Power Dissipation (SOT-8, at Ambient Temperature = 85°C)	400mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V
Gate Output Current	800mA/-1200mA

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(V_{CC}=14.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)					
Startup Current	VCC<UVLO ON		20	30	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		2.0		mA
	V_{COMP}=3V		2.5		mA
	V_{CC} OVP		0.45		mA
	V_{INV}=0V		65	95	μA
UVLO (off)		7.5	8.5	9.5	V
UVLO (on)		11.0	12.0	13.0	V
VCC OVP Level		19.5	21	22.5	V
Error Amplifier (Comp Pin)					
Feedback Input Voltage, V_{REF}		2.465	2.500	2.535	V
Input Bias Current	V_{INV}=1V~4V	-0.5		0.5	μA
Transconductance			140		μmho
Output Sink Current	V_{INV}= V_{REF} +0.05V		7		μA
Output Source Current	V_{INV}= V_{REF} -0.05V		-7		μA
Output Source Current	V_{INV}= V_{REF} -1V		-200		μA
Output Upper Clamp Voltage	V_{INV}= V_{REF} -0.1V	5.4	5.9	6.4	V
TCR Mode Frequency	VCOMP=1.05V	70	90	110	KHz
Burst Mode COMP pin Threshold Voltage			0.95		V
	Hysteresis		50		mV
INV pin					
OVP Trip Level		2.62	2.675	2.73	V
	OVP Hysteresis		0.175		V
Enable Threshold Voltage		0.4	0.45	0.5	V
	Enable Hysteresis		0.1		V
Current Sensing (CS Pin)					
Current Sense Input Threshold Voltage		0.75	0.8	0.85	V
Input bias current	V_{CS}=0V~1V	0		1.0	μA
LEB time			250		ns
Zero Current Detector (ZCD Pin)					
Upper Clamp Voltage	I_{DET}=100μA		6.0		V
Lower Clamp Voltage	I_{DET}=100μA		-0.7		V
Input Voltage Threshold		0.05	0.1	0.15	V
	Hysteresis		0.1		V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input bias current	V_{ZCD}=1V~4V, OUT=OFF	0.0	1.0		μA
Maximum Delay from ZCD to Output			250		ns
Maximum ON-Time, Ton-max (Ramp Pin)					
Maximum On Time Voltage	R_{RAMP}=40.5K	2.784	2.900V	3.016	V
Maximum On Time Programming	R_{RAMP} =40.5K	19	24	29	μs
Maximum On Time	$R_{RAMP} \geq$ 100K		40		μs
Minimum OFF-Time					
Minimum OFF-Time			1		μs
Minimum OFF-Time Programming			0.10		Ton-max
Gate Drive Output (OUT Pin)					
Output Low Level	V_{CC}=12V, I_{SINK}=20mA			0.5	V
Output High Level	V_{CC}=12V, I_{SOURCE}=20mA	9		12	V
Output High Clamp Level	V_{CC}=18V		13		V
Rising Time	V_{CC} =12V, CL=1000pF		75	150	ns
Falling Time	V_{CC} =12V, CL=1000pF		25	100	ns
Starter					
Start Timer Period		50	150	300	μs
OTP (Over Temp. Protection)					
OTP Trip level			140		°C
OTP Hysteresis			30		°C

Typical Performance Characteristics

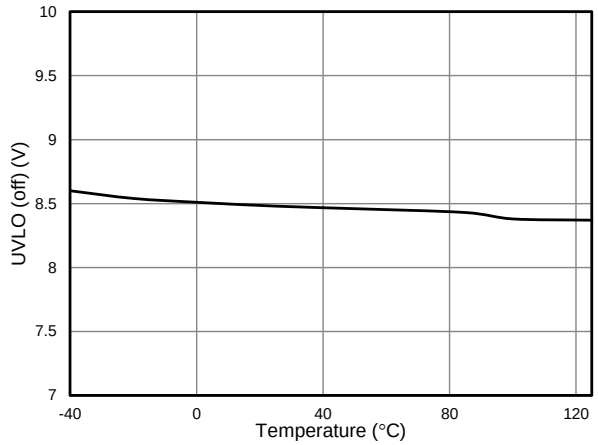


Fig. 1 UVLO (off) vs.Temperature

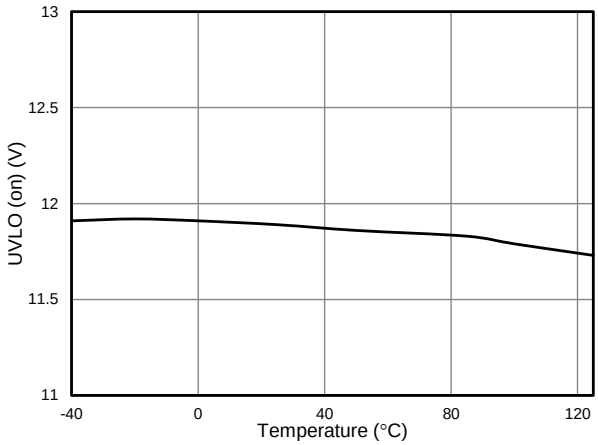


Fig. 2 UVLO (on) vs.Temperature

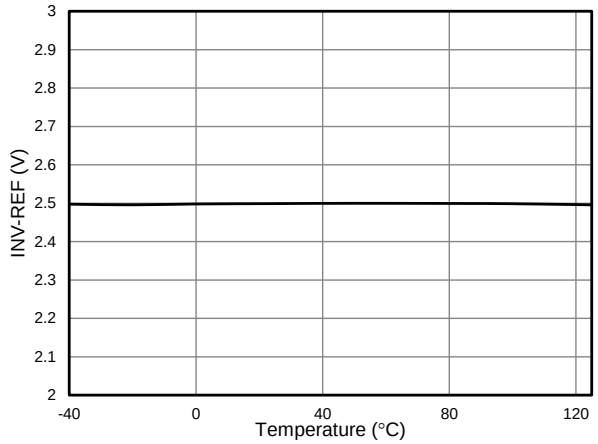


Fig. 3 INV-REF vs.Temperature

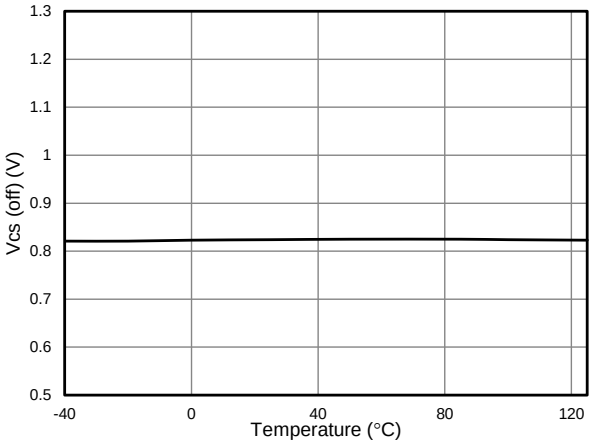


Fig. 4 Vcs (off) vs.Temperature

Application Information

Operation Overview

The LD7591T is an excellent voltage mode PFC controller. It meets the IEC61000-3-2 requirement and is intended for the use in those pre-regulator that demand low power harmonics distortion. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD7591T PFC controllers and further to drive the power MOSFET. As shown in Fig. 5, a hysteresis is built in to prevent the shutdown from the voltage dip during start up. The turn-on and turn-off threshold level are set at 12.0V and 8.5V, respectively.

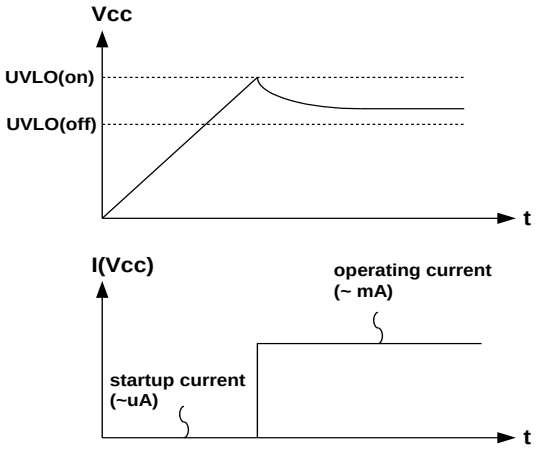


Fig. 5

Startup Current and Startup Circuit

The typical startup circuit to generate the LD7591T Vcc is shown in Fig. 6. At the startup transient, the Vcc is lower than the UVLO threshold thus there is no gate pulse produced from LD7591T to drive power MOSFET. Therefore, the current through R1 will provide the startup current to charge the capacitor C1. When the Vcc voltage is high enough to turn on the LD7591T and then it will send a gate drive signal to draw the supply current from the auxiliary winding of the PFC choke. Lower startup current requirement for the PFC controller will help to increase the value of R1 and reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD7591T is only 30μA. If a higher resistance value of R1 is chosen, it usually takes more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

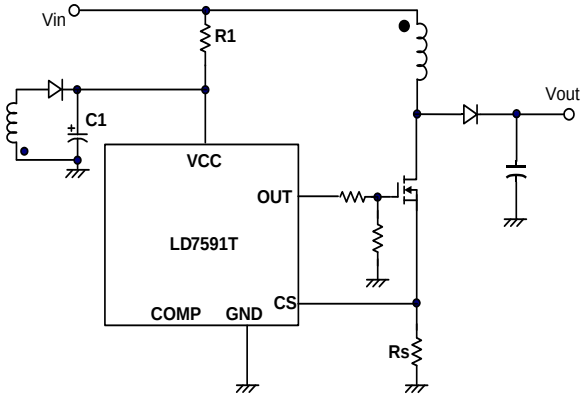


Fig. 6

Output Voltage Setting

The LD7591T monitors the output voltage signal on INV pin through a resistor divider pair of Ra and Rb. A transconductance amplifier is used to replace the conventional voltage amplifier. The transconductance amplifier (voltage controlled current source) enhances the implementation of OVP and disables function. The output current of the amplifier changes with the various voltage of the inverting and non-inverting input of the amplifier. The output voltage of the amplifier is compared with the internal ramp signal to generate the turn-off signal. The output voltage is determined by the following relationship.

$$V_{OUT} = 2.5V(1+\frac{Ra}{Rb})$$

Where Ra and Rb are top and bottom feedback resistor values (as shown in the Fig. 7).

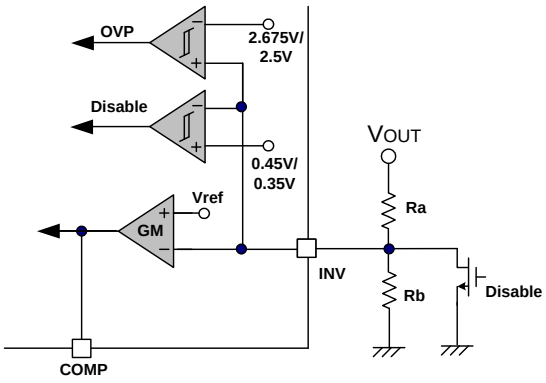


Fig. 7

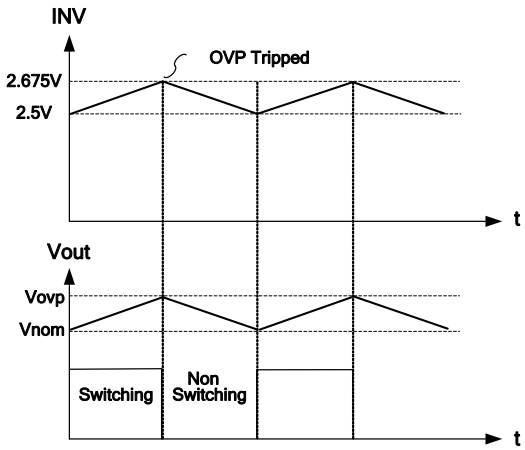


Fig. 8

OVP and Disable on INV pin

To prevent the over-voltage on the output capacitor from the fault condition, LD7591T is implemented with an OVP function on INV pin. Once the INV voltage is higher than the OVP threshold voltage 2.675V, the output gate drive circuit will be shut down simultaneously thus to stop the switching of the power MOSFET until the INV pin down to 2.5V. The OVP function in LD7591T is an auto-recovery type protection. The Fig. 8 shows its operation. On the other hand, if the OVP condition is removed, the Vcc level will get back to normal level and the output will automatically return to the normal operation.

The disable comparator disables the operation of the LD7591T when the voltage of the inverting input is lower than 0.35V and there is hysteresis of 100mV. An external small signal MOSFET can be used to disable the IC, referring to Fig. 7. The IC operating current decreases below 65μA to reduce power consumption if the IC is disabled.

Zero Current Detection (ZCD)

Fig. 9 shows typical ZCD-block. The Zero Current Detection block will switch on the external MOSFET as the current through the boost inductor drops to zero in using an auxiliary winding coupled with the inductor. This feature allows transition-mode operation. If the voltage of the ZCD pin goes higher than 0.2V, the ZCD comparator waits until the voltage rises above 0.1V. If the voltage goes below 0.1V, the zero current detector will turn on the MOSFET. The ZCD pin is protected internally by two clamps, 6.0V-high clamp and -0.7V-low clamp. The 150μs timer generates a MOSFET turn on signal if the driver output has been low for more than 150μs from the falling edge of the driver output.

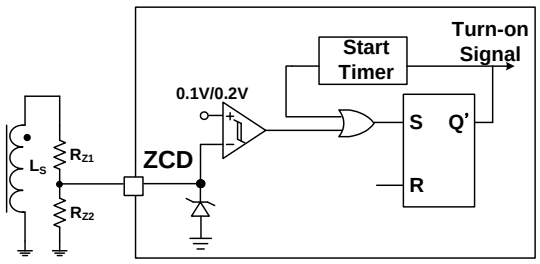


Fig. 9

Fig. 10 shows typical ZCD-related waveforms. Rz1 will produce some delay because of the capacitance carried by ZCD pin, it therefore delay the turn-on time accordingly. The switch will be turned on when the inductor current reaches zero; because of the structure of the ZCD delay, it will be turned on after some delay time. During this delay time, the stored charge of the COSS (MOSFET output capacitor) will be discharged through the path indicated in Fig. 11. This charge is transferred into a small filter capacitor $C_{IN}1$, which is connected to the bridge diode. Therefore, there is no current flowing from the input side. That is, the input current I_{IN} is zero during this period. In order to reduce the negative current flowing to the internal diode, a larger resistance of R_{Z1} over 47kΩ is recommended.

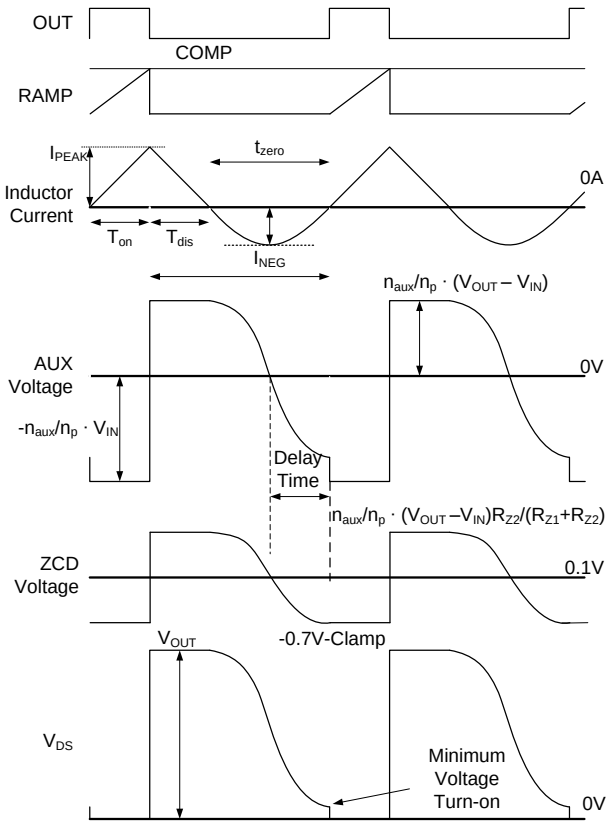


Fig. 10

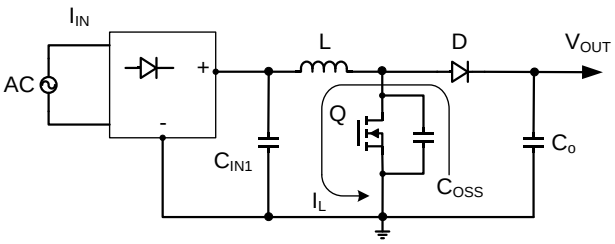


Fig. 11

Ramp Generator Block

The output of the gm error amplifier and the output of the ramp generator block are compared to determine the MOSFET on time, as shown in Fig. 12. The slope of the ramp is determined by an external resistor connected to the RAMP pin. The voltage of the RAMP pin is 2.9V and the slope is proportional to the current flowing out of the RAMP pin. The internal ramp signal has a 1V offset; therefore, the drive output will be shut down if the voltage of the COMP pin is lower than 0.95V. The programmed on-time will be at its maximum when the COMP pin is open. The COMP pin open voltage is about 5.4~6.4V. According to the slope of the internal ramp, the maximum on-time can be programmed. The necessary maximum on-time will be achieved depending on the boost inductor, lowest AC line voltage, and maximum output power. The resistor value should be designed properly. The maximum on-time can be obtained from below

$$T_{ON-Time(MAX)} = \frac{R_{RAMP}}{1.58 \cdot 10^{9}}$$

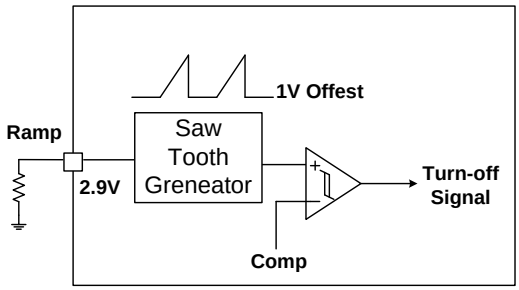


Fig. 12

Output Drive Stage

An output stage of a CMOS buffer, with typical 800mA/-1200mA driving capability, is incorporated to drive a power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage is higher than 13V.

Current Sensing and Leading-edge Blanking

The typical voltage mode of PFC controller feedbacks the voltage signals to close the control loop and achieve regulation. The LD7591T detects the primary MOSFET current from the CS pin, which is for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.8V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.8V}{R_S}$$

A 250ns leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. The R-C filter may be eliminated in some low power applications, such as the pulse width of the turn-on spikes is below 250ns and the negative spike on the CS pin is below -0.3V.

However, the pulse width of the turn-on spike is determined according to the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

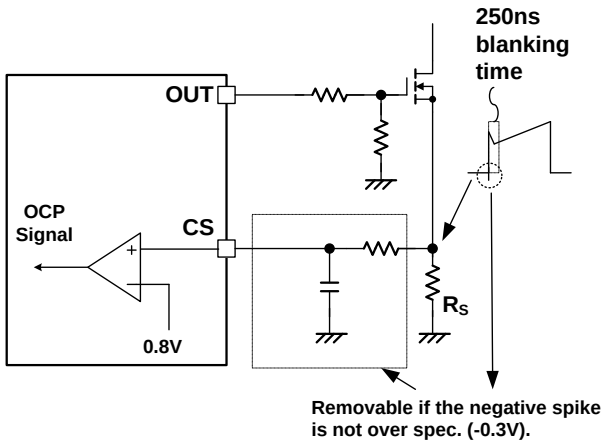


Fig. 13

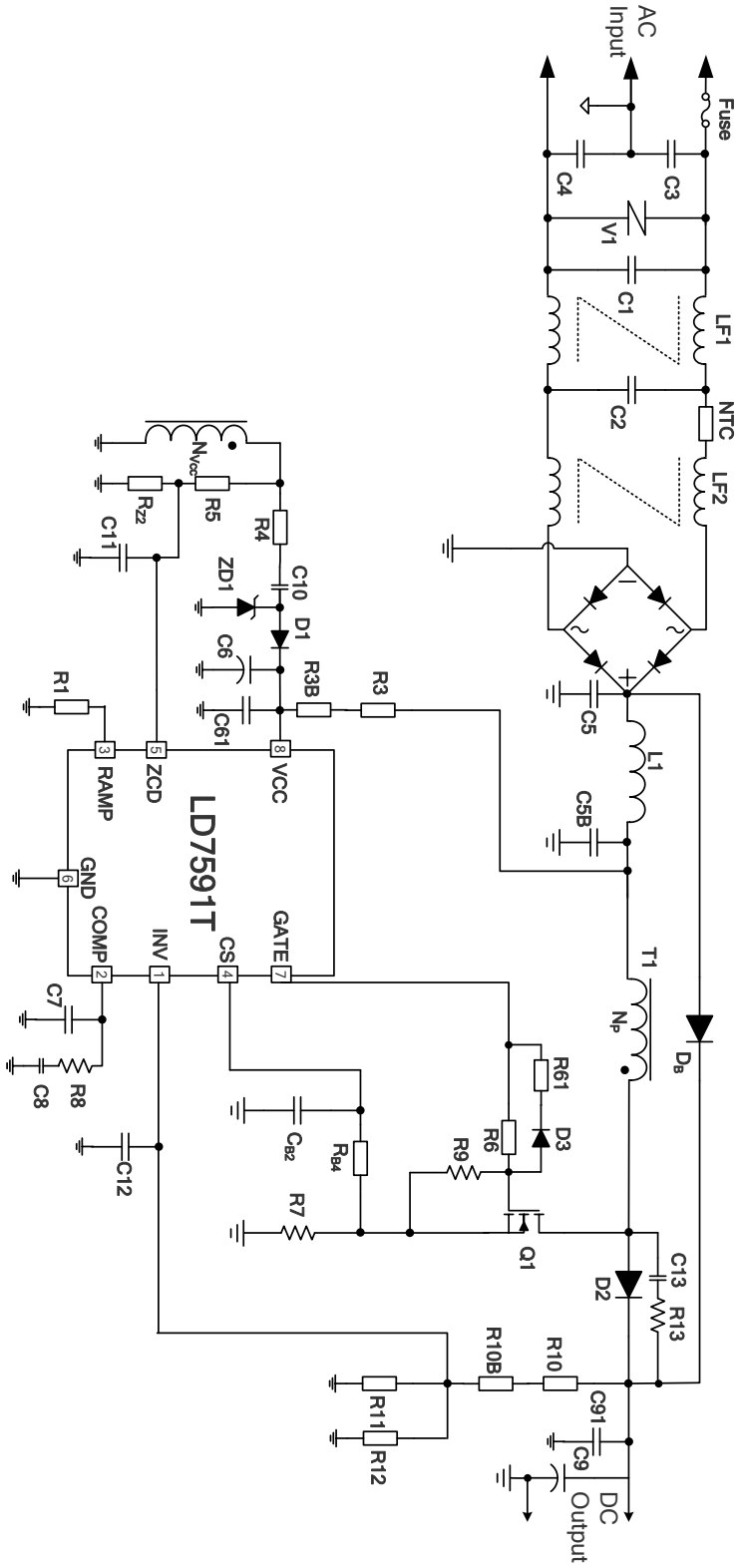
Fault Protection

There are several critical protections integrated in the LD7591T to prevent the power supply or adapter from being damaged. Those damages usually come from open or short condition on the pins of LD7591T.

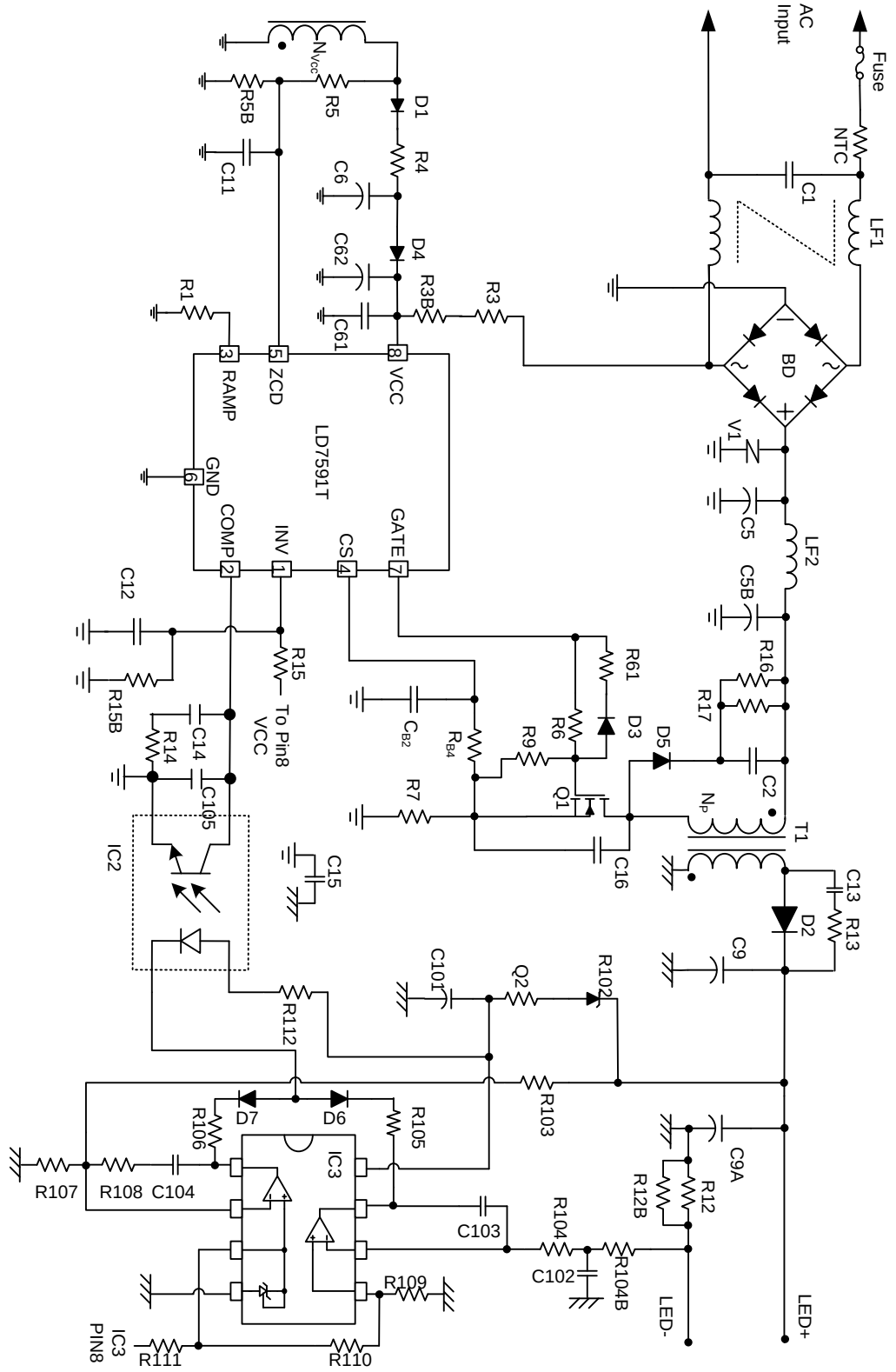
Under the conditions listed below, the gate output will turn off immediately to protect the power circuit ---

1. Ramp pin short to ground
2. Ramp pin floating
3. CS pin floating

Reference Application Circuit --- 400V/100W (90~264V_{AC})

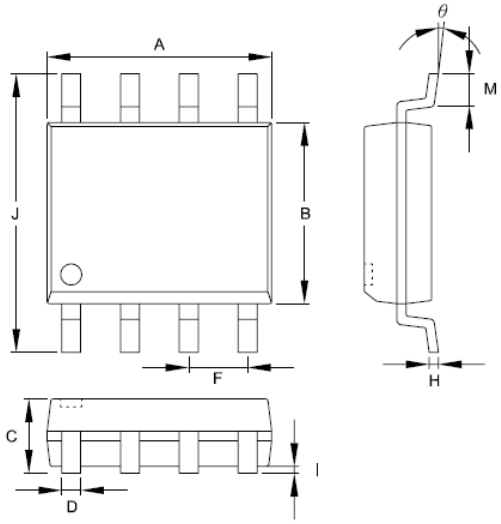


Reference Application Circuit --- LED -42V/350mA (90~264V_{AC})



Package Information

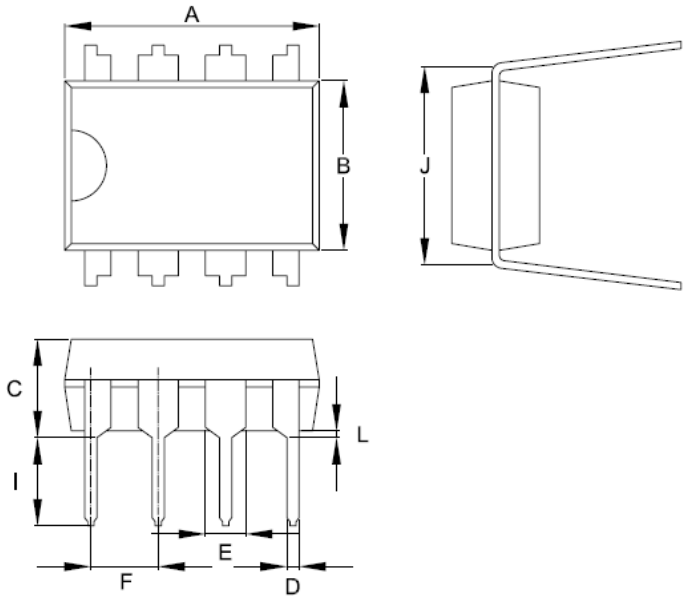
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change notice
00	11/9/2012	Original specification