Transition-Mode PFC Controller with Fault Condition Protection

REV. 00

General Description

The LD7592S is a voltage mode PFC controller operating on transition mode, with several integrated functions of protection, such as OVP, OCP, and brown-in protection. It reduces the components counts and is available in a SOP-8 or DIP-8 package. Those make it an ideal design for low cost applications.

It provides functions of low startup current, over voltage protection, open feedback protection, disable function, over current protection, under voltage lockout and integrated LEB of current sensing. The LD7592S adopts transition mode for power factor correction and realizes high efficiency and a low switching noise by zero current switching.

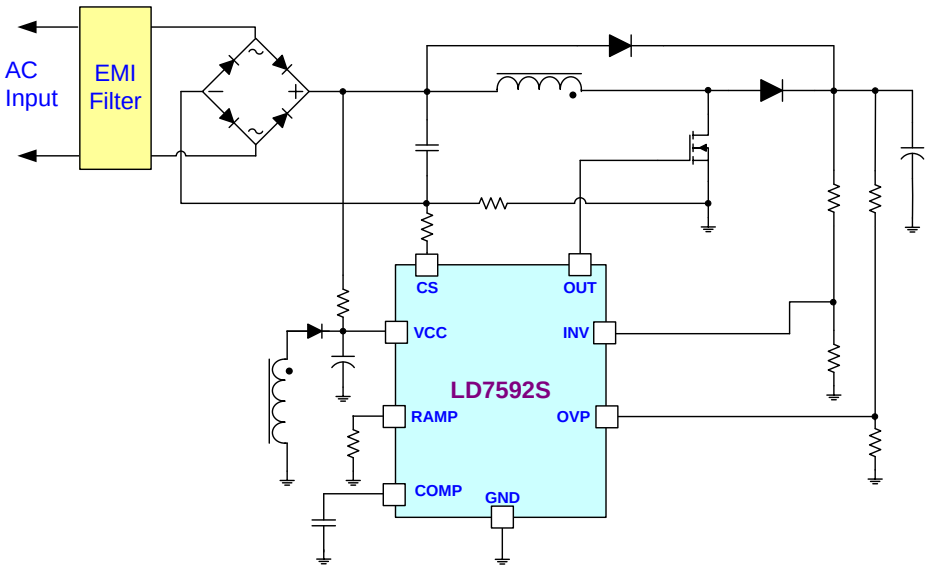
Features

- Transition Mode of PFC Pre-Regulator
- Voltage Mode Control
- Programmable Maximum on-time
- ZCD Auxiliary Winding is Unnecessary
- Low Startup Current (<1μA)
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS pin
- VCC OVP (Over Voltage Protection) on VCC pin
- VO OVP (Over Voltage Protection) on INV pin
- Bulk Cap OVP (Over Voltage Protection) on OVP pin
- OCP (Cycle by Cycle Current Limit)
- 900/-1200mA Driving Capability
- Internal OTP (Over Temperature Protection)

Applications

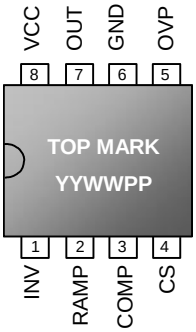
- Adaptor of Output above 75W.
- LCD TV Power Supply

Typical Application for Boost PFC



Pin Configuration

SOP-8 & DIP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package		Top Mark	Shipping
LD7592S GS	SOP-8	Green package	LD7592SGS	2500 /tape & reel
LD7592S GN	DIP-8	Green package	LD7592SGN	3600 /tube /carton

The LD7592S is RoHs compliant/ green packaged.

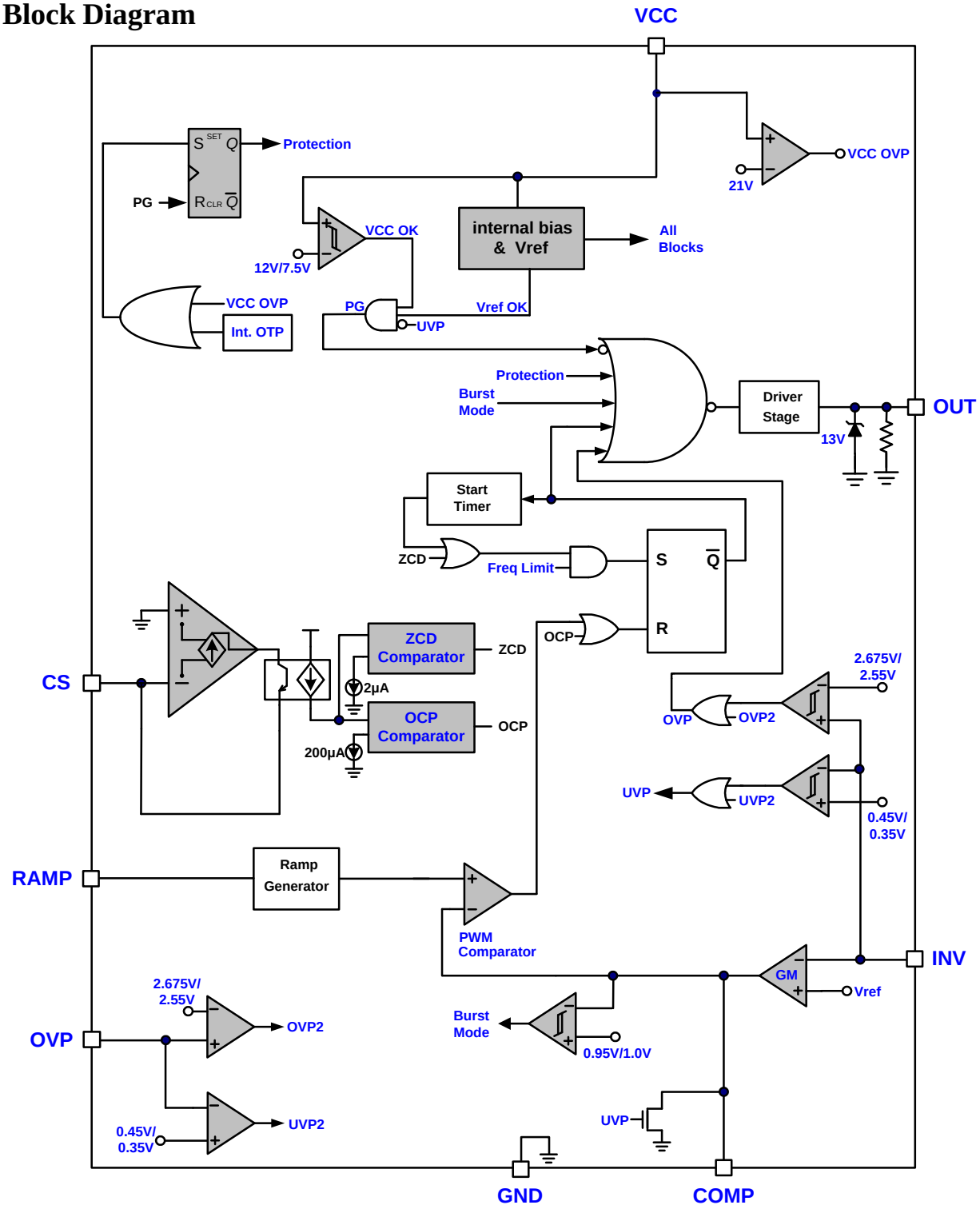
Protection Mode

Part number	V_{CC_OVP}	OCP	OVP	OTP
LD7592S	Auto-Restart	Cycle by Cycle	Auto-Recovery	Auto-Restart

Pin Descriptions

Pin	NAME	FUNCTION
1	INV	Output voltage feedback control
2	RAMP	Ramp generator, connecting a resistor to GND pin to set the saw tooth signal
3	COMP	Output of the error amplifier for voltage loop compensation to achieve stable
4	CS	This pin is the input of the zero current detection and over-current protection comparator
5	OVP	The OVP pin is used to detect PFC output over-voltage when the INV pin information is not correct
6	GND	Ground
7	OUT	Gate drive output to drive the external MOSFET
8	VCC	Supply voltage pin

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V ~ 30V
OUT	Note2~ VCC +0.3V
COMP, INV, RAMP, OVP	-0.3V ~ 6V
CS	Note1~ 6V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8, θ_{JA})	160°C/W
Package Thermal Resistance (DIP-8, θ_{JA})	100°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	250mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	400mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V
Gate Output Current	900mA/-1200mA

Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note1: When CS pin voltage < 0V ~ -2V, the current of I_{CS} must be < 100mA in 10ms.

Note2: When OUT pin voltage < -0.3V ~ -1V, the current of I_{OUT} must be < 20mA in 1μs and the pin has to connect a resistor with the values between 47Ω~150Ω in series.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
VCC pin capacitor	22	47	μF
COMP pin capacitor	0.1	4.7	μF
RAMP pin resistor	4.7	100	kΩ
Current Sense resistor, R_{SNS}	1		kΩ

Electrical Characteristics

(VCC=14.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current	VCC<UVLO (on)	I_{CC_ST}	0		1	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V	I_{CC_OP1}	0.25	0.5	0.75	mA
	V_{COMP}=3V	I_{CC_OP2}	1	3	5	mA
	V_{CC_OVP}	I_{CC_OPA1}	0.15	0.4	0.45	mA
	V_{INV}=0V	I_{CC_OPA2}	30	100	170	μA
UVLO (off)		V_{CC_OFF}	7	7.5	8	V
UVLO (on)		V_{CC_ON}	11.0	12.0	13.0	V
VCC OVP Level		V_{CC_OVP}	19.5	21	22.5	V
Error Amplifier (COMP Pin)						
Feedback Input Voltage		V_{REF}	2.465	2.500	2.535	V
Transconductance		gm_{COMP}	100	140	180	μmho
Output Sink Current	V_{INV}=V_{REF}+0.05 V	I_{SINK1}	5	7	9	μA
	V_{INV}=V_{REF}+1V	I_{SINK2}	160	200	240	μA
Output Source Current	V_{INV}=V_{REF}-0.05V	$I_{SOURCE1}$	-5	-7	-9	μA
	V_{INV}=V_{REF}-1V	$I_{SOURCE2}$	-160	-200	-240	μA
Output Upper Clamp Voltage	V_{INV}=V_{REF}-0.1V	$VCOMP_{CLAMP}$	4.8	5	5.2	V
Zero Duty Threshold VCOMP		V_{ZDC}	0.9	0.95	1.0	V
Zero Duty Hysteresis	Hysteresis	V_{ZDCH}	20	50	80	mV
Maximum Frequency		FMAX	240	300	360	kHz
INV pin						
Output Brown IN		UVP	0.4	0.45	0.5	V
	Hysteresis	$UVP_{\_HYS}$	0.05	0.1	0.15	V
OVP Trip Level		OVP	2.62	2.675	2.73	V
OVP pin						
Output Brown IN		UVP2	0.4	0.45	0.5	V
	Hysteresis	$UVP2_{\_HYS}$	0.05	0.1	0.15	V
OVP Trip Level		OVP2	2.62	2.675	2.73	V
Current Sensing (CS Pin)						
Current Sense Input Threshold Voltage		OCP		200		μA
Input bias current	V_{CS}=0V~1V	I_{BIAS1}		1		μA
Leading Edge Blanking Time		LEB		350		ns
CS Lower Clamp Voltage	ICS=-2mA	VCS_{CLAMP}	0		-0.3	V
ZCD Trip Level		I_{ZCD}		2		μA

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Maximum ON-Time, Ton-max (RAMP Pin)						
Maximum On Time Voltage	R_{RAMP}=40.5K	VRAMP	2.7	2.900	3.1	V
Maximum On Time Programming	R_{RAMP}=40.5K	T_{RAMP1}	20	24	28	μs
Maximum On Time	R_{RAMP}≥100K	$T_{RAMPMAX1}$	36	40	44	μs
Minimum OFF-Time						
Minimum OFF-Time		T_{MIN}		1		μs
Gate Drive Output (OUT Pin)						
Output Low Level	VCC=12V, I_{SINK}=20mA	V_{OL}			0.5	V
Output High Level	VCC=12V, I_{SOURCE}=20mA	V_{OH}	9		12	V
Output High Clamp Level	VCC=18V	V_{O_CLAMP}	11	13	15	V
Rising Time	VCC=12V, CL=1000pF	T_r		75		ns
Falling Time	VCC=12V, CL=1000pF	T_f		75		ns
Starter						
Start Timer Period		T_{START}	45	50	55	μs
Internal OTP						
OTP Trip level	*	T_{INOTP}		140		°C
OTP Hysteresis	*	T_{INOTP_HYS}		30		°C

*: Guaranteed by design.

Typical Performance Characteristics

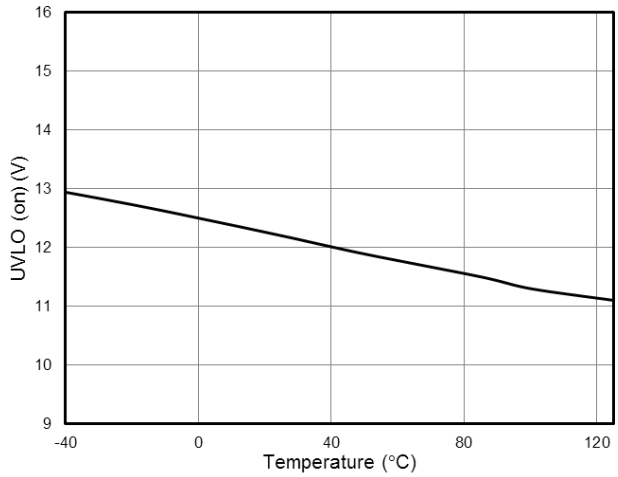


Fig. 1 UVLO (on) vs. Temperature

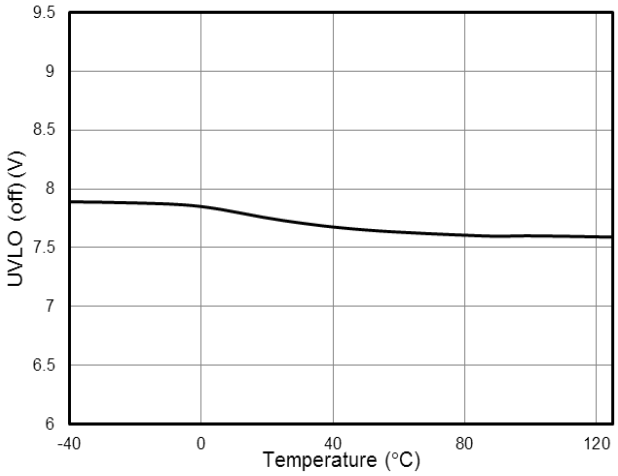


Fig. 2 UVLO (off) vs. Temperature

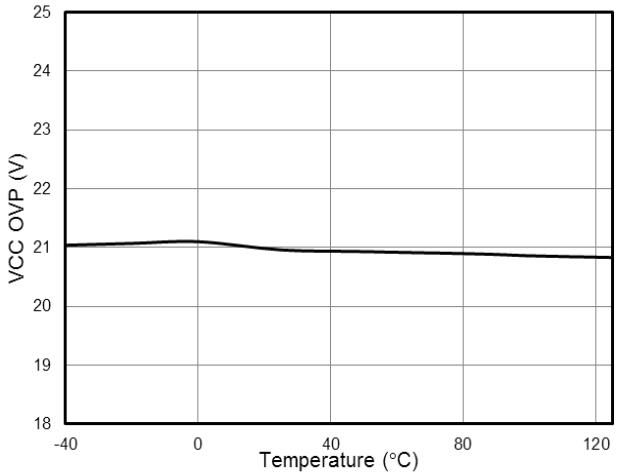


Fig. 3 VCC OVP vs. Temperature

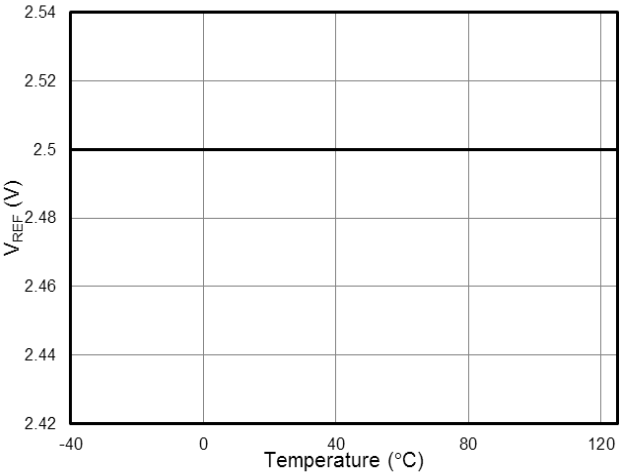


Fig. 4 V_{REF} vs. Temperature

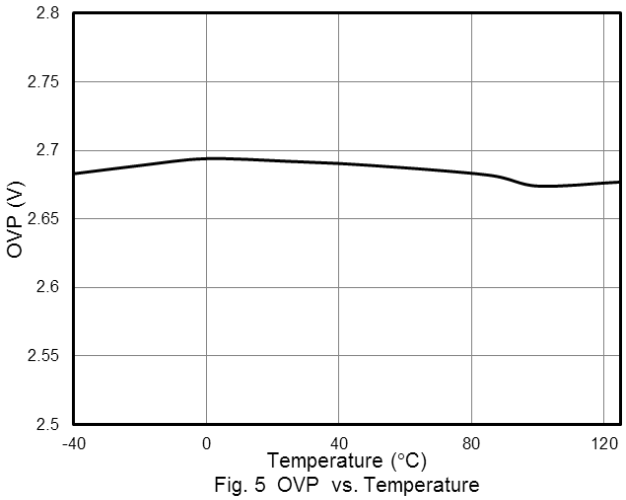


Fig. 5 OVP vs. Temperature

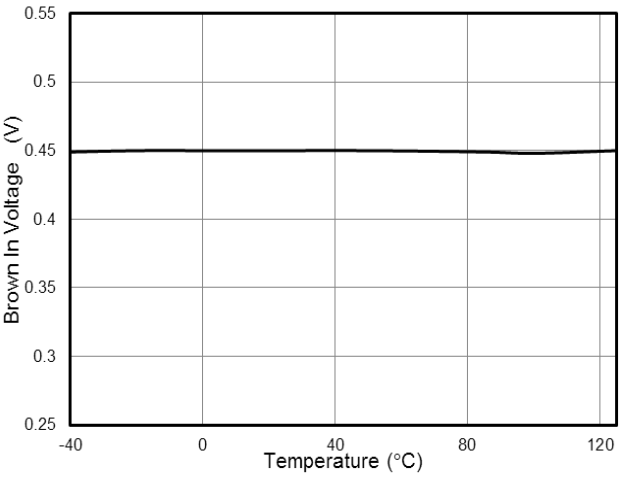


Fig. 6 Brown In Voltage vs. Temperature

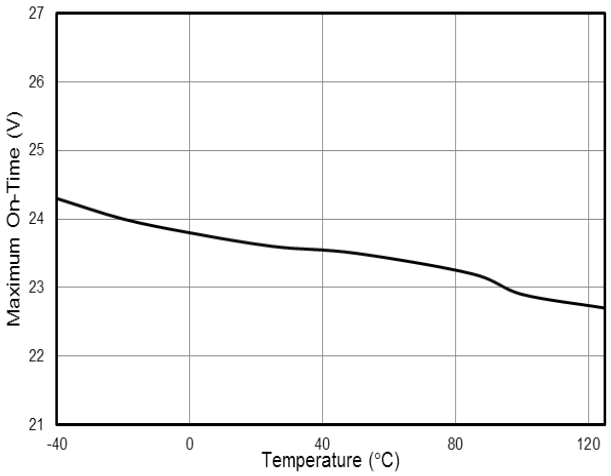


Fig. 7 Maximum On-Time vs.Temperature

Application Information

Operation Overview

The LD7592S is an excellent voltage mode PFC controller. It meets the IEC61000-3-2 requirement and is intended for the use in those pre-regulator that demands low power harmonics distortion. It integrates more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD7592S PFC controllers and further to drive the power MOSFET. As shown in Fig. 8, a hysteresis is built in to prevent the shutdown from the voltage dip during start up. The turn-on and turn-off threshold level are set at 12.0V and 7.5V, respectively.

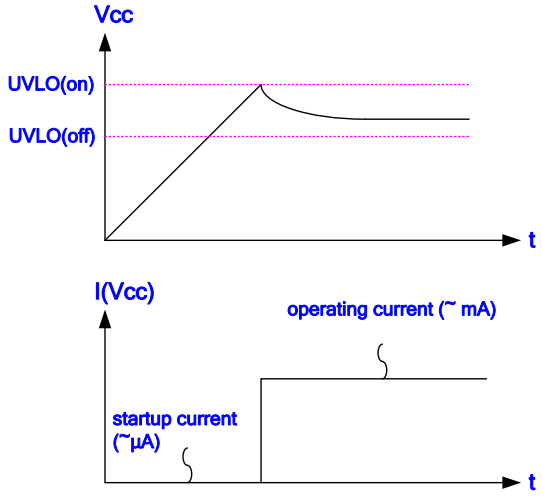


Fig. 8

Startup Current and Startup Circuit

The typical startup circuit to generate the LD7592S VCC is shown in Fig. 9. During the startup transient, the VCC is lower than the UVLO threshold. Thus, there is no gate pulse produced from LD7592S to drive power MOSFET. Therefore, the current through R1 will provide the startup current and charge the capacitor C1. Whenever the VCC voltage is high enough to turn on the LD7592S and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the PFC choke. Lower startup current requirement on the PFC controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD7592S is only 1μA. If a higher resistance value of R1 is chosen, it usually takes more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

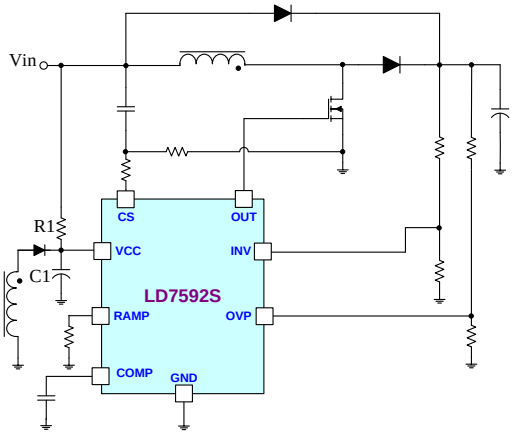


Fig. 9

Output Voltage Setting

The LD7592S monitors the output voltage signal at INV pin through a resistor divider pair Ra and Rb. A transconductance amplifier is used instead of the conventional voltage amplifier. The transconductance amplifier (voltage controlled current source) aids the implementation of OVP and disables function. The output current of the amplifier changes according to the voltage difference of the inverting and non-inverting input of the amplifier. The output voltage of the amplifier is compared with the internal ramp signal to generate the turn-off signal. The output voltage is determined by the following relationship.

$$V_O = 2.5V(1+\frac{Ra}{Rb})\ (V)$$

Where Ra and Rb are top and bottom feedback resistor values (as shown in the Fig. 10).

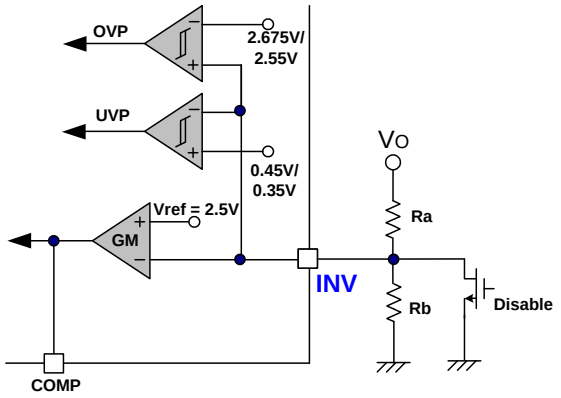


Fig. 10

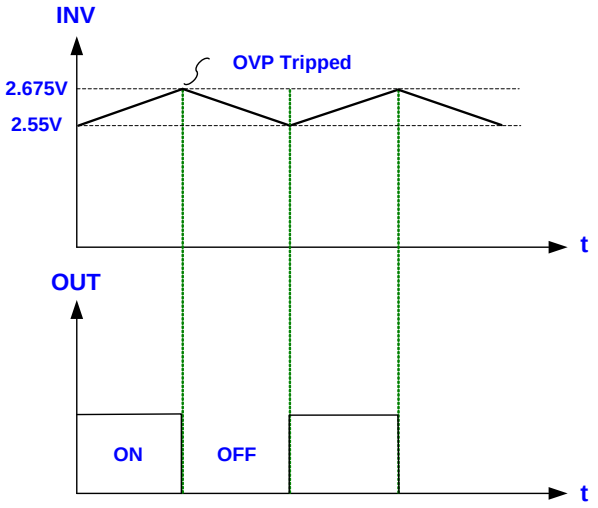


Fig. 11

OVP and Disable Function

To prevent the over voltage on the output capacitor from the fault condition, LD7592S is implemented with an OVP function on INV pin. Whenever the INV pin voltage is higher than OVP, the output gate drive circuit will be shutdown simultaneously to stop the switching of the power MOSFET until the INV pin down to (OVP - $OVP_{\_HYS}$). The OVP function in LD7592S is an auto-recovery type protection. The Fig. 11 shows its operation.

The disable comparator disables the operation of the LD7592S when the voltage of the inverting input is lower than 0.35V and there is 100mV hysteresis. An external small signal MOSFET can be used to disable the IC. If the IC is disabled, operating current decreases below 100μA to reduce power consumption.

The LD7592S can provide additional over voltage protection on OVP pin. If INV pin voltage divider gets damaged, then OVP pin can supply additional over voltage protection. If OVP pin protection is not required, the OVP pin can connect with INV pin.

Brown in Protection

The LD7592S features brown-in function on INV pin. The built-in comparator detects the V_{INV} and V_{OVP} voltage condition, as shown in Fig. 12. This is done as follows:

1. The INV and OVP voltage is higher than UVP
2. The COMP voltage rise up and higher than V_{ZDC}

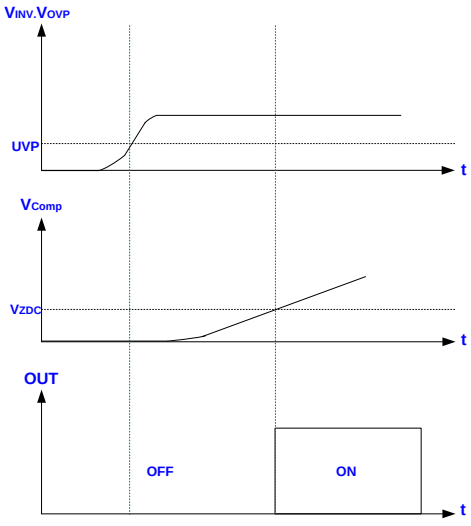


Fig. 12

Ramp Generator Block

The output of the gm error amplifier and the output of the ramp generator block are compared to determine the MOSFET on time, as shown in Fig. 13. The slope of the

ramp is determined by an external resistor connected to the RAMP pin. The voltage of the RAMP pin is 2.9V and the slope is proportional to the current flowing out of the RAMP pin. The internal ramp signal has a 1V offset; therefore, the drive output will be shut down if the voltage of the COMP pin is lower than 0.95V. The programmed on-time will be at its maximum when the COMP pin pulls high. The COMP pin open voltage is about $VComp_{clamp}$. According to the slope of the internal ramp, the maximum on-time can be programmed. The necessary maximum on-time will be achieved depending on the boost inductor, lowest AC line voltage, and maximum output power. The resistor value should be designed properly. The maximum on-time can be obtained from below

$$T_{ON-Time(MAX)} = \frac{R_{RAMP}}{1.6875 \cdot 10^{9}} \text{ (Sec.)}$$

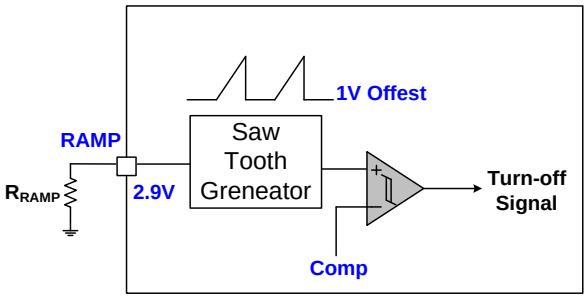


Fig. 13

Output Drive Stage

An output stage of a CMOS buffer, with typical 900mA/-1200mA driving capability, is incorporated to drive a power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage is higher than 13V.

Current Sensing and Leading-Edge Blanking

The typical voltage mode of PFC controller feedbacks the voltage signals to close the control loop and achieve regulation. The LD7592S detects the inductor current from the CS pin, which is for the pulse-by-pulse current limit. The maximum current threshold of the current sensing pin is set at 200μA. From above, the inductor peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{200\mu A \cdot R_{SNS}}{R_{CS}} \text{ (A)}$$

A 350ns leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike.

Zero Current Detection

In DCM operation, the inductor current decreases during MOSFET off. The current, ISNS, sourced from CS pin also decreases simultaneously. When I_{SNS} becomes smaller than I_{ZCD}, MOSFET will be turned on again. Since the voltage of CS pin is clamped at 0V, I_{SNS} can be shown below, as shown in Fig. 14 and Fig. 15.

$$I_{SNS} = \frac{-V_{CSA}}{R_{SNS}} \text{ (A)}$$

Because of the inrush current of the boost topology, VCSA will be a large negative voltage at startup. Meanwhile, LD7592S may be not enabled so the clamping circuit of CS pin does not work. ISNS flowing through the ESD diode of CS pin can only be limited by RSNS. To prevent too large ISNS from damaging LD7592S, the resistance value of RSNS is recommended to be larger than 1kΩ.

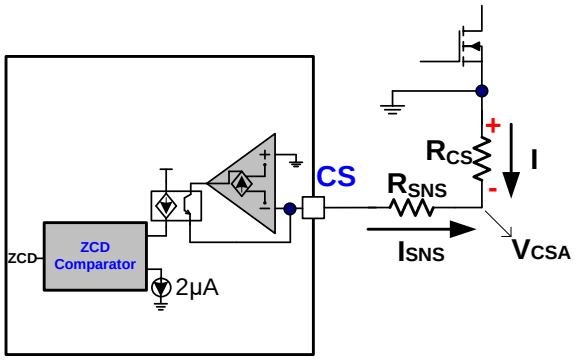


Fig. 14

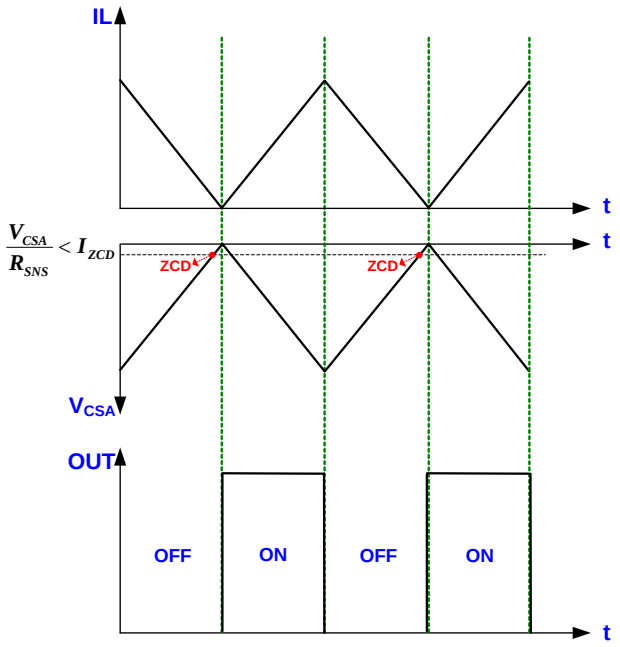


Fig. 15

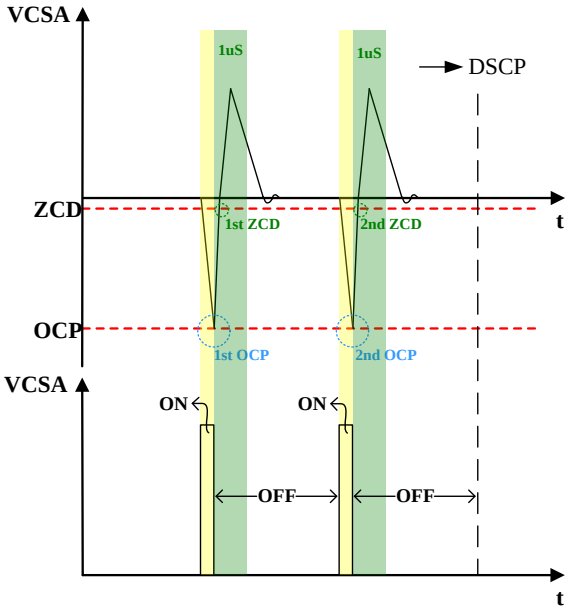


Fig. 16

Diode Short Circuit Protection (DSCP)

The method that the LD7592S judges the logic of DSCP is described briefly as follows. LD7592S will detect VCSA voltage, when trigger two consecutive (OCP + ZCD) level, the DSCP protection will be activated, and immediately to protect, as shown in Fig. 16.

$$\begin{cases} \text{OCP, during } T_{on} \\ \text{ZCD, within } 1\mu s \text{ of } T_{off} \end{cases}$$

Fault Protection

There are several critical protections integrated in the LD7592S to prevent the power supply or adapter from being damaged. Those damages usually come from open or short condition on the pins of LD7592S.

Under the conditions listed below, the gate output will turn off immediately to protect the power circuit:

1. Ramp pin short to ground
2. Ramp pin floating
3. CS pin floating

GND Layout Suggestion

LD7592S GND layout suggestion is shown in Fig. 17. The LD7592S current sense loop is very important for the stable operation.

The following are GND layout suggestion for LD7592S:

1. The current sense loop path should be minimized, as shown in Fig. 17 (red line loop).
2. The current sense resistor R_{CS} should be placed close to IC GND.

3. The VCC capacitor C_{VCC} should be placed close to VCC pin.

4. Signal ground will be separated, as shown in Fig. 17 (green area).

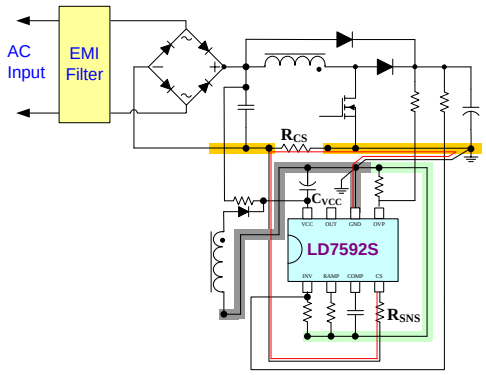
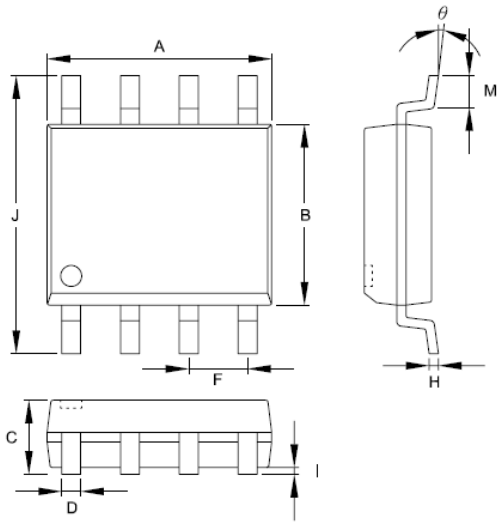


Fig. 17

Package Information

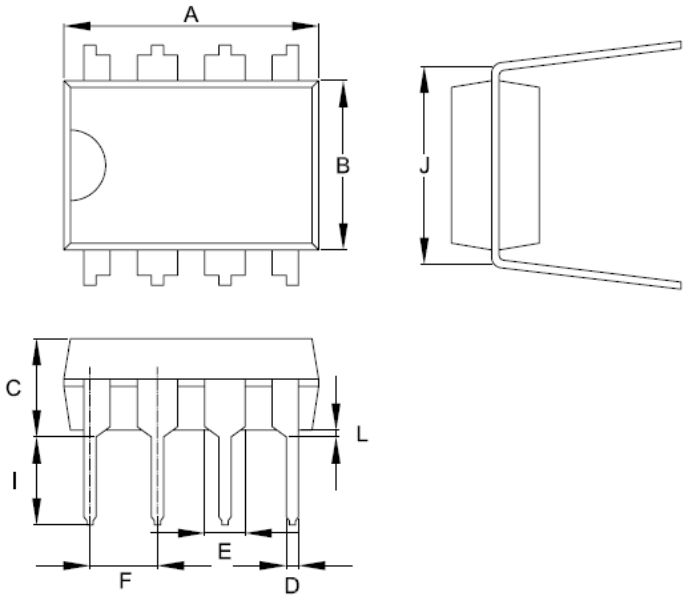
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	05/08/2018	Original Specification