

Low Power Off-line Switcher

P03 (Internal use only)

General Description

The LD7660J integrated a 600V power MOSFET and a current mode PWM controller in a DIP-8 package. It's operating at fixed frequency of 65 kHz. It provides important functions needed for a low output power applications such as leading-edge blanking of the current sensing, internal slope compensation, and green-mode power-saving operation under light load or no load condition. This highly integrated device provides the users a high efficiency, low external component counts, and low cost solution for low power adaptor or charger applications.

The special green-mode control is not only to achieve the low power consumption but also to offer a non-audible-noise operation when the LD7660J is operating under light load or no load condition.

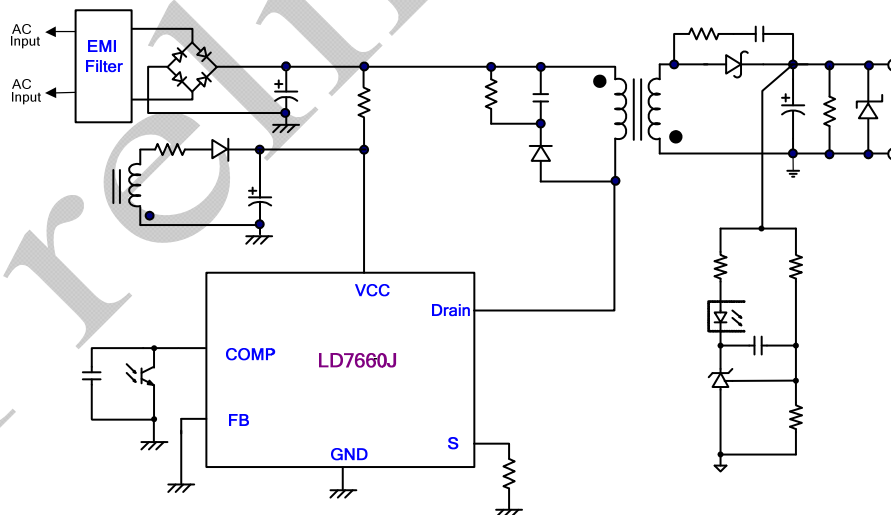
Features

- Built-in 600V/1A Power MOSFET
- Secondary-side/Primary-side feedback control
- Switching Frequency at 65KHz
- Fixed Internal Frequency Trembling
- Built-in Load Regulation Compensation
- Built-in Slope Compensation with 75% max duty-cycle
- Low Startup Current (<20 μ A)
- Current Mode Control with Cycle-by-Cycle Current Limit
- Non-audible-noise Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- OVP (Over Voltage Protection) on Vcc
- OLP (Over Load Protection)

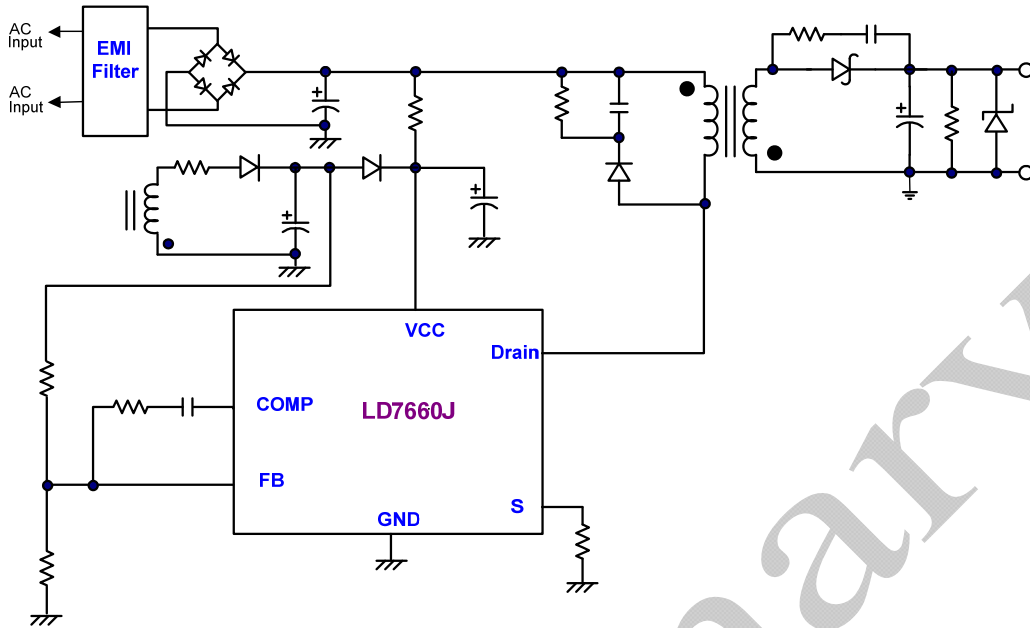
Applications

- Switching AC/DC Adaptor
- LCD TV or PC Standby Power

Typical Application



Secondary-side Feedback



Primary-side Feedback

Pin Configuration

DIP- 8 (TOP VIEW)



YY: Year code (D: 2004, E: 2005...)
WW: Week code
PP: Production code

Ordering Information

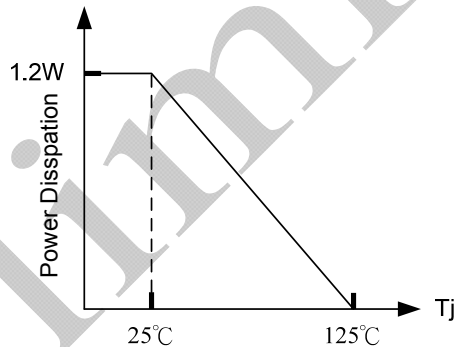
Part number	Package	Fosc	Top Mark	Shipping
LD7660J GN	DIP-8/Green Package	65KHz	LD7660J GN	3600/ Tube/ Carton

Pin Descriptions

PIN (DIP-8)	NAME	FUNCTION
1	FB	Inverting input to the error amplifier
2	COMP	Output of the error amplifier for voltage compensation
3	GND	Ground of the controller
4	S	Source of internal power MOSFET, connecting a sense resistor to ground.
5	Drain	Drain terminal of the internal power MOSFET
6	Drain	Drain terminal of the internal power MOSFET
7	NC	Not Connected
8	VCC	Power supply to Vcc

Output Power Table & De-rating Curve

Product	Drain Current	Rds(on) *	230VAC \pm 15% **		90~264VAC **	
			Adapter	Open frame	Adapter	Open frame
LD7660J	1.3A	9 Ω	7W	10W	5W	8W



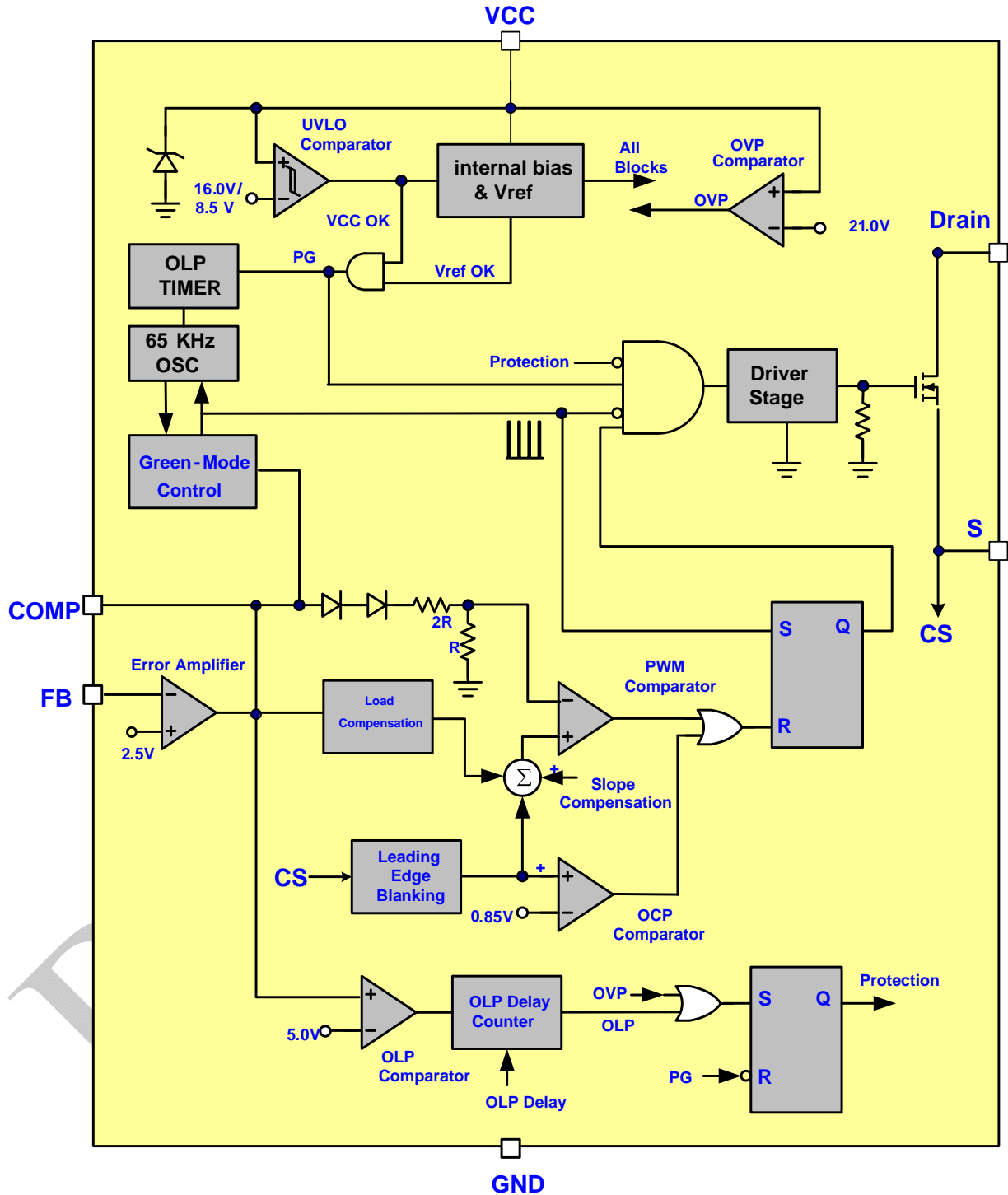
*Typ.@25°C, Vcc=10V Drain Current=0.65A

**Calculated maximum Input Power Rating at Ta=25°C

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage Vcc	10	20	V
Start-up capacitor	2.2	22	μ F
Start-up resistor	1.0	4.7	M Ω

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC.....	30V
FB, S.....	-0.3 ~7V
Drain.....	-0.3~600V
Continuous drain current ¹ , T _c =25°C	
LD7660J.....	1.3A
Single Pulse Avalanche Energy ²	
LD7660J.....	30mJ
Total Power Dissipation of DIP-8, T _a =25°C.....	1.2W
Package thermal resistance (DIP-8)	
θ_{JA}	80°C/W ³
θ_{JA}	20°C/W ⁴
θ_{JC}	35°C/W ⁵
Maximum Junction Temperature.....	150°C
Operating Junction Temperature Range.....	-40°C to 125°C
Operating Ambient Temperature Range.....	-40°C to 85°C
Storage Temperature Range.....	-50°C to 150°C
Lead temperature (DIP-8, Soldering, 10sec).....	260°C
ESD Voltage Protection, Human Body Model.....	2.5 KV
ESD Voltage Protection, Machine Model.....	250 V

1. Repetitive rating: Pulse width limited by maximum junction temperature
2. L=60mH, I_{DS}=1A, V_{DD}=150V, Starting T_J=25°C
3. w/o heat-sink, under natural convection
4. Infinite cooling Condition, refer to SEMI G30-88
5. Measured on the package top surface

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not limited.

Electrical Characteristics

Electrical Characteristics for Control Section (Ta=25°C, V_{CC}=15.0V, unless otherwise stated,)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC} Pin)					
Startup Current			10	20	μA
Operating Current (with 1nF load on OUT pin)	V _{FB} =3.0V, V _{COMP} =0V		2.3		mA
	R _{COMP-FB} =20K, R _{FB-GND} =100K, OUT=1nF		3.6		mA
	V _{COMP} opened		0.65		mA
	I _{ovp}		0.7		mA
UVLO (off)		7.5	8.5	9.5	V
UVLO (on)		15.0	16.0	17.0	V
OVP Level		20	21	22	V
Error Amplifier					
Feedback Input Voltage	FB=COMP	2.475	2.5	2.525	V
Load Compensation Current	R _{COMP-FB} =20K, V _{CS} =0.7V (linear type)		-27		μA
Output Sink Current	V _{FB} =2.7V, Comp=1.1V		6		mA
Output Source Current	V _{FB} =2.3V, Comp=4.9V		-2.75		mA
High-level Output Voltage	V _{FB} =2.3V, R _L =15 KΩ to GND	5.5			V
Low-level Output Voltage	V _{FB} =2.7V, R _L =15 KΩ to GND			1.2	V
Current Sensing (CS Pin)					
Maximum Input Voltage, V _{CS(off)max.}		0.80	0.85	0.90	V
Leading Edge Blanking Time	V _{COMP} >2.4V		225		nS
Slope Compensation	0~max. duty (Linearly)		300		mV
Input impedance		1			MΩ
Delay to Output			100		nS
Oscillator for Switching Frequency					
Frequency	COMP=4.5V	60	65	70	KHz
Green Mode Frequency	COMP=4.5V		21		KHz
Trembling Frequency	COMP=4.5V		± 4.5		KHz
Modulation Frequency			180		Hz
Temp. Stability	(-40°C ~105°C)			5	%
Voltage Stability	(V _{CC} =11V-19.5V)			1	%
Comp Pin Detect					
Green Mode Threshold Voltage			2.50V		V
Burst Mode Threshold Voltage			1.6		V
Gate Drive Output (OUT Pin)					
Maximum duty			75		%

OLP (Over Load Protection)					
OLP Trip Level	V_{COMP} (OLP)		5		V
OLP Delay Time			107		mS

Preliminary

Electrical Characteristics

(Ta=25°C, VCC=15.0V, unless otherwise stated,)

Electrical Characteristics for MOSFET

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage					
Breakdown Voltage BV _{DSS}	COMP=0V, I _D =250μA, T _J =25°C	600			V
Breakdown Voltage Temperature Coefficient	I _D =250μA, COMP=0V		0.6		V/°C
Drain Current					
Drain Current	V _{CC} =15V, 25°C			1.3	A
	V _{CC} =15V, 100°C			0.8	
Drain Leakage Current					
Drain-Source Leakage Current	V _{DS} =600V, COMP=0V, T _J =25°C	0		1	μA
	V _{DS} =480V, COMP=0V, T _J =125°C	0		10	
Drain on Resistance					
Drain to S pin On-Resistance	I _D =0.65A; V _{CC} =10V; T _J =25°C		7.5	9	Ω

Typical Performance Characteristics

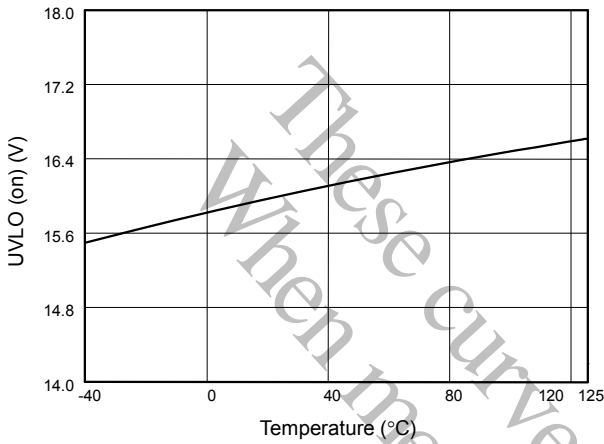


Fig. 1 UVLO (on) vs. Temperature

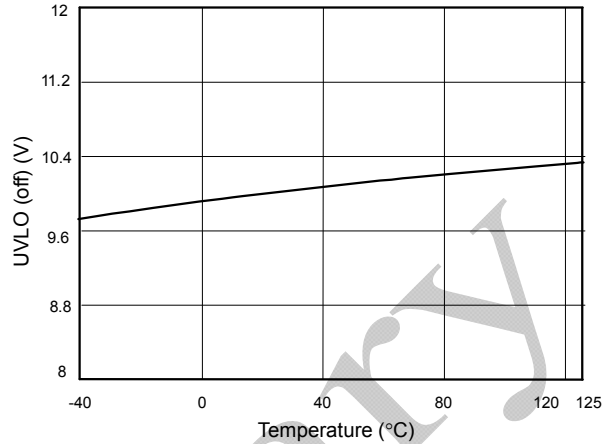


Fig. 2 UVLO (off) vs. Temperature

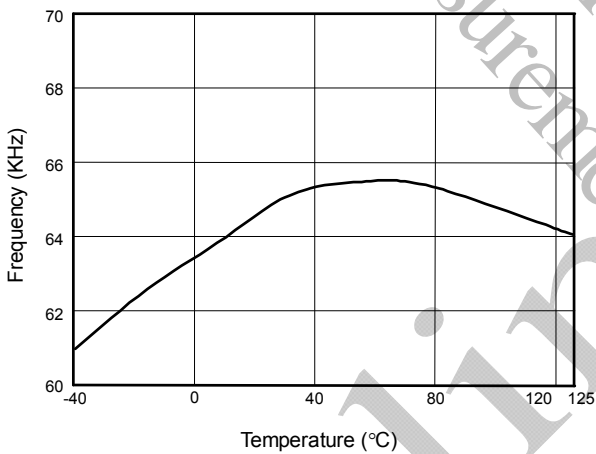


Fig. 3 Frequency vs. Temperature

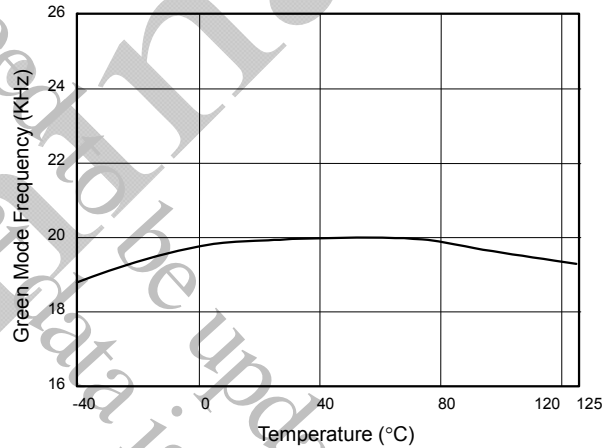


Fig. 4 Green Mode Frequency vs. Temperature

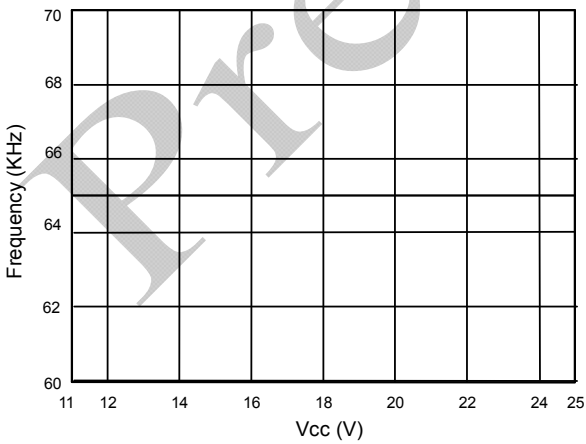


Fig. 5 Frequency vs. Vcc

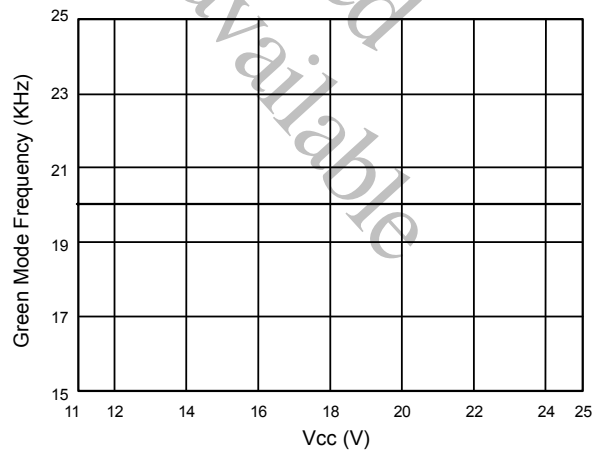


Fig. 6 Green Mode Frequency vs. Vcc

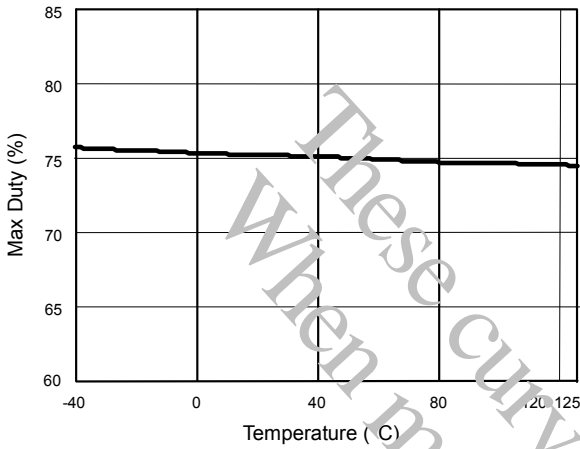


Fig. 7 Max Duty vs. Temperature

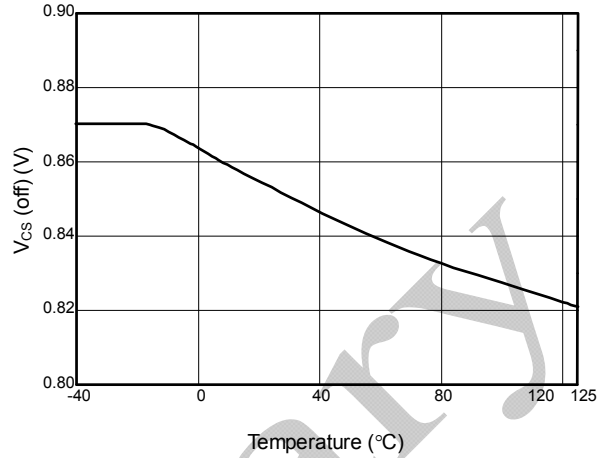


Fig. 8 V_{CS} (off) vs. Temperature

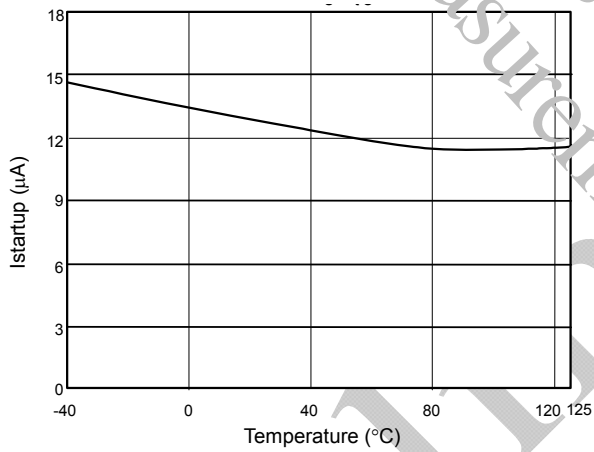


Fig. 9 Startup Current (I_{start-up}) vs. Temperature

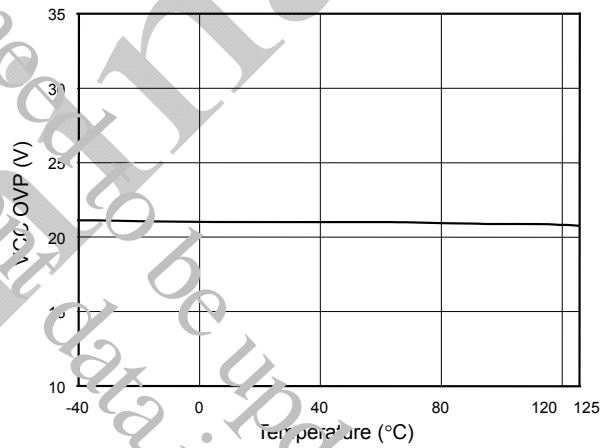


Fig. 10 V_{CC} OVP vs. Temperature

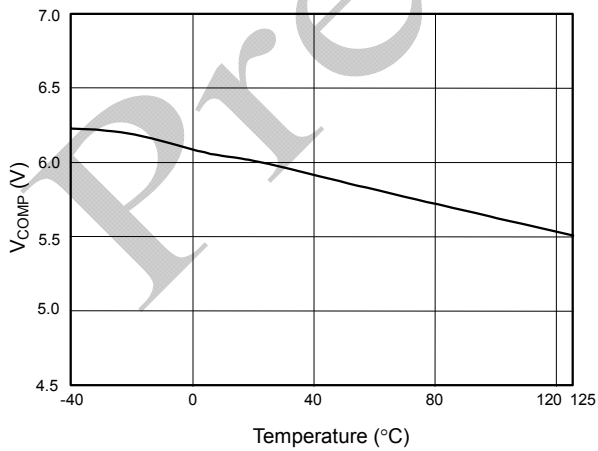


Fig. 11 V_{COMP} open loop voltage vs. Temperature

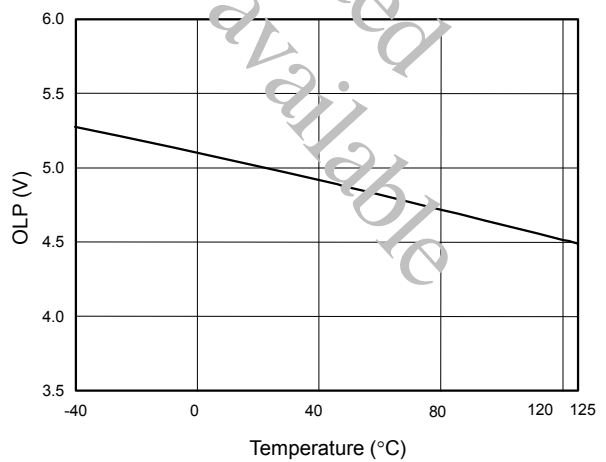


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

The LD7660J is an excellent primary side feedback controller. It meets the green-power requirement and is intended for the use in those modern switching power suppliers and linear adaptors that demand higher power efficiency and power-saving. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD7660J PWM controllers and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.0V and 10.0V, respectively.

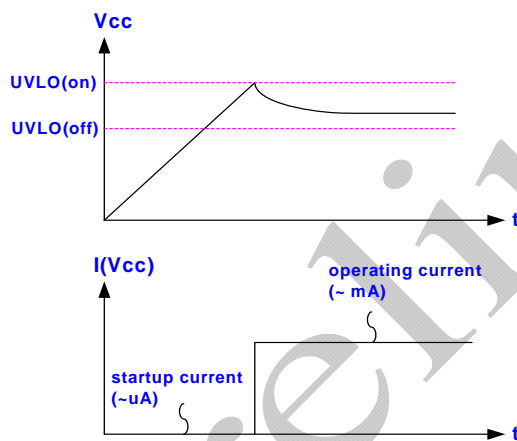


Fig. 13

Output Voltage setting

The LD7660J monitors the auxiliary fly-back signal at FB pin through a resistor divider pair R_a and R_b . An error signal representing the difference between the voltage at FB and the reference voltage is generated by LD's patent-pending circuitry, which is then integrated by the Error Amplifier and used to control switching duty cycle.

The output voltage is determined by the following relationship. For improving the output voltage accuracy, the transformer leakage inductance should be reduced as much as possible.

Where R_a and R_b are top and bottom feedback resistor value, N_s and N_a are the turns of transformer secondary and auxiliary (as shown in the figure 14).

The load regulation and line regulation for primary side feedback control is sensitive to the structure of transformer. For getting good regulation and efficiency, the sandwich structure by two secondary separate parallel layer windings surrounding primary winding is recommended.

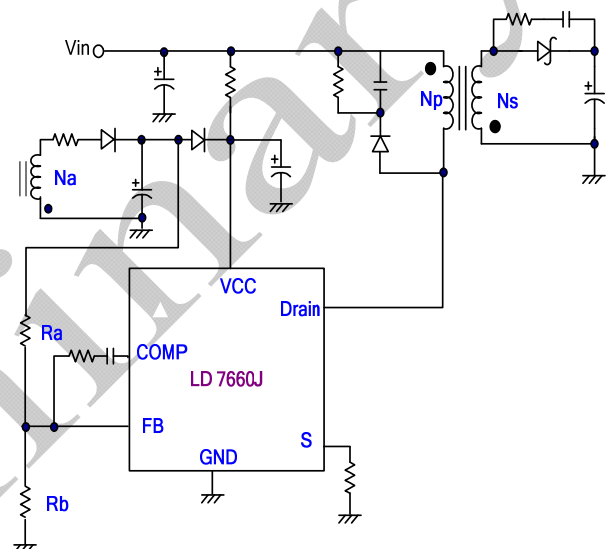


Fig.14

Startup Current and Startup Circuit

The typical startup circuit to generate the LD7660J V_{cc} is shown in Fig. 15. During the startup transient, the V_{cc} is lower than the UVLO threshold thus there is no gate pulse produced from LD7660J to drive power MOSFET. Therefore, the current through R_1 will provide the startup current and to charge the capacitor C_1 . Whenever the V_{cc} voltage is high enough to turn on the LD7660J and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer. Lower startup current requirement on the PWM controller will help to increase the value of R_1 and then reduce the power consumption on R_1 . By using CMOS process and the special circuit design, the maximum startup current of LD7660J is only $20\mu A$.

If a higher resistance value of R1 is chosen, it usually takes more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

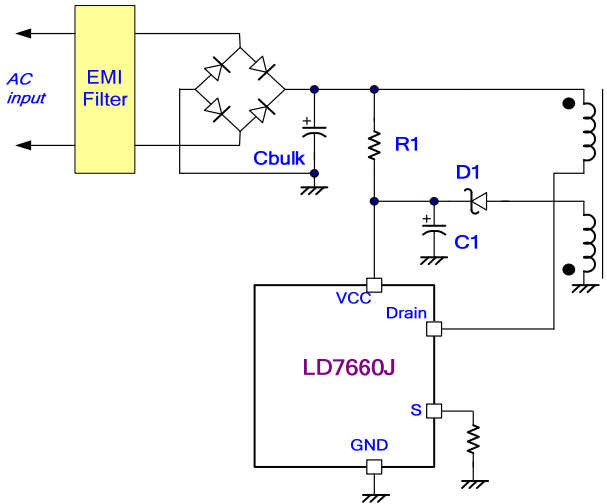


Fig. 15

Current Sensing, load compensation, and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD7660J detect the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A 225nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike.

This pin also acts as load compensation's duty. The built-in dependent sink current source is proportional to the peak value of Vcs. This current sinks from FB pin to get an increment on Vcc and induces the secondary output voltage rising to offset the voltage drop on circuit. Its equation is $I_{fb} = 6 + V_{cspk} * 30$ (uA)

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 300mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7660J is limited to 75% to avoid the transformer saturation.

Oscillator and Switching Frequency

The switching frequency of LD7660J is fixed as 65KHz internally to provide the optimized operations by considering the EMI performance, thermal treatment, component sizes and transformer design.

Internal Slope Compensation

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in higher than 50% of the duty-cycle. As UC384X, It takes slope compensation from injecting the ramp signal of the RT/CT pin through a coupling capacitor. It therefore requires no extra design for the LD7660J since it has integrated it already.

Frequency Trembling

The LD7660J are implemented with an adjustable modulating frequency for trembling function which provides the power supply designers to choose the optimized EMI performance and lowest system cost. The Trembling frequency is fixed internally between $\pm 4.5KHz$ which is incorporated with the 65KHz switching frequency.

Dual-Oscillator Green-Mode Operation

There are many different topologies has been implemented in different chips for the green-mode or power saving requirements such as "burst-mode control", "skipping-cycle mode", "variable off-time control "...etc. The basic operation theory of all these approaches intended to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reduce the switching frequency. What LD7660 use to implement the power-saving operation is Leadtrend Technology's own IP.

OVP (Over Voltage Protection) on Vcc

The V_{GS} ratings of the nowadays power MOSFETs are often limited up to max. 30V. To prevent the V_{GS} from the fault condition, LD7660J is implemented with an OVP function on Vcc. Whenever the Vcc voltage is higher than the OVP

threshold voltage, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(on).

The Vcc OVP function in LD7660J is an auto-recovery type protection. The figure 18 shows its operation.

On the other hand, if the OVP condition is removed, the Vcc level will get back to normal level and the output will automatically return to the normal operation.

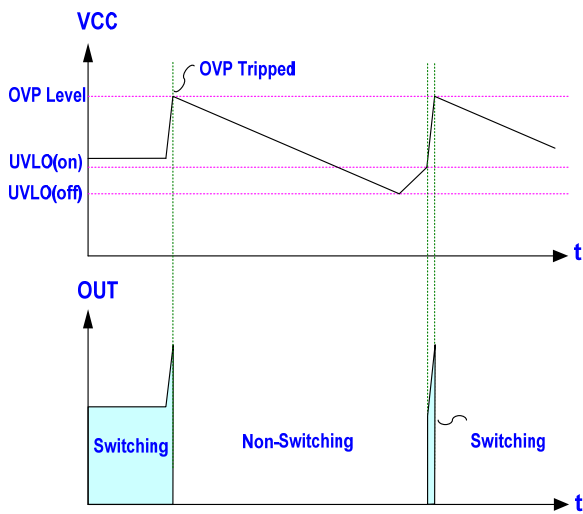


Fig. 18

Over Load Protection (OLP)

To protect the circuit from being damaged under over load condition or short condition, a smart OLP function is implemented in the LD7660J. The figure 19 shows the waveforms of the OLP operation. In this case, the feedback system will force the voltage loop proceed toward the saturation and then pull up the voltage on COMP pin (VCOMP). Whenever the VCOMP trips up to the OLP threshold 5V and stays longer than the OLP delay time (30mS), the protection will activate and then turn off the gate output to stop the switching of power circuit. By such

protection mechanism, the average input power can be reduced to very low level so that the component temperature and stress can be controlled within the safe operating area.

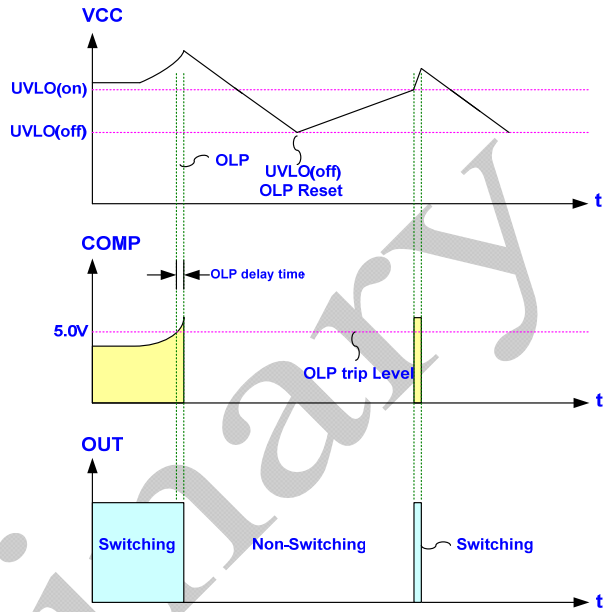


Fig. 19

Fault Protection

There are several critical protections were integrated in the LD7660J to prevent the power supply or adapter had being damaged. Those damages usually come from open or short condition on the pins of LD7660J.

Under the conditions listed below, the MOSFET will be turned off immediately to protect the power circuit.

1. COMP pin short to ground
2. S pin floating

Reference Application Circuit --- 6W (5V/1.2A)

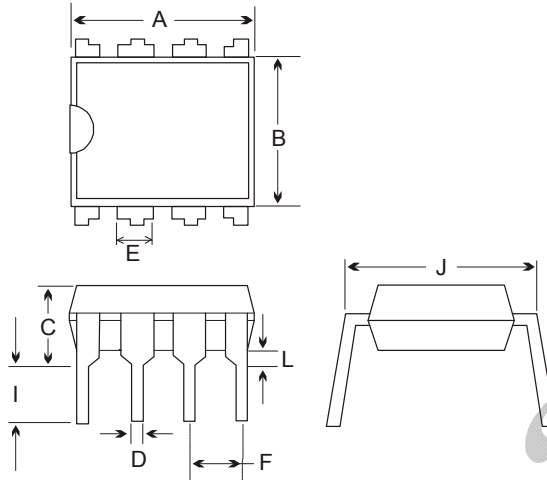
BOM

P/N	Component Value	Note
R1	NC	1206
R2	NC	1206
R3A	22Ω, 1206, 1%	
R3B	22Ω, 1206, 1%	
R4	0Ω, 0805, 1%	
R5	1.5MΩ, 1206, 1%	
R6	1.5MΩ, 1206, 1%	
R9A	200KΩ, 1206, 1%	
R9B	200KΩ, 1206, 1%	
R10	1KΩ, 1206, 1%	
R12	24KΩ, 0805, 1%	
R15	NC, 1206	
R16	2.0Ω, 2W	
R17	NC	0805
R19	NC	0805
R20	NC	0805
R21	NC	0805
R22	51Ω, 1206, 1%	
R23	100KΩ, 0805, 1%	
R24	100KΩ, 0805, 1%	
J1	0Ω, 0805, 1%	
J2	0Ω, 0805, 1%	
L1	Leadtrend's Design	UU9.8
L2	Leadtrend's Design	
L3	Leadtrend's Design	
T1	Leadtrend's Design	EE19-162J

P/N	Component Value	Note
C1	2200pF, 1000V, 1206	
C2	2.2μF, 50V	5*11(LZG)
C3	10μF, 400V	10*16 (TY)
C4	10μF, 400V	10*16 (TY)
C6	2200pF, 1000V, 1206	
C7	1000μF, 10V	8*20
C9	2470μF, 16V	
C10	0.1μF, 25V, 0805	
C11	2.2μF, 50V	5*11(LZG)
C13	0.33μF, 25V, 0805	
C14	NC, 0805	
C15	NC, 0805	
C16	NC, 0805	
CX1	0.1μF, X-cap	
CY1	2200pF, Y-cap, class1	
D1	PS102R	
D2	PS1010R	
D3A	5A/40V	SB540
D4	1N4148	
BR1	1A, 600V	DI106
IC1	LD7660J, DIP8	Leadtrend
F1	250V, T2A	Walter
U1	NC	
IC2	NC	

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	-----	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.14
J	7.366	8.255	0.29	0.325
L	0.381	-----	0.015	-----

Important Notice

Leadtrend Technology Inc. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
P01	01/21/09	Preliminary Release
P02	04/28/09	Revise some typing error
P03	05/21/09	Revise fsw

Preliminary