High Voltage Green-Mode PWM Controller with Over Temperature Protection

Rev. 01

General Description

The LD7750B integrates several functions of protections, and EMI-improved solution in a tiny package to minimize the component counts and the circuit space.

The device provides functions of low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. Also, the LD7750B features more protections like OLP (Over Load Protection), OVP (Over Voltage Protection), and OTP (Over Temperature Protection) to prevent the circuit being damaged under abnormal conditions.

Furthermore, the LD7750B features frequency swapping to depress radiation noise, providing an excellent solution for EMI filter design.

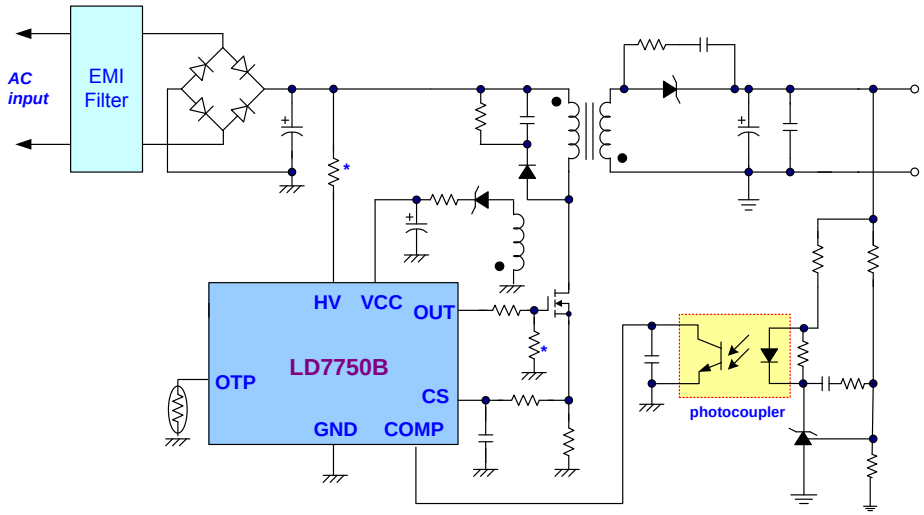
Features

- High-Voltage (500V) Startup Circuit
- Current Mode Control
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Frequency swapping
- Internal Slope Compensation
- Internal Over Current Protection
- OVP (Over Voltage Protection) on Vcc
- OLP (Over Load Protection)
- External OTP through a NTC
- 500mA Driving Capability

Applications

- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

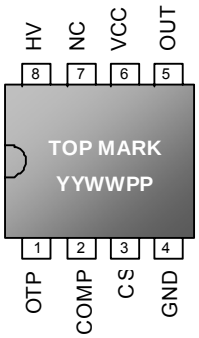
Typical Application



Pin Configuration

SOP-7 (TOP VIEW)

SOP-8/ DIP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package		Top Mark	Shipping
LD7750B GS	SOP-8	Green package	LD7750BGS	2500 /tape & reel
LD7750B GR	SOP-7	Green package	LD7750BGR	2500 /tape & reel
LD7750B GN	DIP-8	Green package	LD7750BGN	3600 /tube /Carton

The LD7750B is ROHS compliant and Halogen Free.

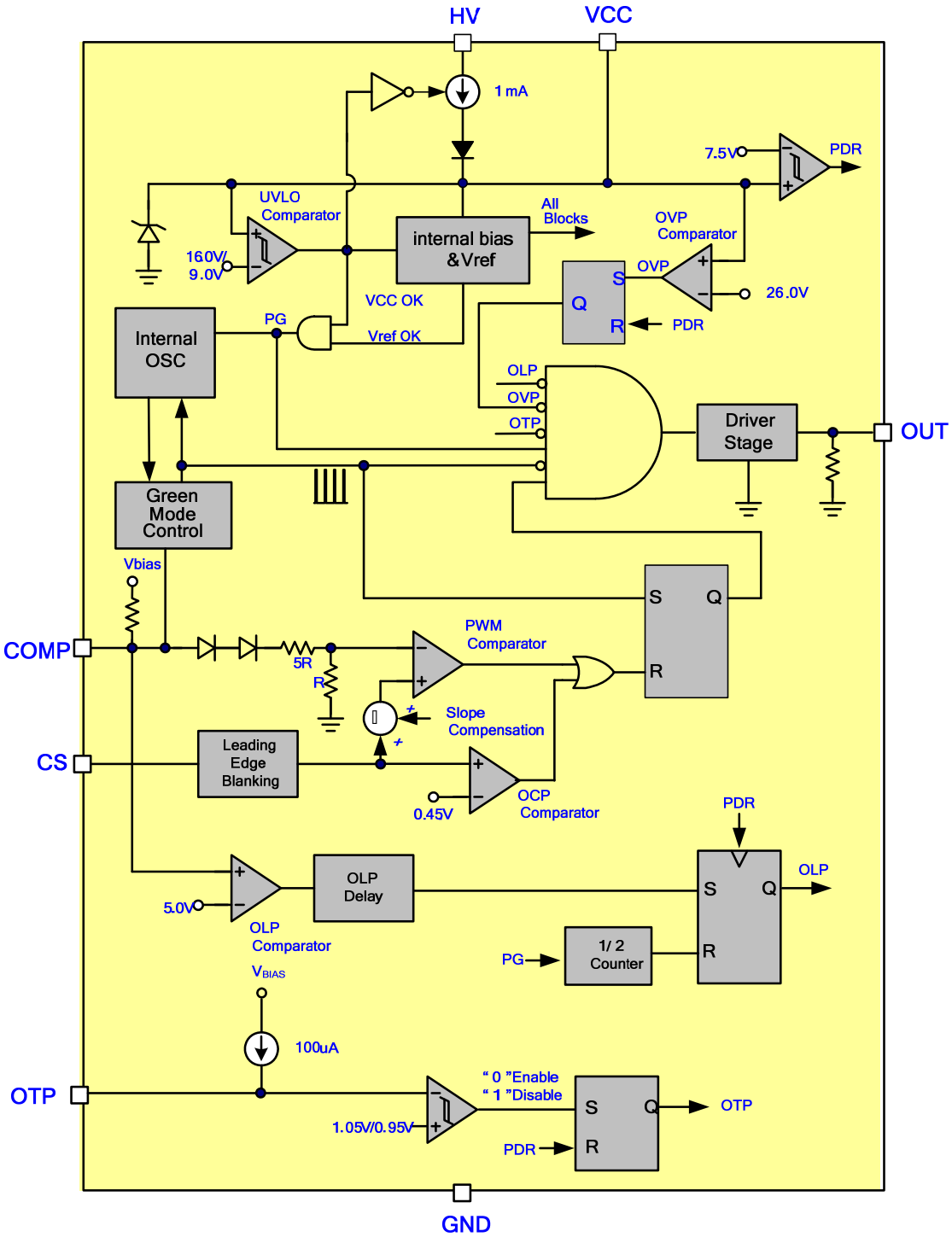
Protection Mode

Part number	Switching Freq.	VCC OVP	OLP	OTP Pin
LD7750B	100kHz	Latch	Auto recovery	Latch

Pin Descriptions

SOP-8, DIP-8	SOP-7	NAME	FUNCTION
1	1	OTP	Pulling this pin below 0.95V will shutdown the controller to enter latch mode until the AC power-on recycles. Connecting a NTC between this pin and ground will achieve OTP protection function. Let this pin float to disable the latch protection.
2	2	COMP	Voltage feedback pin. Connecting a photo-coupler with it can close control loop and achieve regulation.
3	3	CS	Current sense pin, for sensing the MOSFET current.
4	4	GND	Ground.
5	5	OUT	Gate drive output to drive the external MOSFET.
6	6	VCC	Supply voltage pin.
7		NC	Unconnected Pin.
8	8	HV	Connect this pin to a positive terminal of bulk capacitor to provide the startup current for the controller. When Vcc voltage trips the UVLO(on), this HV loop will be turned off to reduce the power loss on the startup circuit.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V 30V
High-Voltage Pin, HV	-0.3V~500V
COMP,OTP, CS	-0.3 ~7V
OUT	-0.3 ~Vcc+0.3
Maximum Junction Temperature	150°C
Operating Ambient Temperature	-40°C to 85°C
Operating Junction Temperature	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-7, SOP-8)	160°C/W
Package Thermal Resistance (DIP-8)	100°C/W
Power Dissipation (SOP-7, SOP-8)	400mW
Power Dissipation (DIP-8)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV Pin)	2.5KV
ESD Voltage Protection, Machine Model	250V

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage Vcc	10	24	V
Comp Pin Capacitor	4.7	100	nF

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)					
High-Voltage Current Source	V_{CC}< UVLO(on), HV=500V	0.5	1.0	1.5	mA
Off-State Leakage Current	V_{CC}> UVLO(off), HV=500V			35	μA
Supply Voltage (Vcc Pin)					
Startup Current		200	320	400	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		1.1		mA
	V_{COMP}=3V,		2.7		mA
	OLP tripped		0.61		mA
	OVP tripped, VCC=OVP		0.70		mA
UVLO (off)		8.0	9.0	10.0	V
UVLO (on)		15.0	16.0	17.0	V
OVP Level		25.0	26.0	27.0	V
Voltage Feedback (COMP Pin)					
Short Circuit Current	V_{COMP}=0V	0.2	0.26	0.32	mA
Open Loop Voltage	COMP pin open	5.5	6.0		V
Green Mode Threshold VCOMP			2.75		V
Zero Duty			1.6		V
Current Sensing (CS Pin)					
Maximum Input Voltage,Vcs_off		0.42	0.45	0.48	V
Leading Edge Blanking Time			250		ns
Input impedance		1			MΩ
Delay to Output			100		ns

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency					
Frequency		94.0	100.0	106.0	kHz
Green Mode Frequency			25		kHz
Swapping Frequency			±6		kHz
Temp. Stability	-20°C~85°C		5		%
Voltage Stability	(V_{CC}=11V-25V)			1	%
OTP Pin Latch Protection (OTP Pin)					
OTP Pin Source Current		92	100	108	μA
Turn-On Trip Level		1.00	1.05	1.10	V
Turn-Off Trip Level		0.90	0.95	1.0	V
De-latch VCC Level	(PDR, Power Down Reset)		7.5		V
Gate Drive Output (OUT Pin)					
Output Low Level	V_{CC}=15V, Io=20mA			1	V
Output High Level	V_{CC}=15V, Io=20mA	9			V
Rising Time	Load Capacitance=1000pF		100	160	ns
Falling Time	Load Capacitance=1000pF		30	60	ns
Max.Duty			75		%
OLP (Over Load Protection)					
OLP Trip Level		4.8	5.0	5.2	V
OLP Delay Time			83		ms
Soft Start Duration					
Soft Start Duration			4		ms
On Chip OTP (Internal Over Temperature Protection, Auto-Recovery)					
OTP Level			140		°C
OTP Hysteresis			30		°C

Typical Performance Characteristics

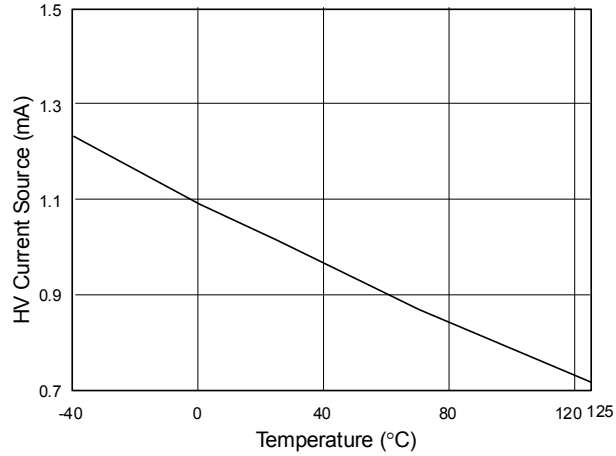


Fig. 1 HV Current Source vs. Temperature (HV=500V, Vcc=0V)

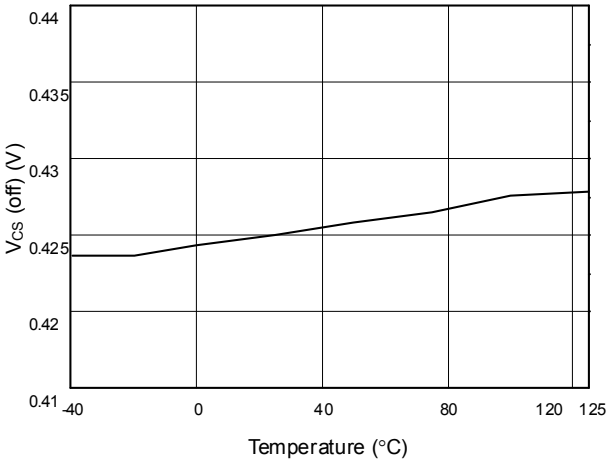


Fig. 2 V_{CS} (off) vs. Temperature

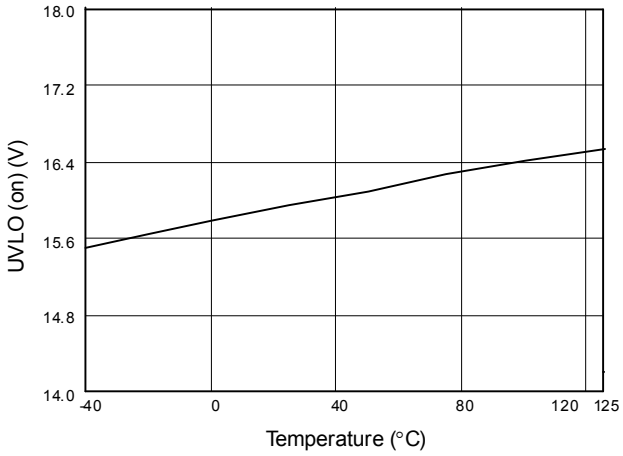


Fig. 3 UVLO (on) vs. Temperature

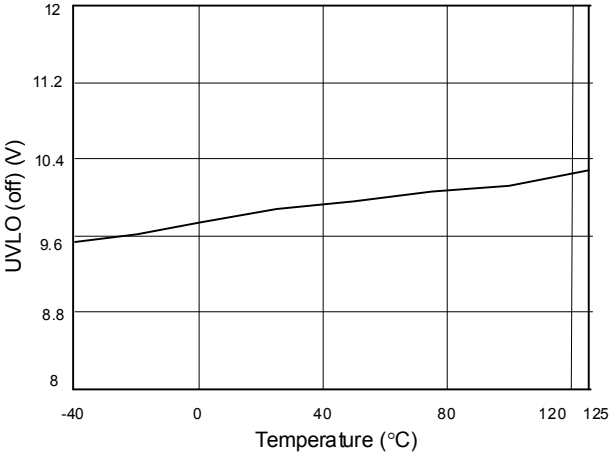


Fig. 4 UVLO (off) vs. Temperature

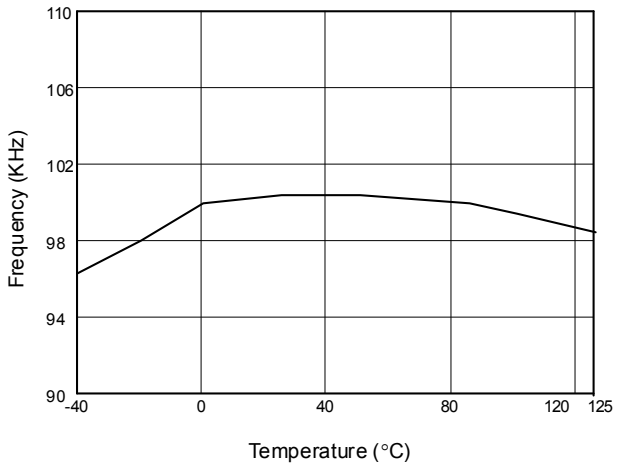


Fig. 5 Frequency vs. Temperature

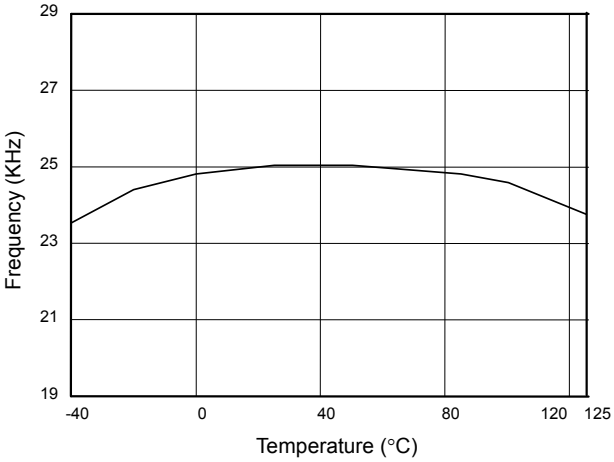


Fig. 6 Green Mode Frequency vs. Temperature

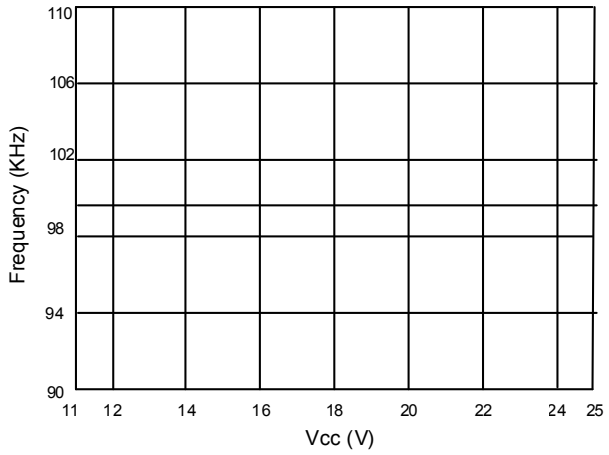


Fig. 7 Frequency vs. Vcc

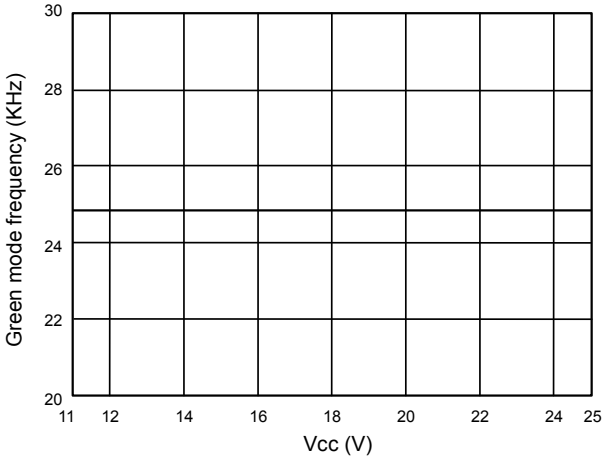


Fig. 8 Green mode frequency vs. Vcc

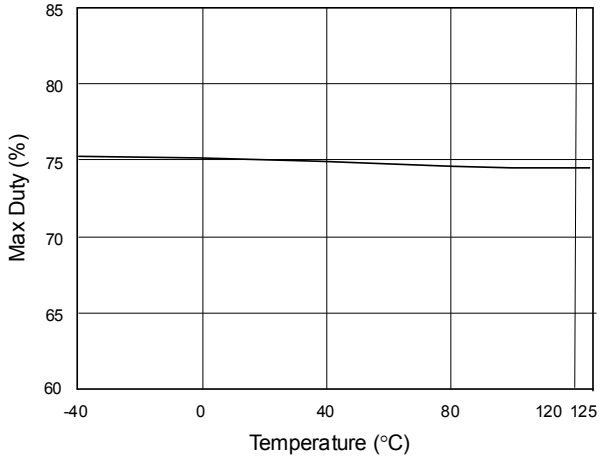


Fig. 9 Max Duty vs. Temperature

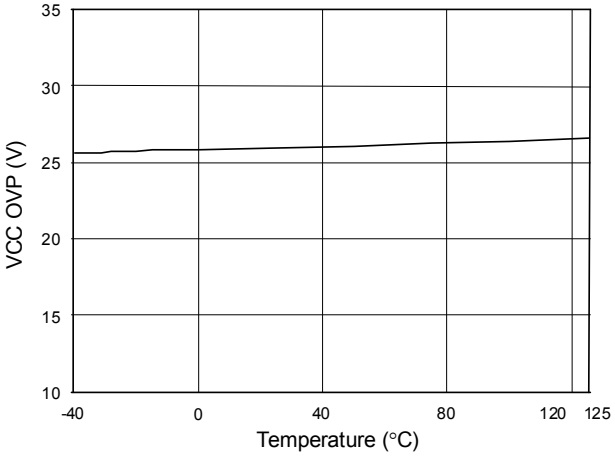


Fig. 10 VCC OVP vs. Temperature

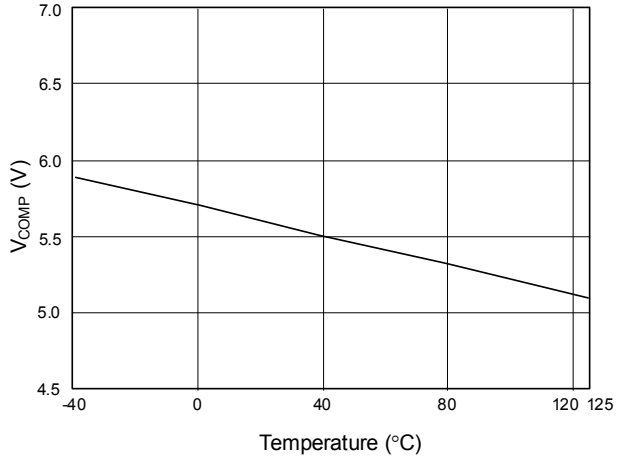


Fig. 11 V_{COMP} open loop voltage vs. Temperature

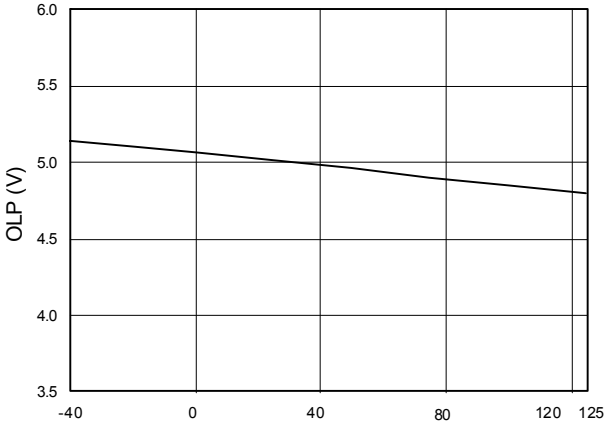


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

As green power requirements become a trend and the power saving gets more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitations force PWM controllers to be more powerful by integrating more functions and, thus, reducing the external part counts. LD7750B is designed for such application to provide an easy and cost effective solution. Its detail features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuits power the PWM controller on through a startup resistor. It will constantly provide current from a rectified voltage to the capacitor connected to Vcc pin. Nevertheless, this startup resistor was usually of larger resistance, and it therefore consumes more power and requires more time to start up.

To achieve an optimized topology, as shown in Fig. 13, The LD7750B is built in with high voltage startup circuit to optimize the power saving. During the startup sequence, a high-voltage current source sinks current from C_{BULK} capacitor to provide the startup current as well as to charge the Vcc capacitor C1. During the initialization of the startup, Vcc voltage is lower than the UVLO(off) threshold thus the current source is on to supply a current of 1mA. Meanwhile, as the Vcc current consumed by the LD7750B is as low as 320μA thus most of the HV current is utilized to charge the Vcc capacitor. By using such configuration, the turn-on delay time will be almost the same no matter what operation condition is, under low-line or high-line.

When Vcc voltage reaches UVLO(on) threshold, the LD7750B is powered on to start issuing the gate drive signal, the high-voltage current source is then disabled, and the Vcc supply current will be only provided from the auxiliary winding of the transformer. Therefore, the power loss on the startup circuit beyond the startup period is minimized and the power saving is enhanced. In general applications, a 39KΩ resistor is still recommended to be placed in high voltage path to limit the current if there is a negative voltage applying in any case.

An UVLO comparator is included to detect the voltage over the V_{CC} pin to ensure the supply voltage is high enough to power on the LD7750B and in addition to drive the power MOSFET as well. As shown in Fig. 14, a hysteresis is provided to prevent the shutdown caused by the voltage dip during startup.

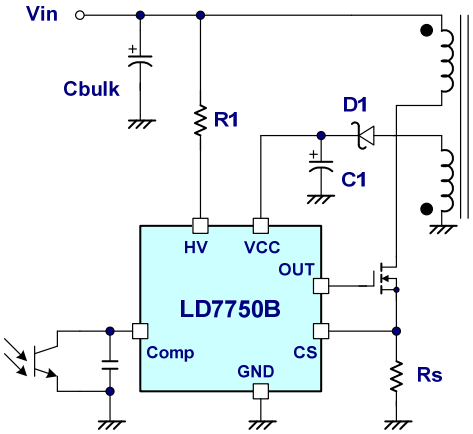


Fig. 13

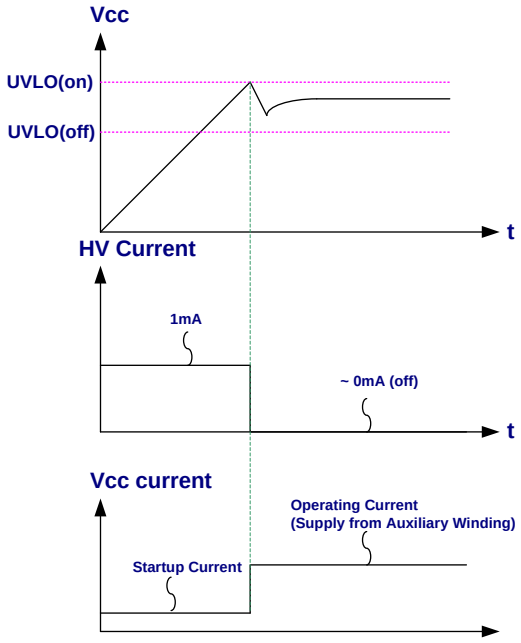


Fig. 14

Current Sensing, Leading-edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feeds back both current signal and voltage signal to close the control loop and achieve regulation. The LD7750B detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set as 0.45V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.45V}{R_S}$$

A 250nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent false-trigger caused by the current spike. For those low power applications, if the total pulse width of the turn-on spike is less than 250nS and the negative spike on the CS pin is above -0.3V, the R-C filter (as shown in Fig.15) is removable.

However, the total pulse width of the turn-on spike is related to the output power, circuit design and PCB layout. Nevertheless, it is strongly recommended to add a small R-C filter (as shown in Fig. 16) for higher power applications to avoid the CS pin being damaged by the negative turn-on spike.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7750B is limited to 75% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 in the secondary side through the photo-coupler to the COMP pin of LD7750B. The input stage of LD7750B, like the UC384X, is incorporated with 2 diodes voltage offset circuit and a voltage divider with 1/6 ratio. Therefore,

$$V_{+(PWM_{COMPARATOR})} = \frac{1}{6} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally and thus no external one is required for it.

Switching Frequency

The LD7750B is implemented with frequency swapping function which helps the power supply designers both optimize EMI performance and lower system cost. The switching frequency substantially centers at 100kHz, and trembles within the range of ±6KHz.

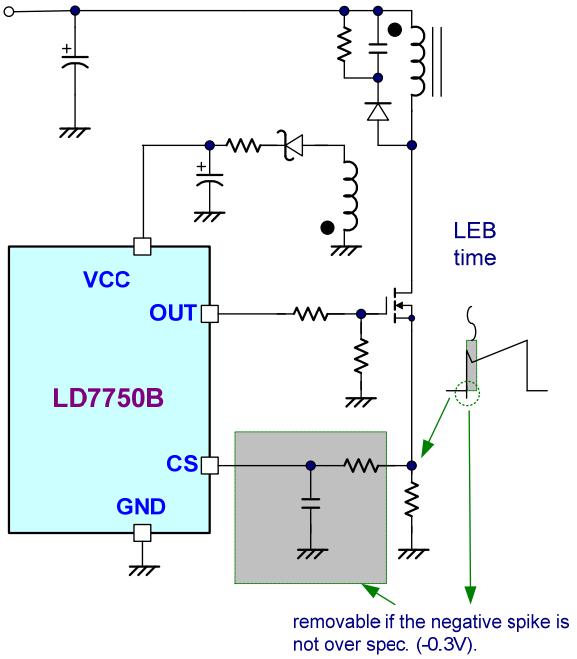


Fig. 15

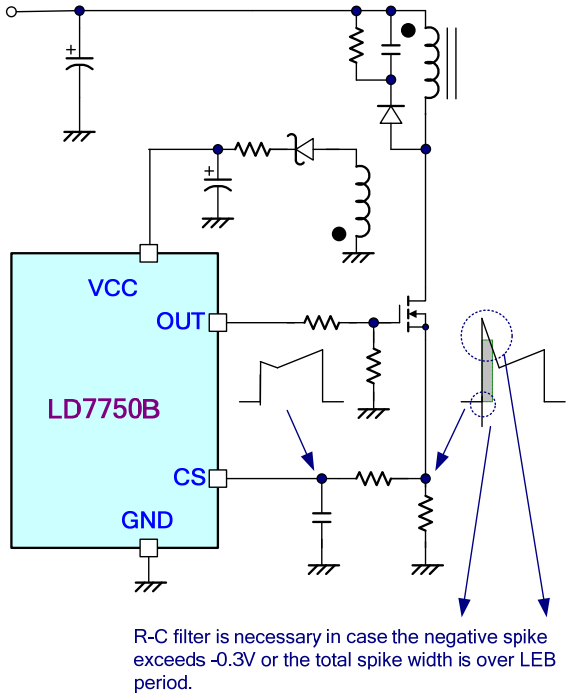


Fig. 16

Internal Slope Compensation

Stability is crucial for current mode control when it operates at more than 50% of duty-cycle. To stabilize the control loop, the slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. In the LD7750B, the internal slope compensation circuit has been implemented to simplify the external circuit design.

On/Off Control

The LD7750B can be turned off by pulling COMP pin to lower than 1.6V. The gate output pin of LD7750B will be disabled immediately under such condition. The off-mode can be released when the pull-low signal is removed.

Green-Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own IP.

Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage caused by overload condition or output short condition, a smart OLP function is implemented in the LD7750B for it. The OLP function in LD7750B is an auto-recovery type protection. Fig. 17 shows the waveforms of the OLP operation. Under such fault condition, the feedback system will force the voltage loop toward saturation and thus pull the voltage on COMP pin (VCOMP) to high. Whenever the VCOMP trips the OLP threshold of 5.0V and stays for over the delay time, the protection will be activated to turn off the gate output and to shutdown the switching of power circuit. The OLP delay time is to prevent the false-trigger during the power-on and turn-off transient.

A divided-by-2 counter is implemented to reduce the average power consumption under OLP behavior. Once OLP is activated, the output is latched off and the divided-by-2 counter starts to count the number of UVLO(off). The latch will be released if the 2nd UVLO(off) point is counted, and then the output recovers switching again.

By using such protection mechanism, the average input power can be reduced to a very low level so that the component temperature and stress can be controlled within a safe operating area.

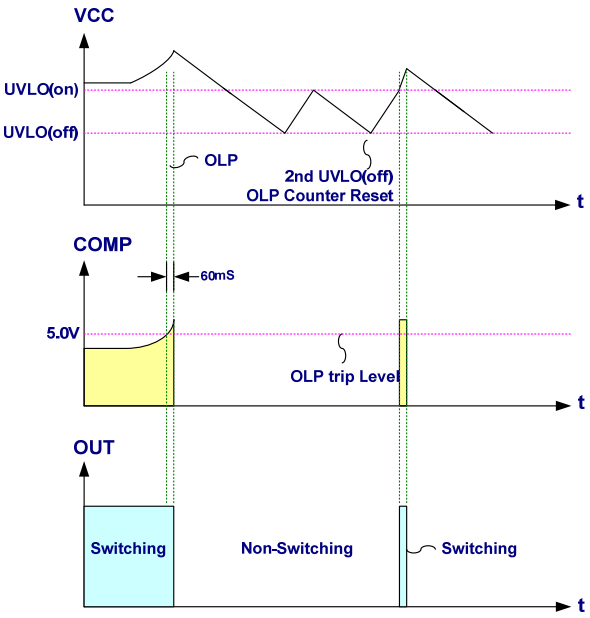


Fig. 17

OVP (Over Voltage Protection) on Vcc-Latched Mode Protection

The V_{GS} ratings of the nowadays power MOSFETs are mostly with 30V maximum. To protect the V_{GS} from the fault condition, LD7750B is implemented with OVP function on Vcc. As soon as Vcc voltage is larger than the OVP threshold voltage, the output gate drive circuit will be shut down simultaneously and stop switching of the power MOSFET.

The Vcc OVP function in LD7750B is latched-off type of protection. If the OVP condition (usually caused by the feedback loop opened) is tripped, the Vcc will not recover until ac power turn off. Figure 18 shows its operation. The Vcc will drop if AC power turns off. The de-latch level of OVP is defined by internal PDR. Over voltage protection will be released after Vcc drops below PDR level.

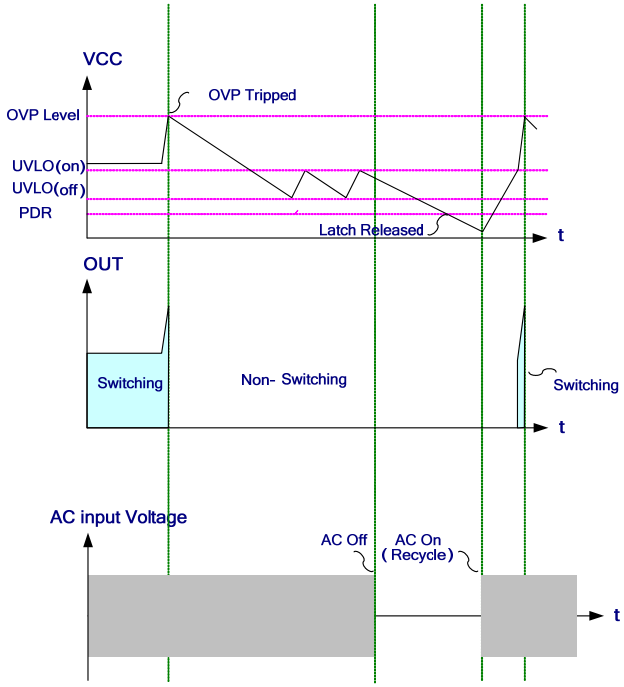


Fig. 18

OTP Pin --- Latched Mode Protection

To protect the power circuit from damage due to system failure, the over temperature protection (OTP) is required. The OTP circuit is implemented to sense a hot-spot of power circuit like power MOSFET or output rectifier. It can be easily achieved by connecting a NTC with OTP pin of LD7750B. As the device temperature or ambient temperature rises, the resistance of NTC decreases. So, the voltage on the OTP pin could be written as below.

$$V_{OTP} = 100\mu A \cdot R_{NTC}$$

When the V_{OTP} is less than the defined threshold voltage (typical 0.95V), LD7750B will shutdown the gate output

and then latch the power supply off. The controller will remain latched unless the Vcc drops below 8V (power down reset) and the fault condition is removed at the same time. There are 2 conditions required to restart it successfully. First, cool down the circuit so that NTC resistance will increase and raise V_{OTP} above 1.05V. Then, remove the AC power cord and restart AC power-on recycling. The detailed operation is depicted in Fig. 19.

Pull-Low Resistor on the Gate Pin of MOSFET

An anti-floating resistor is built in with the OUT pin to prevent the output from any uncertain state. Otherwise, it may cause the MOSFET malfunction or mis-trigger. However, such design won't cover the condition of disconnection between the OUT pin and the gate terminal for the MOSFET. Thus it is still strongly recommended to have a resistor connected at the MOSFET gate terminal (as shown in Fig. 20) to provide extra protection for fault conditions.

This external pull-low resistor is to prevent the MOSFET from damage during power-on when the gate resistor R_g is disconnected. In such a fault condition, as show in Fig. 21, the resistor R8 can provide a discharge path to avoid the MOSFET from being falsely triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the MOSFET should be always pulled-low to persist in off-state.

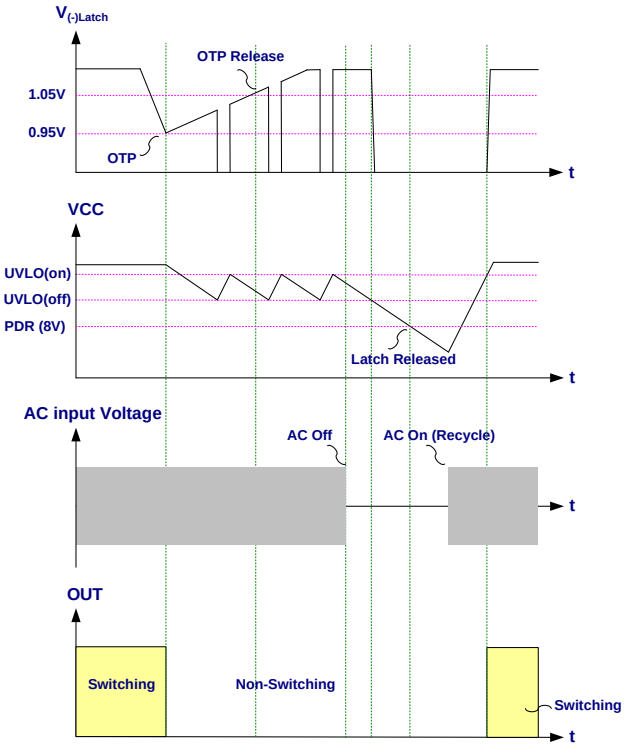


Fig. 19

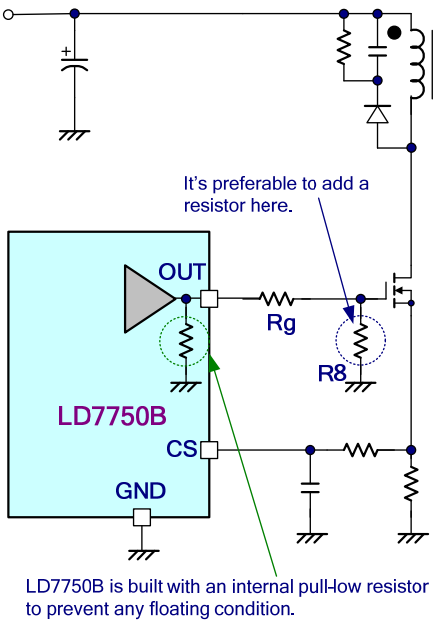


Fig. 20

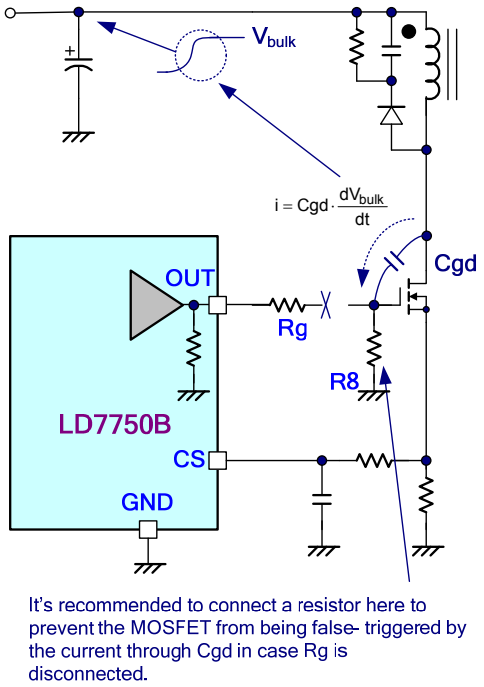


Fig. 21

Protection Resistor on the Hi-V Path

In some other Hi-V processes and designs, there may be a parasitic SCR caused around the pins of HV, Vcc and GND. As shown in Fig. 22, a small negative spike over the HV pin may trigger this parasitic SCR and cause latch up between Vcc and GND. And such latch up will easily damage the chip because of the equivalent short-circuits induced.

With the Leadtrend's proprietary Hi-V technology, there is no such parasitic SCR in LD7750B. Fig. 23 shows the equivalent circuit of LD7750B's Hi-V structure. The LD7750B features superior capability to sustain negative voltage than those similar products. Nevertheless, a 39KΩ resistor is recommended to implement on the Hi-V path to act as a current limit resistor no matter what negative voltage is present in any situation.

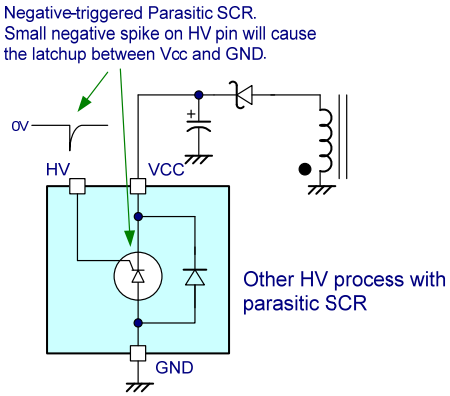


Fig. 22

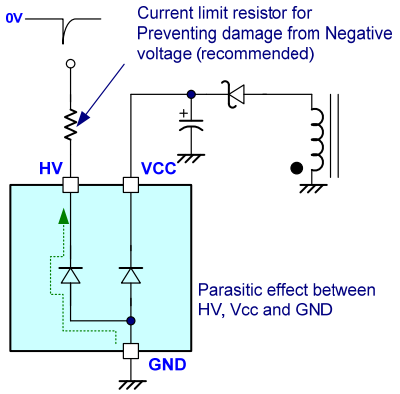
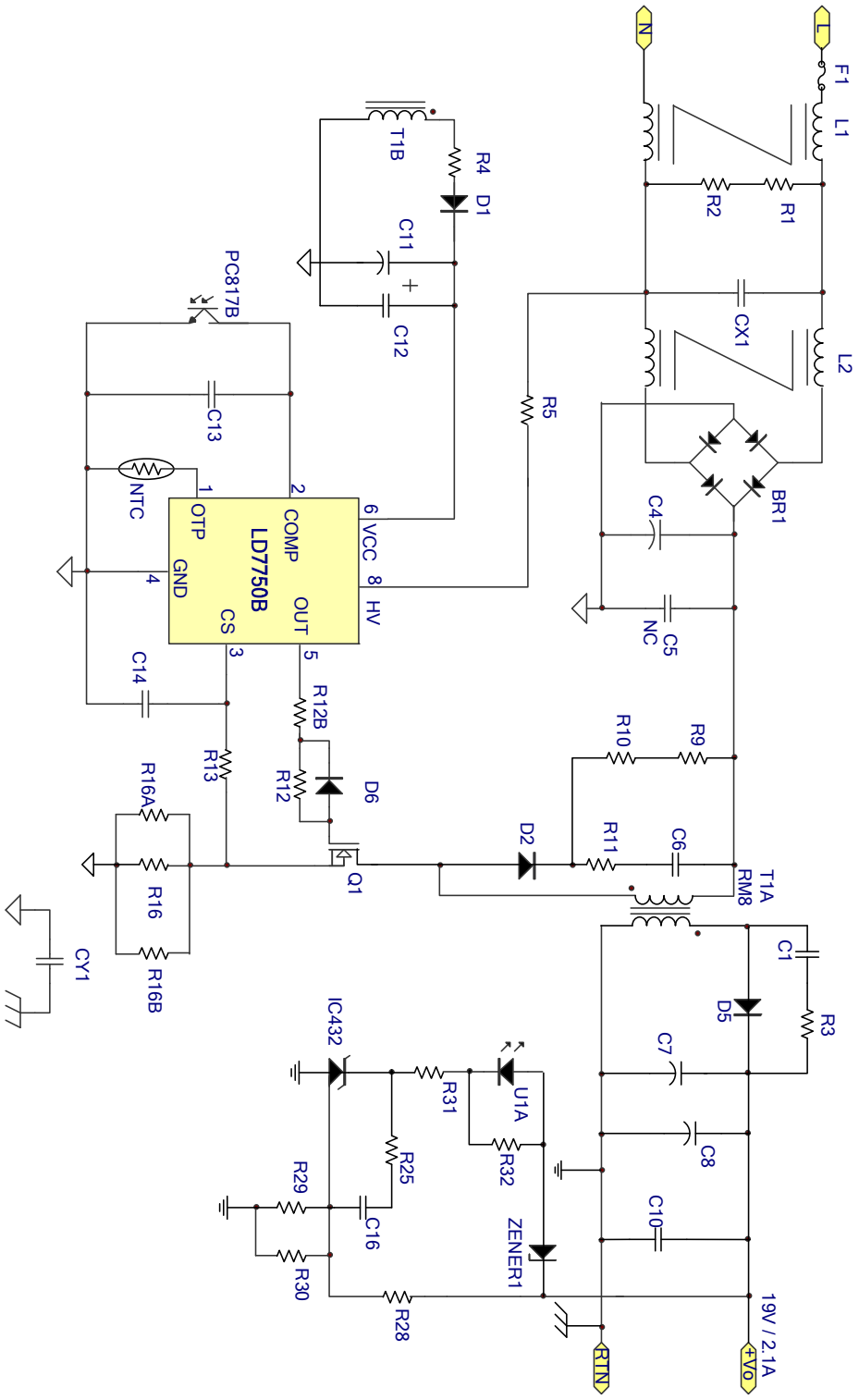


Fig. 23

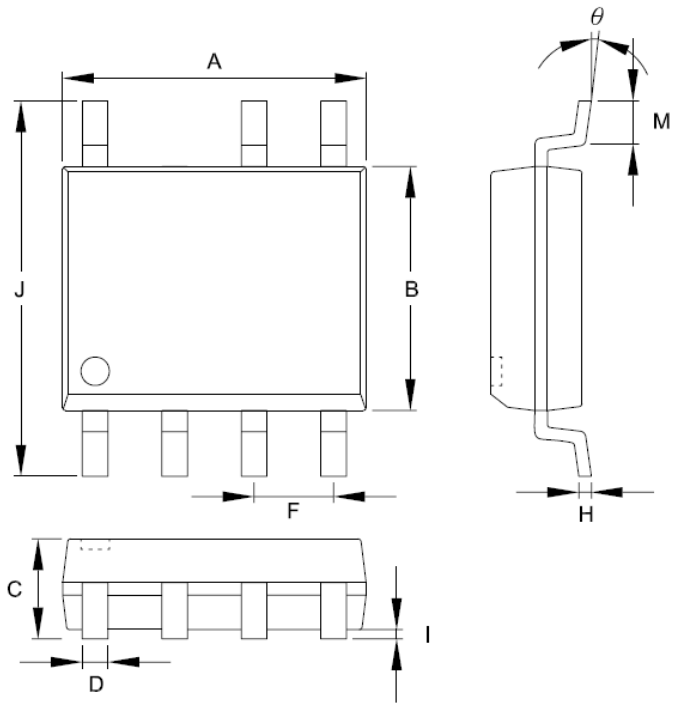
Reference Application Circuit ---19V/2.15A Adapter

Pin < 0.10W when Pout = 0W & Vin = 264Vac



Package Information

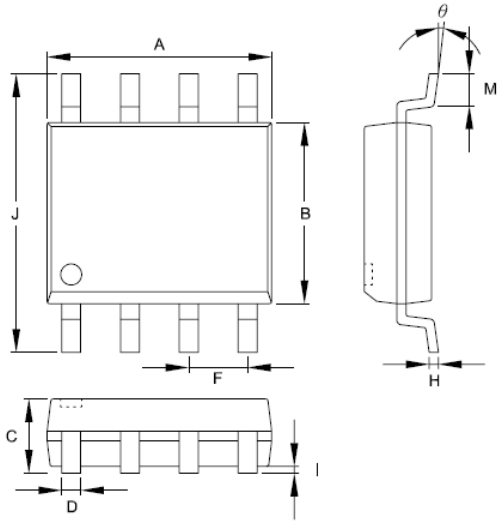
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
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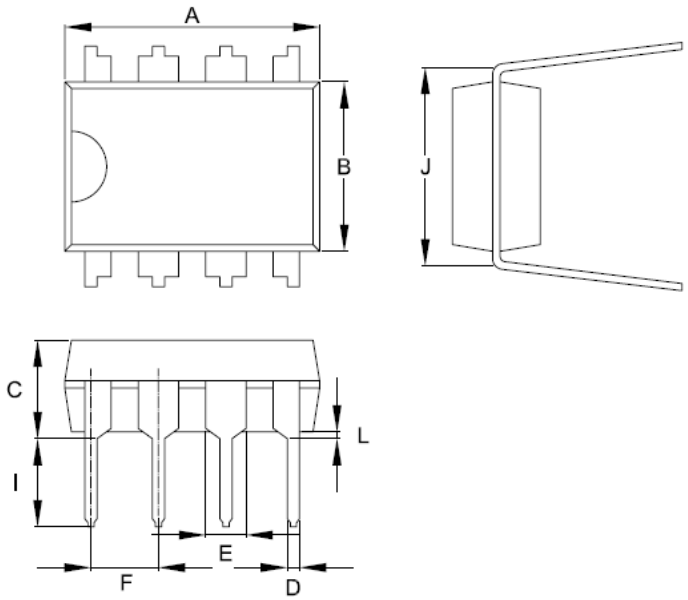
Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	9/19/2011	Original Specification
01	10/31/2011	Revise Operating current, Vcs-off, Frequency, PDR spec.