

## High Voltage Green-Mode PWM Controller with Over Temperature Protection

Rev. 00

### General Description

The LD7750E integrates several functions of protections, and EMI-improved solution in a SOP-7, SOP-8 or DIP-8 package to minimize the component counts and the circuit space.

The device provides functions of low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. Also, the LD7750E features more protections like OLP (Over Load Protection), OVP (Over Voltage Protection), and OTP (Over Temperature Protection) to prevent the circuit being damaged under the abnormal conditions. The LD7750E features built-in auto-recovery function for OVP on Vcc pin and OLP.

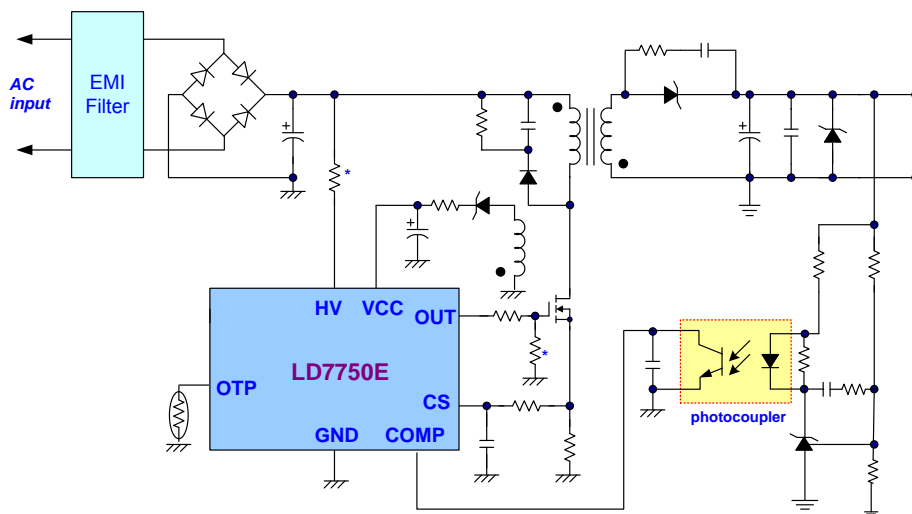
### Features

- High-Voltage (500V) Startup Circuit
- Current Mode Control
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Frequency Swapping
- Internal Slope Compensation
- Internal Over Current Protection
- OVP (Over Voltage Protection) on Vcc
- OLP (Over Load Protection)
- External OTP through a NTC
- 500mA Driving Capability

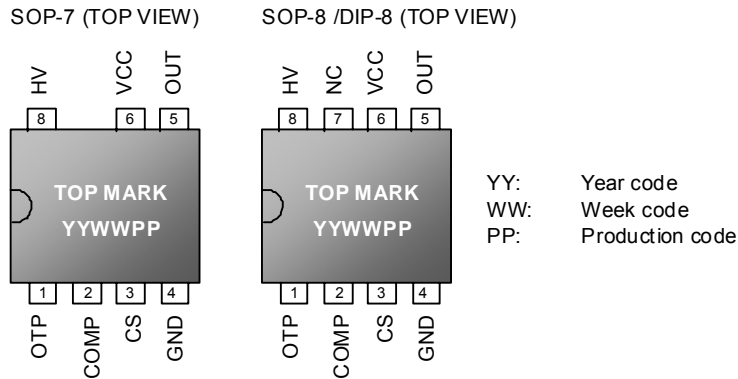
### Applications

- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

### Typical Application



## Pin Configuration



## Ordering Information

Part number	Package	Top Mark	Shipping
LD7750EGS	SOP-8	LD7750EGS	2500 /tape & reel
LD7750EGR	SOP-7	LD7750EGR	2500 /tape & reel
LD7750EGN	DIP-8	LD7750EGN	3600 /tube /Carton

The LD7750E is green packaged

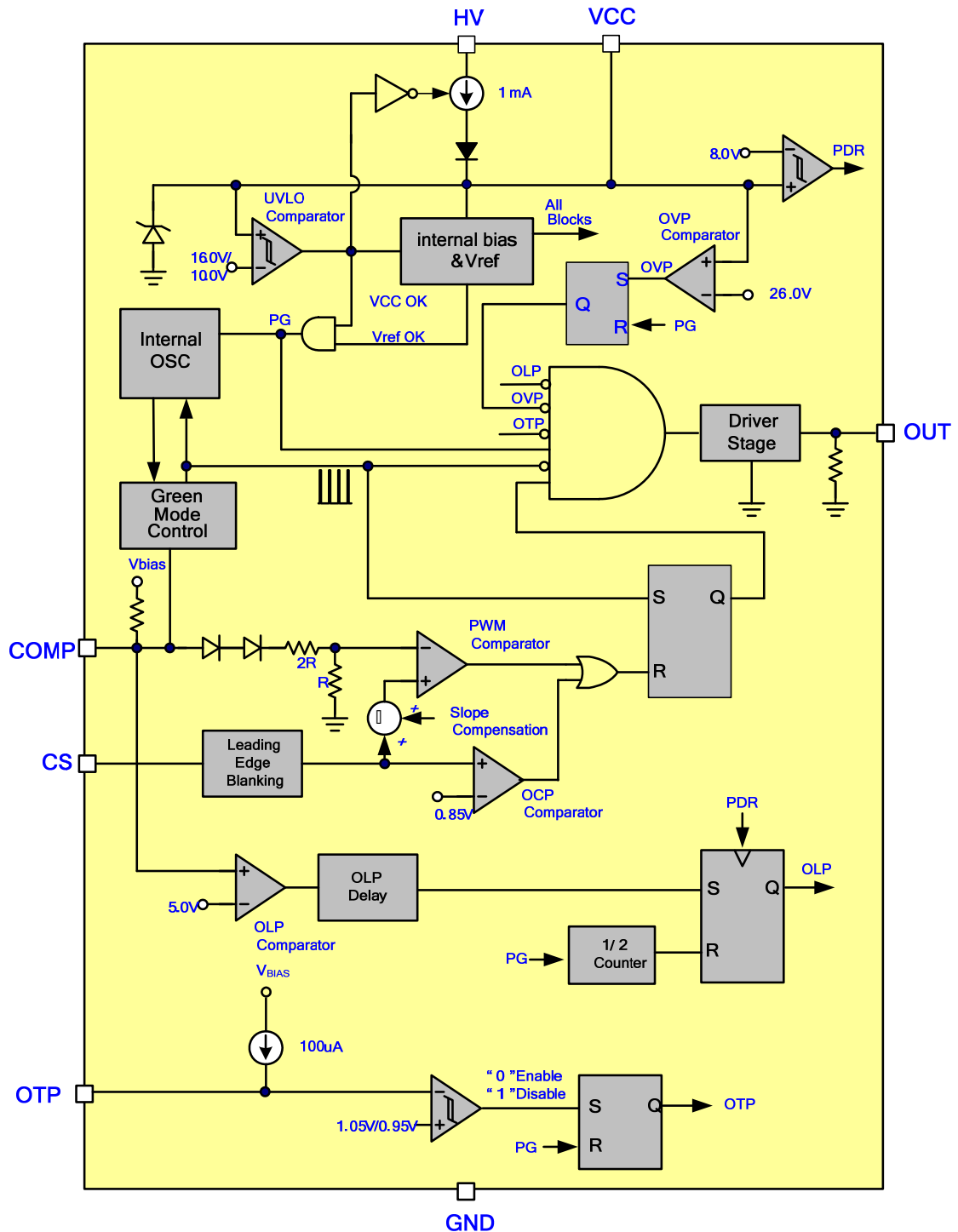
## Protection Mode

Part number	Switching Freq.	VCC OVP	OLP	OTP Pin
LD7750E	65kHz	Auto recovery	Auto recovery	Auto recovery

## Pin Descriptions

SOP-8 DIP-8	SOP-7	NAME	FUNCTION
1	1	OTP	Pulling this pin below 0.95V will shut down the controller. Connecting a NTC between this pin and ground will achieve OTP protection function. Let this pin float or connect a 100k $\Omega$ resistor to disable the latch protection.
2	2	COMP	Voltage feedback pin. By connecting a photo-coupler to close the control loop can achieve the regulation.
3	3	CS	Current sense pin, for sensing the MOSFET current.
4	4	GND	Ground.
5	5	OUT	Gate drive output to drive the external MOSFET.
6	6	VCC	Supply voltage pin.
7		NC	Unconnected Pin.
8	8	HV	Connect this pin to a positive terminal of bulk capacitor to provide the startup current for the controller. When Vcc voltage trips the UVLO(on), this HV loop will be turned off to reduce the power loss on the startup circuit.

## Block Diagram



## Absolute Maximum Ratings

Supply Voltage VCC .....	-0.3V~30V
High-Voltage Pin, HV .....	-0.3V~500V
COMP, OTP, CS .....	-0.3 ~7V
OUT .....	-0.3 ~Vcc+0.3
Maximum Junction Temperature .....	150°C
Operating Ambient Temperature .....	-40°C to 85°C
Operating Junction Temperature .....	-40°C to 125°C
Storage Temperature Range .....	-65°C to 150°C
Package Thermal Resistance (SOP-7/ SOP-8) .....	160°C/W
Package Thermal Resistance (DIP-8) .....	100°C/W
Power Dissipation (SOP-7/ SOP-8, at Ambient Temperature = 85°C) .....	400mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C) .....	650mW
Lead temperature (Soldering, 10sec) .....	260°C
ESD Voltage Protection, Human Body Model (except HV Pin) .....	2.5KV
ESD Voltage Protection, Machine Model .....	250V
Gate Output Current .....	500mA

### Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## Electrical Characteristics

(T<sub>A</sub> = +25°C unless otherwise stated, V<sub>CC</sub>=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>High-Voltage Supply (HV Pin)</b>					
High-Voltage Current Source	V <sub>CC</sub> < UVLO(on), HV=500V	0.5	1.0	1.5	mA
Off-State Leakage Current	V <sub>CC</sub> > UVLO(off), HV=500V			35	μA
<b>Supply Voltage (Vcc Pin)</b>					
Startup Current			320		μA
Operating Current (with 1nF load on OUT pin)	V <sub>COMP</sub> =0V		1.2		mA
	V <sub>COMP</sub> =3V,		2.3		mA
	OLP tripped		0.6		mA
	OVP tripped, V <sub>CC</sub> =OVP		0.7		mA
UVLO (off)		9.0	10.0	11.0	V
UVLO (on)		15.0	16.0	17.0	V
OVP Level		25.0	26.0	27.0	V
<b>Voltage Feedback (COMP Pin)</b>					
Short Circuit Current	V <sub>COMP</sub> =0V	0.20	0.26	0.32	mA
Open Loop Voltage	COMP pin open	5.5	6.0	6.5	V
Green Mode Threshold V <sub>COMP</sub>	*		2.75		V
Zero Duty		1.7	1.8	1.9	V
<b>Current Sensing (CS Pin)</b>					
Maximum Input Voltage, V <sub>cs_off</sub>		0.80	0.85	0.90	V
Leading Edge Blanking Time		160	250	320	ns
Input impedance		1			MΩ
Delay to Output	*		100		ns
<b>Oscillator for Switching Frequency</b>					
Frequency		61.0	65.0	69.0	KHz
Green Mode Frequency			22		KHz
Trembling Frequency	V <sub>COMP</sub> =4.5V		±4		kHz
Temp. Stability	-20°C~85°C*		5		%
Voltage Stability	(V <sub>CC</sub> =11V-25V)*			1	%

## Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>OTP Pin Protection (OTP Pin)</b>					
OTP Pin Source Current		92	100	108	μA
Turn-On Trip Level		1.00	1.05	1.10	V
Turn-Off Trip Level		0.90	0.95	1.0	V
<b>Gate Drive Output (OUT Pin)</b>					
Output Low Level	V <sub>CC</sub> =15V, I <sub>o</sub> =20mA			1	V
Output High Level	V <sub>CC</sub> =15V, I <sub>o</sub> =20mA	9			V
Rising Time	Load Capacitance=1000pF		100	160	ns
Falling Time	Load Capacitance=1000pF		30	60	ns
<b>OLP (Over Load Protection)</b>					
OLP Trip Level		4.8	5.0	5.2	V
OLP Delay Time		57	64	70	ms
<b>Soft Start Duration</b>					
Soft Start Duration	*		2		ms
<b>On Chip OTP (Internal Over Temperature Protection, Auto-Recovery)</b>					
OTP Level	*		140		°C
OTP Hysteresis	*		30		°C

\*: These parameters are guaranteed by design.

## Typical Performance Characteristics

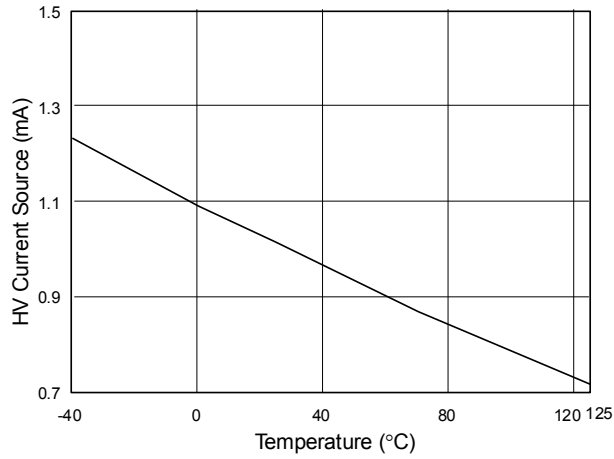


Fig. 1 HV Current Source vs. Temperature (HV=500V, Vcc=0V)

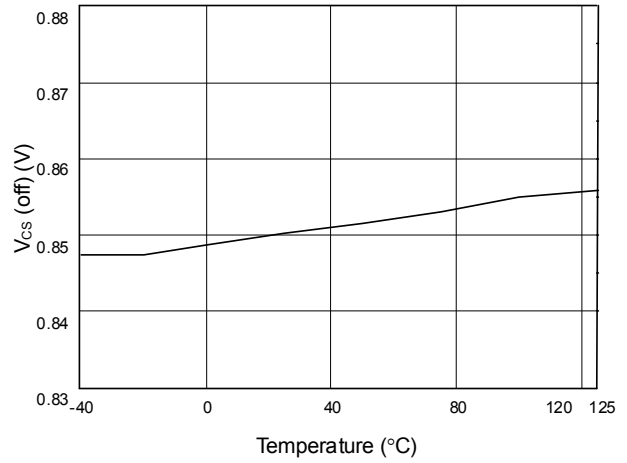


Fig. 2 Vcs (off) vs. Temperature

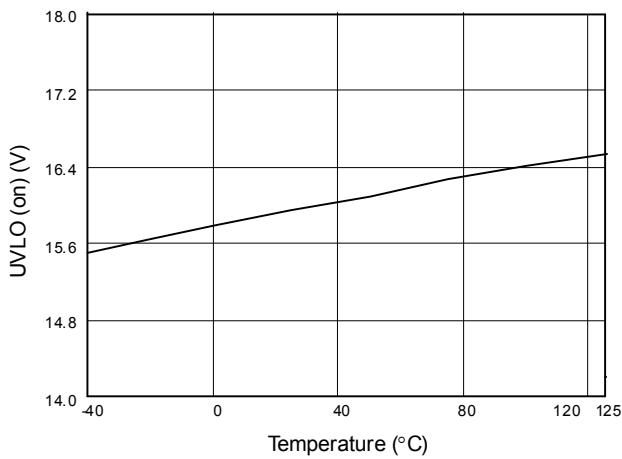


Fig. 3 UVLO (on) vs. Temperature

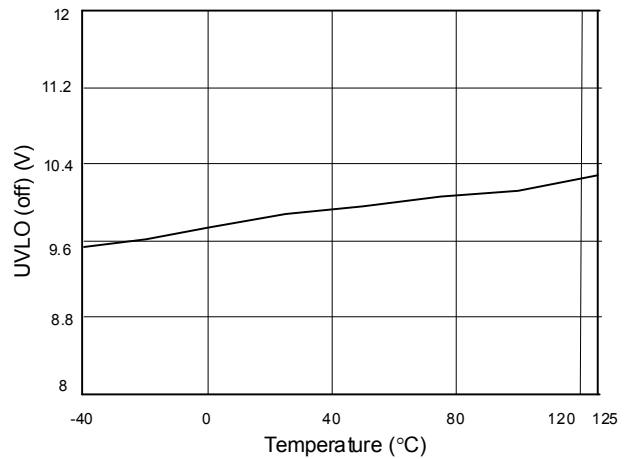


Fig. 4 UVLO (off) vs. Temperature

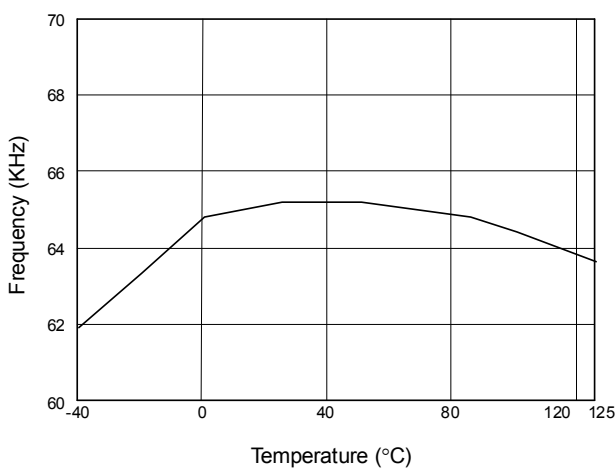


Fig. 5 Frequency vs. Temperature

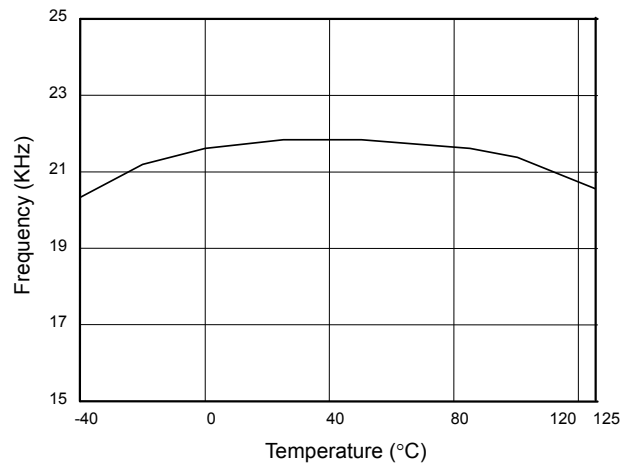


Fig. 6 Green Mode Frequency vs. Temperature

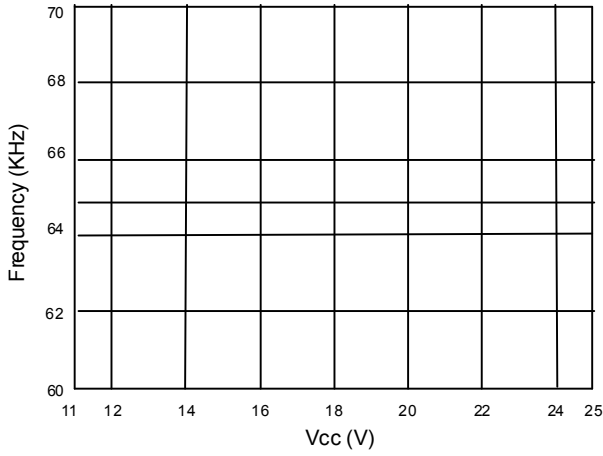


Fig. 7 Frequency vs. Vcc

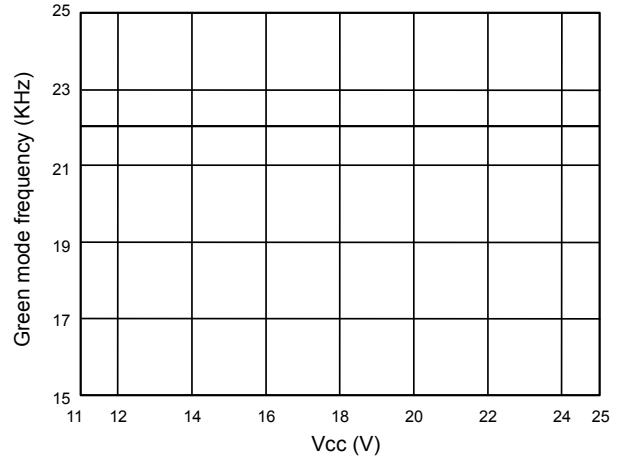


Fig. 8 Green mode frequency vs. Vcc

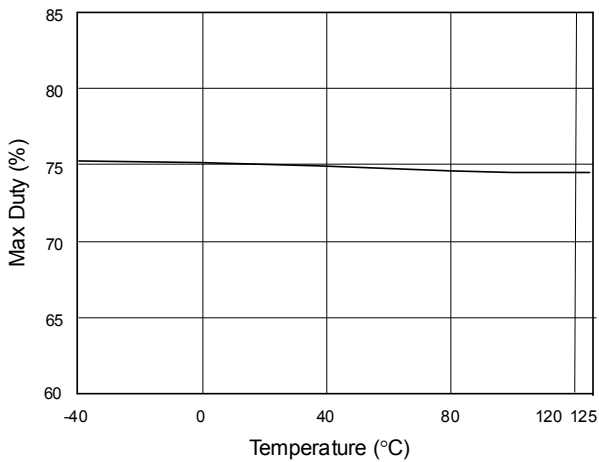


Fig. 9 Max Duty vs. Temperature

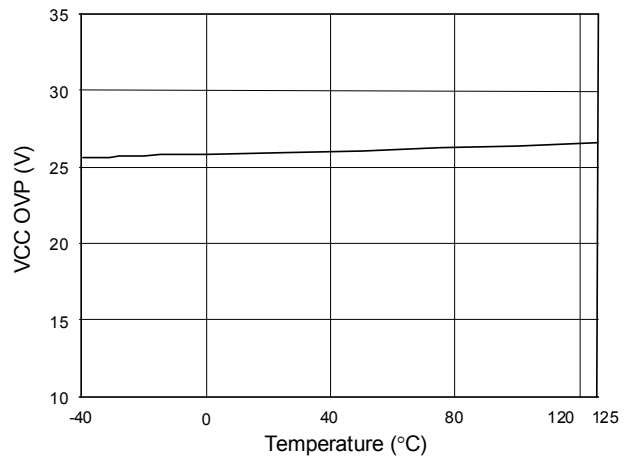


Fig. 10 VCC OVP vs. Temperature

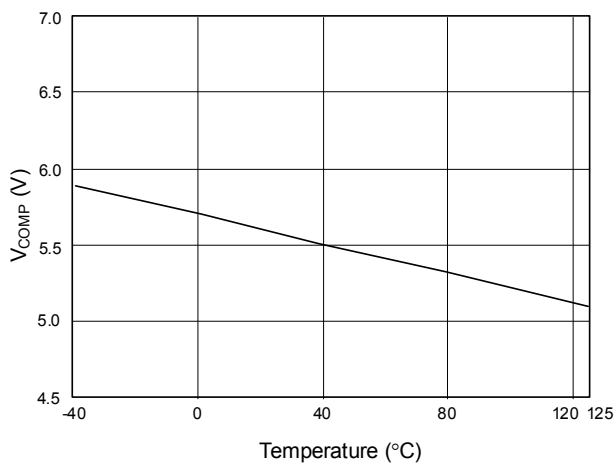


Fig. 11 V<sub>COMP</sub> open loop voltage vs. Temperature

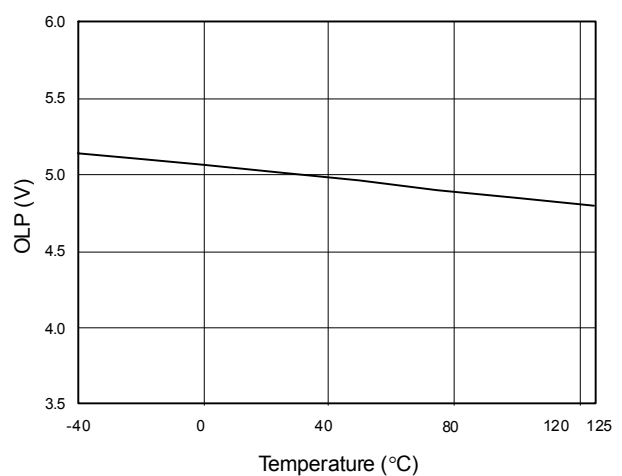


Fig. 12 OLP-Trip Level vs. Temperature



## Application Information

### Operation Overview

As green power requirement becomes a trend and the power saving gets more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitations force PWM controllers to be more powerful by integrating more functions and, thus, reducing the external part count. LD7750E is designed for such application to provide an easy and cost effective solution. Its detailed features are described as below.

### Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit powers on the PWM controller through a startup resistor to constantly provide current from a rectified voltage to the capacitor connected to Vcc pin. Nevertheless, this startup resistor was usually of larger resistance, and it therefore consumed more power and required longer time to start up.

To achieve an optimized topology, as shown in Fig. 13, The LD7750E is built in with high voltage startup circuit to optimize the power saving. During the startup sequence, a high-voltage current source sinks current from C<sub>BULK</sub> capacitor to provide the startup current as well as to charge the Vcc capacitor C1. During the initialization of the startup, Vcc voltage is below UVLO(off) threshold thus the current source is on to supply a current of 1mA. Meanwhile, as the Vcc current consumed by the LD7750E is only 320 $\mu$ A thus most of the HV current is left to charge the Vcc capacitor. With using such configuration, the turn-on delay time will be almost the same no matter what operation condition is under low-line or high-line.

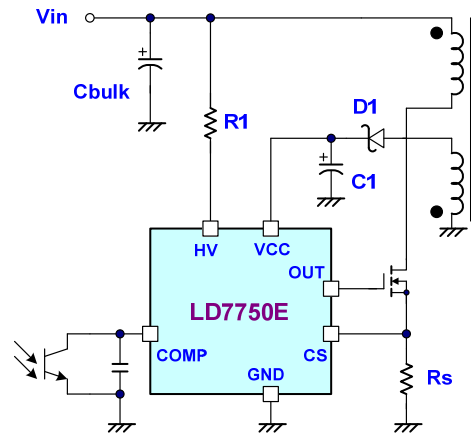


Fig. 13

When Vcc voltage reaches UVLO(on) threshold, the LD7750E is powered on to start issuing the gate drive signal, disable the high-voltage current source, and the Vcc supply current will be only provided from the auxiliary winding of the transformer. Therefore, the power loss for the startup circuit after the startup period can be eliminated and the power saving can be easily achieved. In general application, a 39K $\Omega$  resistor is still recommended to be placed in high voltage path to limit the current if there is a negative voltage applying in any case.

An UVLO comparator is included to detect the voltage of the V<sub>CC</sub> pin to ensure the supply voltage is high enough to power on the LD7750E PWM controller and in addition to drive the power MOSFET as well. As shown in Fig. 14, a Hysteresis is provided to prevent the shutdown caused by the voltage dip during startup. The turn-on and turn-off threshold levels are set at 16V and 10.0V, respectively.

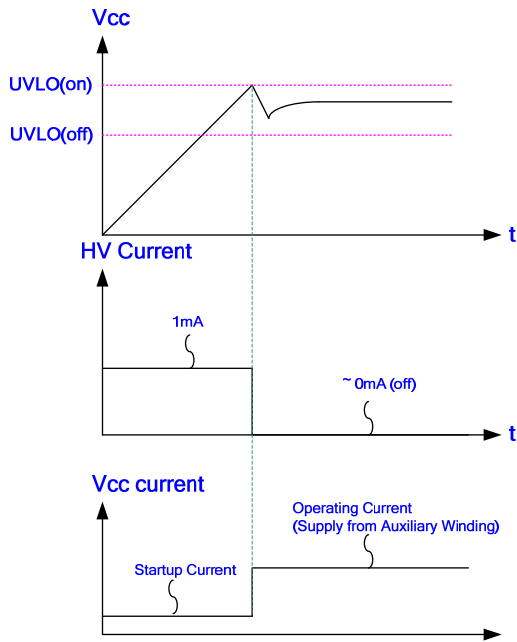


Fig. 14

## Current Sensing, Leading-edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD7750E detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set as 0.85V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A 250nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent false-trigger caused by the current spike. For low power applications, if the total pulse width of the turn-on spike is less than 250nS and the negative spike on the CS pin is above -0.3V, the R-C filter (as shown in Fig.15) is eliminable.

However, the total pulse width of the turn-on spike is related to the output power, circuit design and PCB layout. Nevertheless, it is strongly recommended to add a small

R-C filter (as shown in Fig. 16) for higher power applications to avoid the CS pin being damaged by the negative turn-on spike.

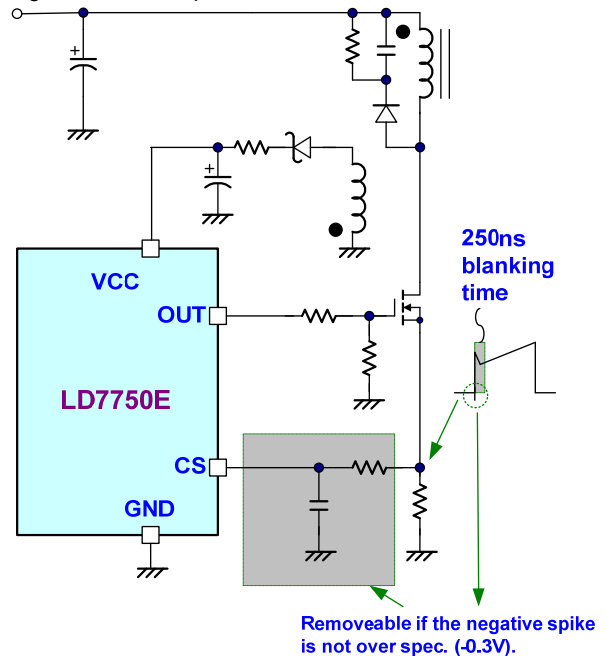


Fig. 15

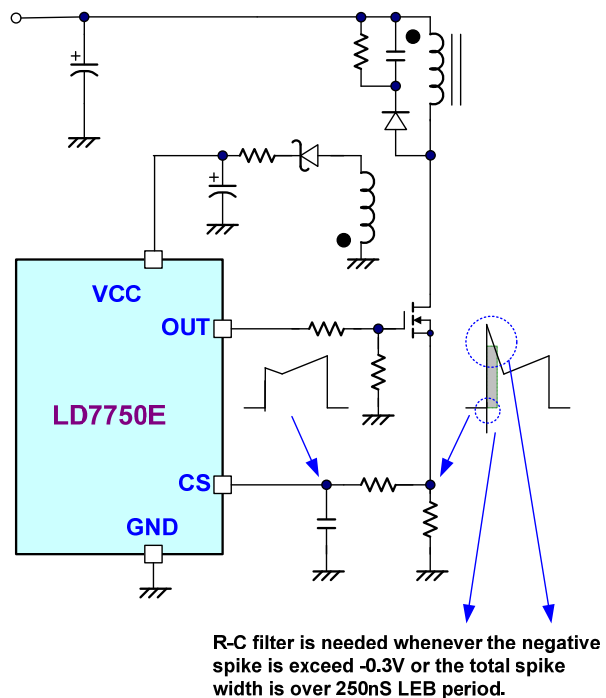


Fig. 16

## Oscillator and Switching Frequency

The LD7750E is implemented with Frequency Swapping function which helps the power supply designers to both optimize EMI performance and minimize the system cost. The switching frequency substantially centers at 65KHz, and swaps between a range of  $\pm 4$ KHz.

## Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer with driving capability of 500mA typically is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7750E is limited to 75% to avoid the transformer saturation.

## Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 in the secondary side through the photo-coupler to the COMP pin of LD7750E. The input stage of LD7750E, like the UC384X, is incorporated with 2 diodes voltage offset circuit and a voltage divider with 1/3 ratio. Therefore,

$$V_{+(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pulled-high resistor is embedded internally and thus no external one is required.

## Internal Slope Compensation

Stability is crucial for current mode control when it operates at more than 50% of duty-cycle. To stabilize the control loop, the slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. In the LD7750E, the internal slope compensation circuit has been implemented to simplify the external circuit design.

## On/Off Control

The LD7750E can be turned off by pulling COMP pin to below 1.8V. The gate output pin of LD7750E will be disabled immediately under such condition. The off-mode can be released when the pull-low signal is removed.

## Green-Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own IP.

## Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage due to overload condition or output short condition, a smart OLP function is implemented in the LD7750E for it. The OLP function is an auto-recovery type protection. Fig. 17 shows the waveforms of the OLP operation. Under such fault condition, the feedback system will force the voltage loop toward saturation and thus pull up the voltage of COMP pin ( $V_{COMP}$ ). If the  $V_{COMP}$  trips the OLP threshold of 5.0V and stays for over 64mS, the protection will be activated to turn off the gate output and to shutdown the switching of power circuit. The 64mS delay time is to prevent the false-trigger during the power-on and turn-off transient.

A divided-by-2 counter is implemented to reduce the average power consumption under OLP behavior. Whenever OLP is activated, the output is latched off and the divided-by-2 counter starts to count the number of UVLO(off). The latch will be released if the 2nd UVLO(off) point is counted, and then the output recovers switching again.

By using such protection mechanism, the average input power can be reduced to a very low level so that the

component temperature and stress can be controlled within a safe operating area.

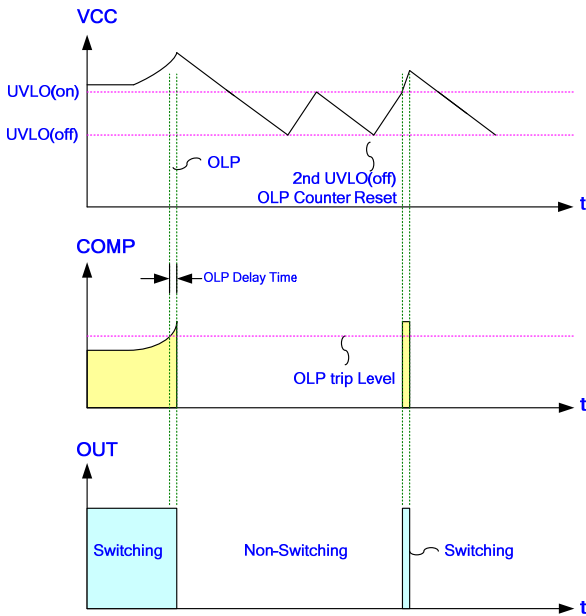


Fig. 17

## OVP (Over Voltage Protection) on Vcc- Auto Recovery

The  $V_{GS}$  ratings of the nowadays power MOSFETs are mostly 30V maximum. To protect the  $V_{GS}$  from the fault condition, LD7750E is implemented with OVP function at Vcc. Once the Vcc voltage is larger than the OVP threshold voltage, the output gate drive circuit will be shut down simultaneously and stop switching of the power MOSFET until the next UVLO<sub>(ON)</sub>.

The Vcc OVP function in LD7750E is an auto-recovery type protection. If the OVP condition, usually caused by open feedback loop, is not released, the Vcc will trip the OVP level again and shutdown the output. The Vcc is working in hiccup mode. Fig. 18 shows its operation.

Once the OVP condition is removed, the Vcc and the output will resume to normal operation.

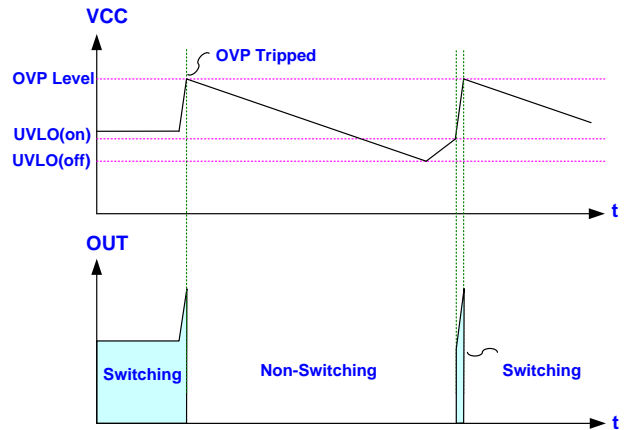


Fig. 18

## OTP Pin --- Auto Recovery Mode Protection

To protect the power circuit from damage due to system failure, over temperature protection (OTP) is required. The OTP circuit is implemented to sense a hot-spot of power circuit like power MOSFET or output rectifier. It can be easily achieved by connecting a NTC with OTP pin. As the device temperature or ambient temperature rises, the resistance of NTC decreases. So, the voltage on the OTP pin could be written as below.

$$V_{OTP} = 100\mu A \cdot R_{NTC}$$

When the  $V_{OTP}$  falls below the defined threshold (typ. 0.95V), LD7750E will shut down the gate output and stop switching of the power MOSFET until the next UVLO<sub>(ON)</sub>. The detailed operation is depicted in Fig. 19.

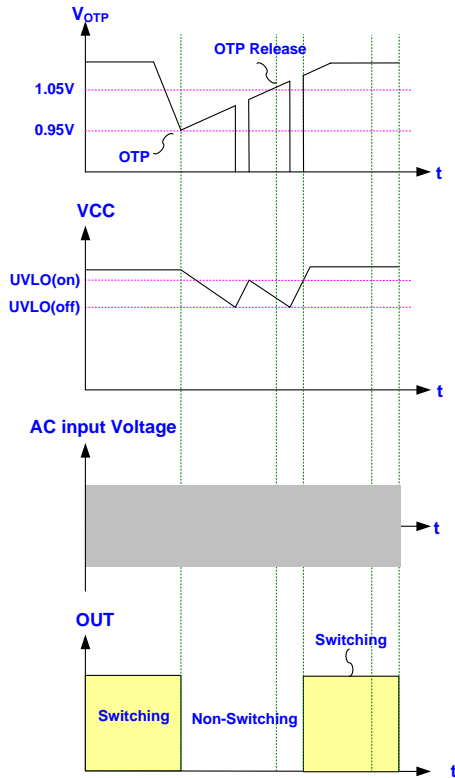


Fig. 19

## Pull-Low Resistor on the Gate Pin of MOSFET

An anti-floating resistor is built in with the OUT pin to prevent the output from any uncertain state. Otherwise, it may cause the MOSFET work abnormally or mis-trigger. However, such design won't cover the condition of disconnection between the OUT pin and the gate terminal for the MOSFET. Thus it is still strongly recommended to have a resistor connected at the MOSFET gate terminal (as shown in Fig. 20) to provide extra protection for fault conditions.

This external pull-low resistor is to prevent the MOSFET from being damaged during power-on when the gate resistor  $R_G$  is disconnected. In such fault condition, as show in Fig. 21, the resistor  $R_8$  will provide a discharge path to avoid the MOSFET from being falsely triggered by the current through the gate-to-drain capacitor  $C_{GD}$ .

Therefore, the MOSFET should be always pulled-low to persist in off-state.

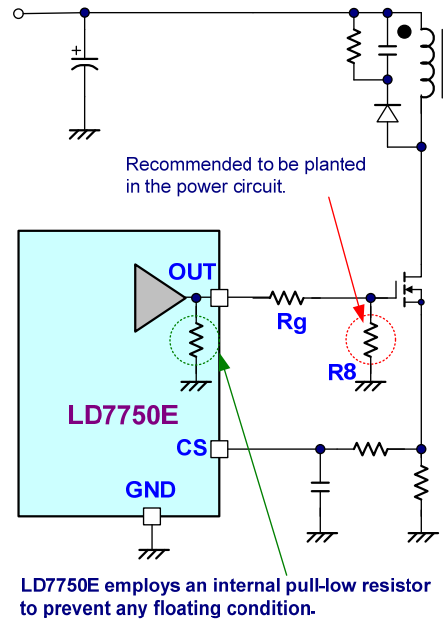


Fig. 20

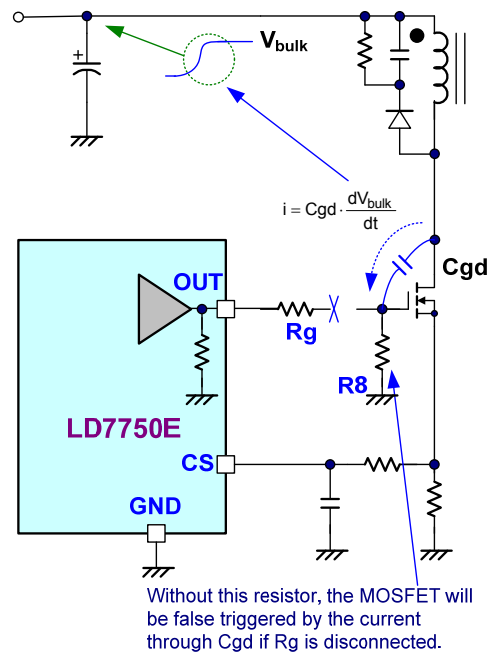


Fig. 21

## Protection Resistor on the Hi-V Path

In some Hi-V processes and designs, there may be a parasitic SCR between HV pin, Vcc and GND. As shown in Fig. 22, any small negative spike on the HV pin may trigger this parasitic SCR and latchup between Vcc and GND. It will easily damage the chip because of the equivalent short-circuit induced.

With the Leadtrend's proprietary Hi-V technology, there is no such parasitic SCR in LD7750E. Fig. 23 shows the equivalent circuit of LD7750E's Hi-V structure. The LD7750E has higher capability to sustain negative voltage than similar products. Nevertheless, a 39KΩ resistor is recommended to plant in the Hi-V path as a current limit resistor, no matter what negative voltage is present in any situation.

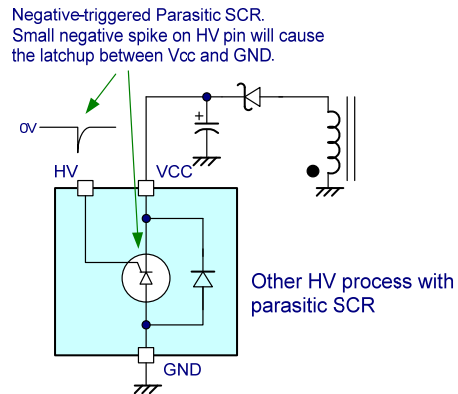


Fig. 22

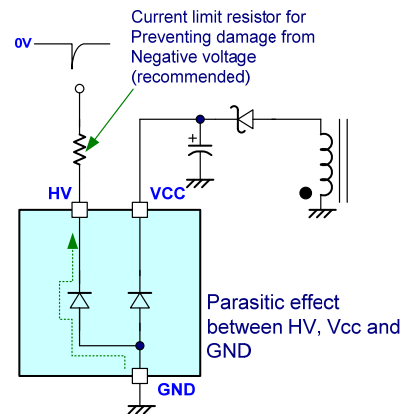
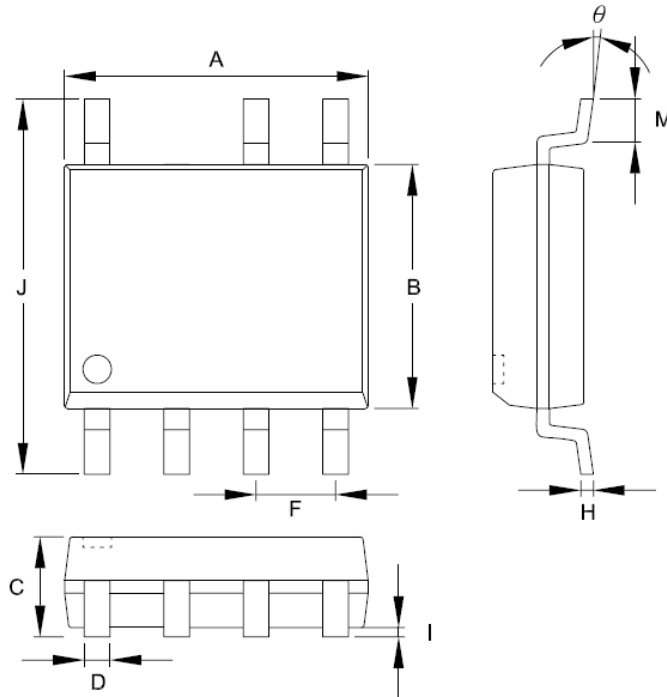


Fig. 23



## Package Information

SOP-7

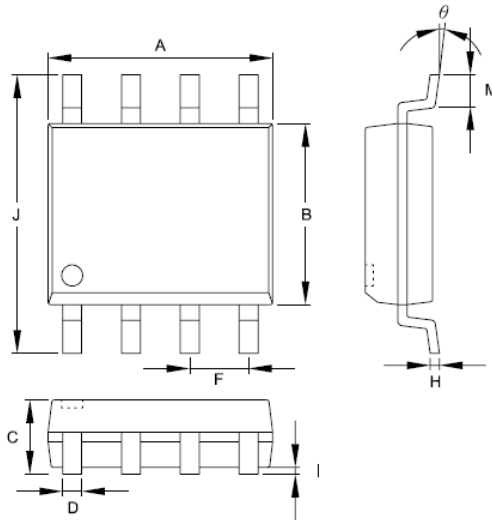


Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°



## Package Information

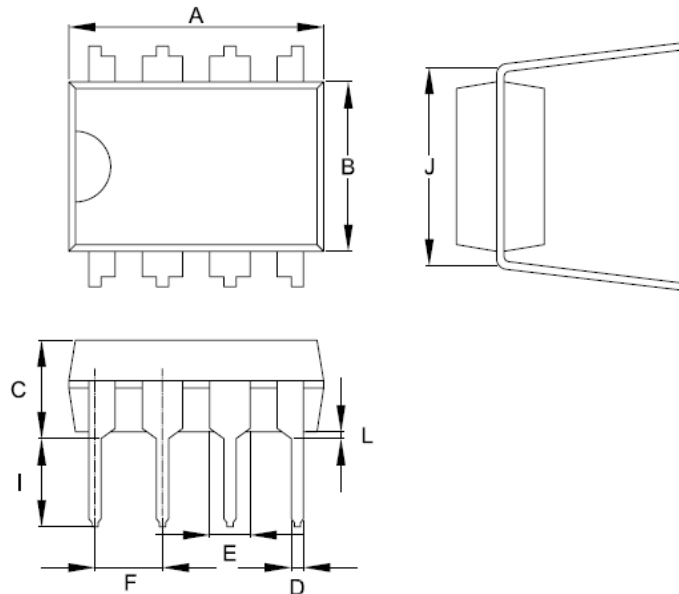
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

## Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	-----	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	-----	0.015	-----

### Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

**Revision History**

Rev.	Date	Change Notice
00	2/29/2012	Original Specification