High Voltage Green-Mode PWM Controller with BNO Function

REV: 00

General Description

The LD7765 is a Green Mode PWM IC, featuring X-cap discharge functions to reduce the discharge resistor loss in less component counts.

The LD7765 provides HV start-up, green-mode power-saving operation, internal slope compensation and Soft-start functions which could minimize the power loss and enhance the system performance.

With complete protection as OLP/ OVP/ OTP and brown-in/out, this chip prevents the circuit from being damaged in abnormal conditions.

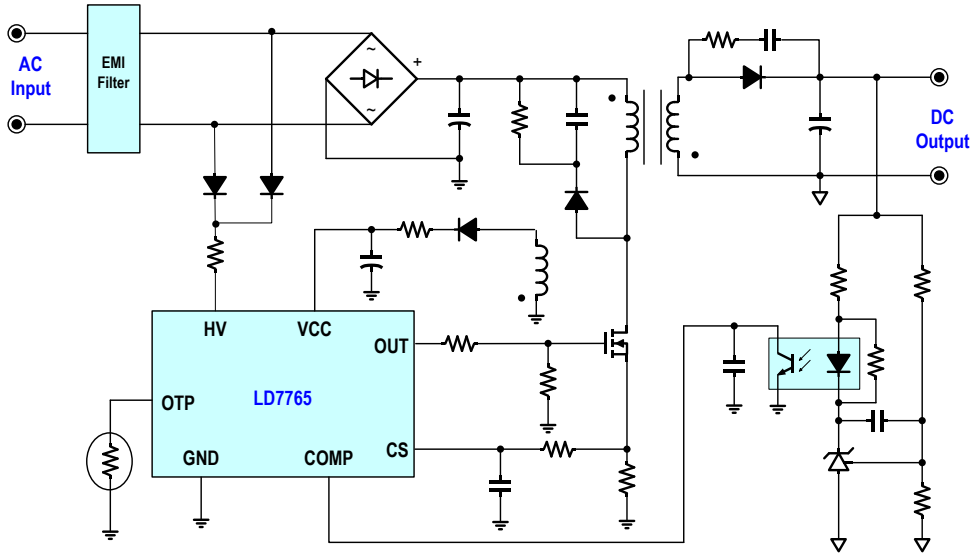
Features

- High-Voltage (500V) Startup Circuit on HV pin
- Brown-in/out Function on HV pin
- X-Cap Discharge function on HV pin
- Frequency Trembling for EMI improve
- Green Mode Control for Power Saving
- Current Mode control with Slope Compensation
- OVP (Over Voltage Protection) on Vcc
- OLP (Over Load Protection)
- OTP (Over temperature protection)
- Soft Start
- Soft Driving
- +500mA/-800mA Driving Capability

Applications

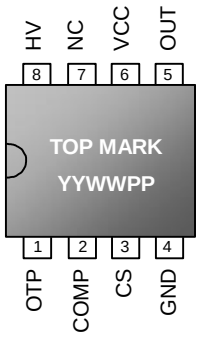
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

Typical Application

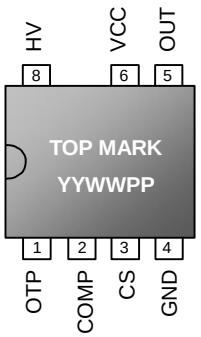


Pin Configuration

SOP-8 (TOP VIEW)



SOP-7 (TOP VIEW)



YY: Year code (D:2004, E2005…)
WW: Week code
PP: Production code

Ordering Information

Part number	Switching Freq.	Package	Top Mark	Shipping
LD7765 GS	65KHz	SOP-8	LD7765GS	2500 /tape & reel
LD7765 GR	65KHz	SOP-7	LD7765GR	2500 /tape & reel

The LD7765 is ROHS compliant/ green packaged.

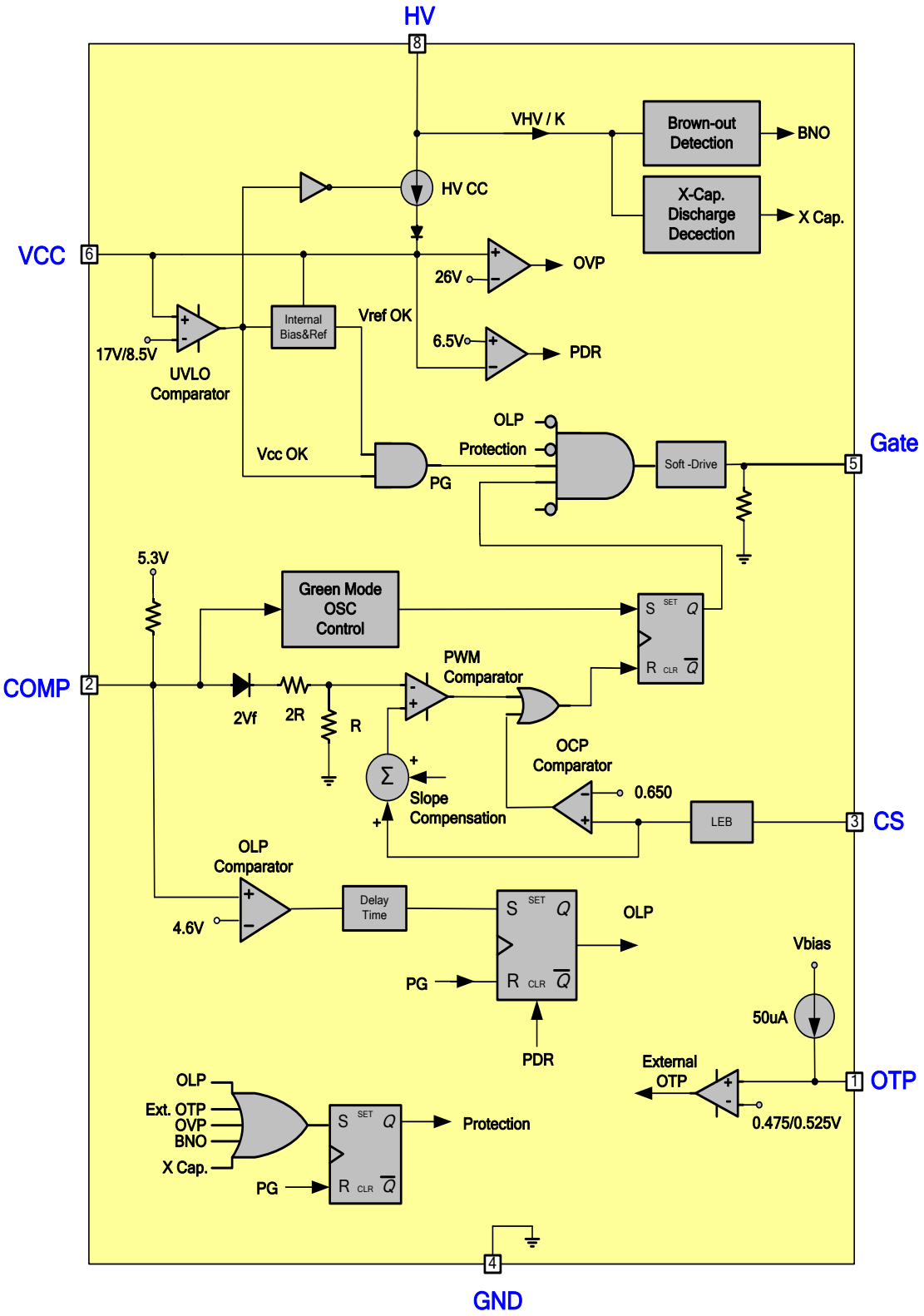
Protection Mode

VCC OVP	OLP	External OTP	Internal OTP
Auto recovery	Auto recovery	Latch	Auto recovery

Pin Descriptions

PIN	NAME	FUNCTION
1	OTP	Pulling this pin below 0.5V will shut down the controller to enter latch mode. Connecting a NTC between this pin and ground will achieve OTP protection function.
2	COMP	Voltage feedback pin. Connect a photo-coupler with it to close the control loop and achieve the regulation.
3	CS	Current sense pin. Connect it to sense the MOSFET current
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Supply voltage pin
7	NC	Unconnected Pin
8	HV	Connect this pin to Line/Neutral of AC main voltage through resistors to provide the startup current for the controller. When Vcc voltage increases to trip the point of UVLO(on), this HV loop will be turned off to reduce the power loss on the startup circuit. HV pin Internal Resistor divider will detect the AC peak voltage, and provide Brown in/out function. HV pin internal circuit will discharge X-cap's energy through HV current source when AC line is disconnected.

Block Diagram



Absolute Maximum Ratings

VCC	-0.3V~30V
HV	-0.3V~500V
COMP, OTP, CS	-0.3V ~6V
OUT	-0.3V ~Vcc+0.3V
Power Dissipation, PD@85°C	
SOP-8/SOP-7	250mW
Package Thermal Resistance	
SOP-8/SOP-7,ΘJA	160 °C/W
Junction Temperature	150°C
Lead Temperature (Soldering, 10sec)	260°C
Storage Temperature Range	-55°C to 125°C
ESD Voltage Protection, Human Body Model (except HV Pin)	2.5KV
ESD Voltage Protection, Machine Model (except HV Pin)	250V
ESD Voltage Protection, Human Body Model (HV Pin)	1KV
ESD Voltage Protection, Machine Model (HV pin)	200V
Gate Output Current	+500/-800mA

Recommended Operating Conditions

Supply Voltage Vcc	10V to 24V
VCC Capacitor	10 to 47μF
HV Pin Resistor	5~10kΩ
COMP Capacitor Value	1~100nF
Operating Ambient Temperature	-40°C to 85°C
Operating Junction Temperature Range	-40°C to 125°C

Note:

1. COMP pin connecting a capacitor is essential to filter out the undesired switching noise for stable operation.
2. The small signal components as closed to IC pin as possible.

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)					
High-Voltage Current Source	Vcc< UVLO(on), HV=500V	2		4.5	mA
HV Pin Total Input Current	HV=500Vdc,Vcc>UVLO(on),			45	μA
HV Pin Brown –In Level(HVBI)	HV pin = rectifier wave increase	89	95.0	101	Vac(peak)
HV Pin Brown-out Level(HVBO)	HV pin = rectifier wave decrease	71.9	76.5	81.1	Vac(peak)
Brown-in De-bounce Time		160	210	260	μs
Brown-out Detection Debounce Time		45	55	65	ms
HV Discharge capability	HV=500V,Vcc < UVLO(on) - 1	2		4.5	mA
Supply Voltage (Vcc Pin)					
Startup Current	Vcc=15V ,HV=500V	160		300	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=3V	1.5	2.0	2.5	mA
	V_{COMP}=0V	0.30	0.62	0.65	mA
	OLP,OVP Tripped	0.3	0.4	0.5	mA
UVLO (off)		8.0	8.5	9.0	V
UVLO (on)		16.0	17.0	18.0	V
PDR		6	6.5	7.0	V
Vcc OVP Level		25.00	26.25	27.50	V
Voltage Feedback (Comp Pin)					
Short Circuit Current	V_{COMP}=0V	105	125	145	μA
Open Loop Voltage	COMP pin open	5.1	5.3	5.5	V
OLP Tripped Level		4.4	4.6	4.8	V
Fix Frequency Mode Threshold(*)		-	2.8	-	V
Green Mode Threshold(*)		-	2.3	-	V
Zero Duty Threshold VCOMP	Zero Duty,V_{FB_B}	1.69	1.80	1.91	V
	Zero Duty-recover	1.80	1.90	2.00	V
Current Sensing (CS Pin)					
Maximum Input Voltage, V_{CS_OFF}		0.620	0.650	0.680	V
Maximum Input Voltage, V_{CS_MIN}	For High Line	0.445	0.475	0.515	V
Leading Edge Blanking Time	-20°C ~125°C	150	215	280	ns
Delay to Output		50	100	150	ns

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency					
Frequency		62	65	68	KHz
Trembling Frequency		±4	±5	±6	%
Green Mode Frequency		23.6	25.6	27.6	KHz
Fsw Temp. Stability(*)	-40°C ~105°C	-	5	-	%
Fsw Voltage Stability(*)	Vcc=UVLO(off)~(Vcc OVP-1V)	-	1	-	%
Maximum Duty		70	75	80	%
Gate Drive Output (OUT Pin)					
Output Low Level	V_{CC}=15V, Io=20mA	0	-	1	V
Output High Level	V_{CC}=15V, Io=20mA	9	-	Vcc	V
Rising Time(*)	Load Capacitance=1000pF, 4V~90% Output High Level	-	100	-	ns
Falling Time(*)	Load Capacitance=1000pF	-	48	-	ns
OUT Pin Clamping Voltage	V_{CC}=21V,1nF on OUT pin	14	15	16	V
OLP (Over Load Protection)					
OLP Delay Time	Auto restart, F_{SW}=65KHz	57	63	69	ms
OLP De-Latch Counter	Auto-Restart Mode	-	2	-	
Soft Start					
Soft Start Duration		3	4	5	ms
External Over Temperature Protection(OTP Pin)					
OTP pin Source Current		46	50	54	μA
Turn-on Tripped Level (VOTP_on)		0.500	0.525	0.550	V
Turn-off Tripped Level (VOTP_off)		VOTP_ON-0.05			V
OTP Detect De-bounce cycle		-	16	-	PWM cycle
De-latch Level		UVLO(off)/AC-off			
Internal OTP					
OTP Tripped Level(T_{OTP}) (*)		-	140	-	°C
OTP Hysteresis(*)		-	T_{OTP}-30	-	°C
OTP Protection		Auto Recovery by Vcc UVLO			

Notes:

*Guaranteed by design.

Typical Performance Characteristics

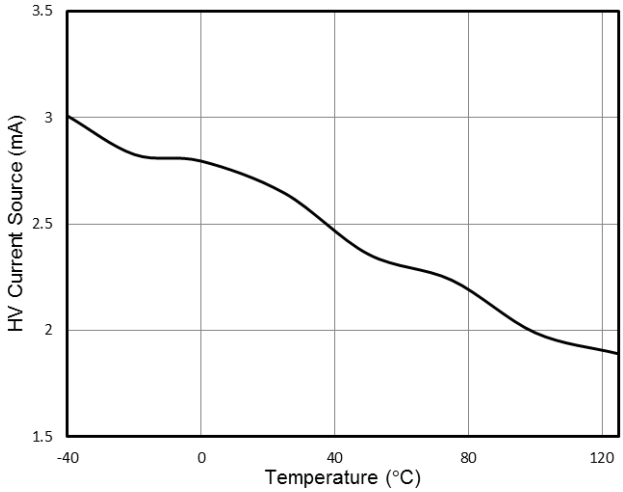


Fig. 1 IHV vs. Temperature (HV=500V, V_{CC}=15V)

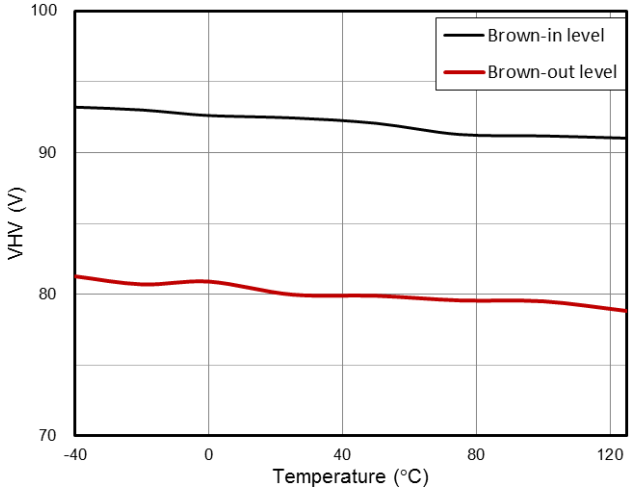


Fig. 2 BNO level vs.Temperature

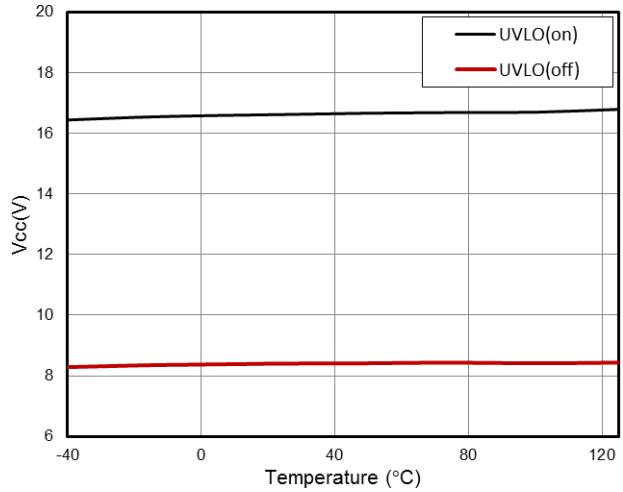


Fig. 3 UVLO level vs.Temperature

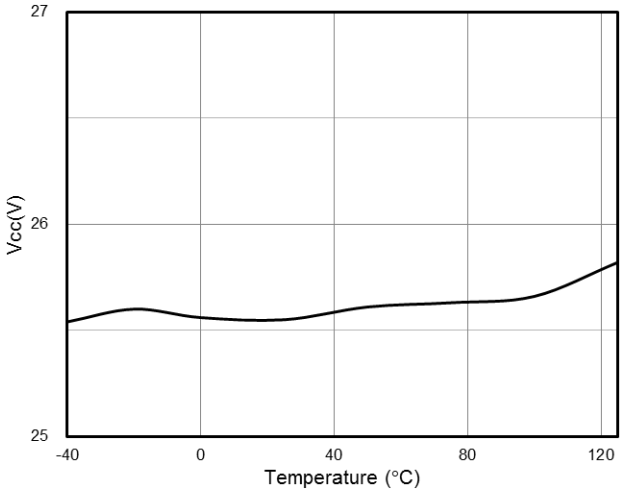


Fig. 4 Vcc OVP Level vs.Temperature

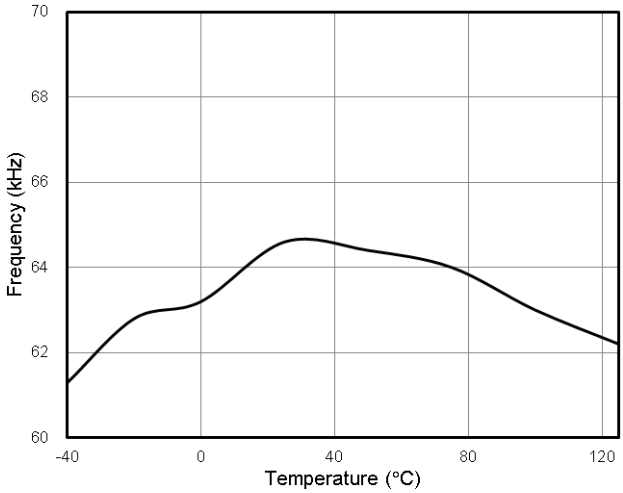


Fig. 5 Frequency vs.Temperature

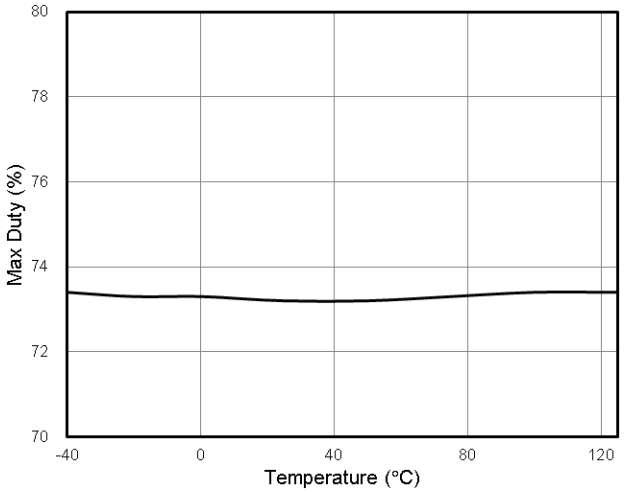


Fig. 6 Max Duty vs.Temperature

Typical Performance Characteristics

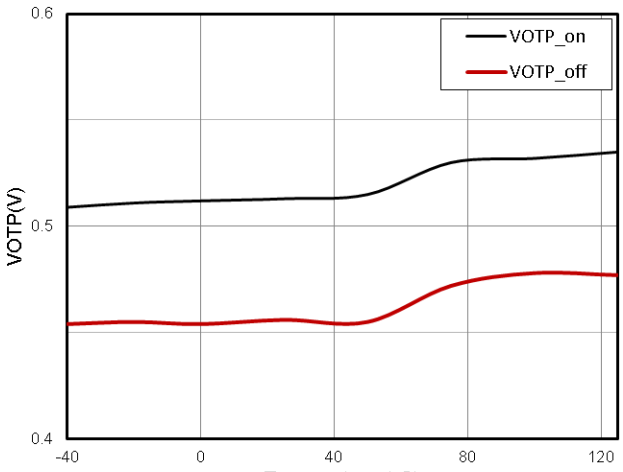


Fig. 7 External OTP level vs.Temperature

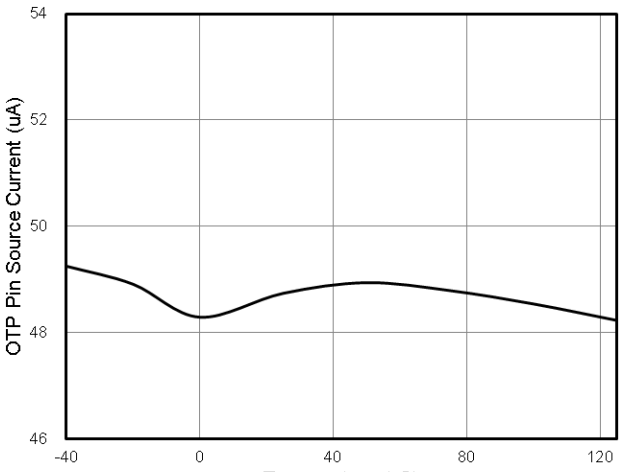


Fig. 8 OTP Pin Source Current vs.Temperature

Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation force the PWM controllers need to be powerful to integrate more functions to reduce the external part counts. The LD7765 is ideal for these applications to provide an easy and cost effective solution; its detailed features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes much significant power to meet the current power saving requirement. In most cases, startup resistors carry larger resistance and spend more time to start up.

As shown in Fig 9, LD7765 is implemented with a high-voltage startup circuit with it to minimize power loss on startup circuit. During the startup transient, a high-voltage current source sinks current from AC Line or Neutral to provide the startup current and charge the Vcc capacitor C1 the same time.

See in Fig 10. Once VCC voltage rises up to reach the UVLO(on) threshold, HV pin will stop charging the VCC capacitor and BNO will detect the AC line status. In the meantime, VCC voltage begins to fall and consumes less current for operation from 0.6mA to 300μA as it's falling to UVLO(off)

As VCC trips UVLO(off), HV pin will recharge VCC capacitor till VCC voltage rises back to UVLO(on) again. Since then, HV pin would no longer charge the capacitor and instead, send a gate drive signal to draw supply current for VCC from the auxiliary winding of the transformer. That minimizes the power loss on the start-up circuit successfully.

By using such configuration, the turn-on delay time will be almost same no matter under low-line or high-line conditions.

An UVLO comparator is embedded to detect the voltage across Vcc pin to ensure the supply voltage enough to power on the LD7765 and in addition to drive the power MOSFET. As shown in Fig 10, a hysteresis is provided to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 17V and 8.5 V, respectively.

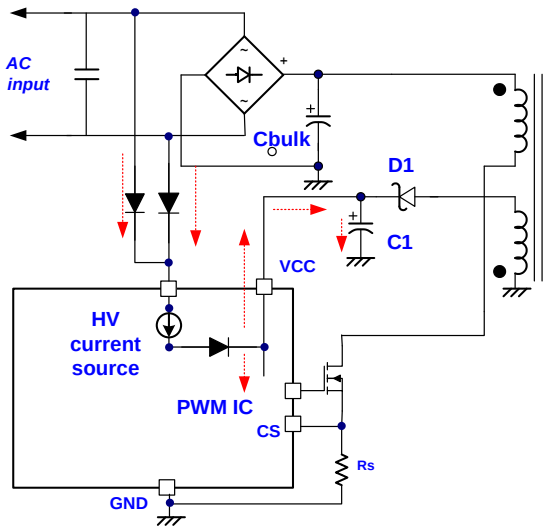


Fig 9.

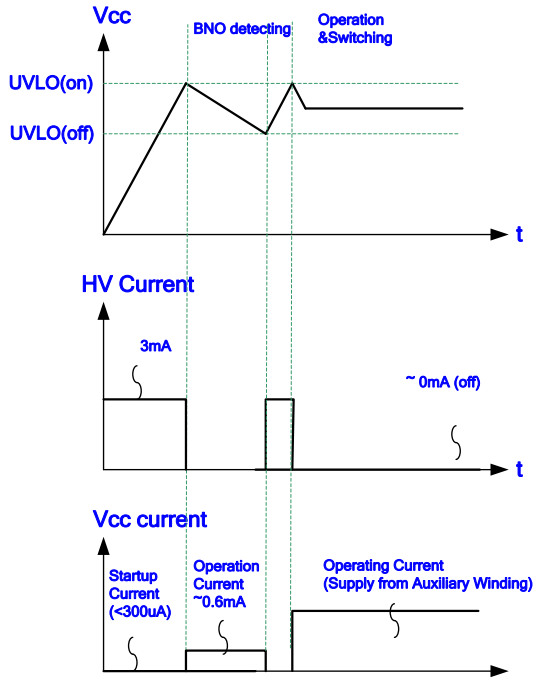


Fig 10.

Brown In/ Out Protection

The LD7765 features Brown-in / Brown-out protection on HV pin. As the built-in comparator detects line voltage, it will turn off the controller to prevent from any damage. In case V_{HV}<VHBO, the gate output will be disabled even when the VCC already reach $UVLO_{(ON)}$. It therefore forces VCC hiccup between $ULVO_{(ON)}$ and $UVLO_{(OFF)}$. Unless the line voltage is large enough and over HVBI VAC, the gate output will not start switching even as the next $ULVO_{(ON)}$ is tripped. A hysteresis is designed to prevent from false-triggering and damage to the external components during turn-on and turn-off transient. See Fig 11 for the operation.

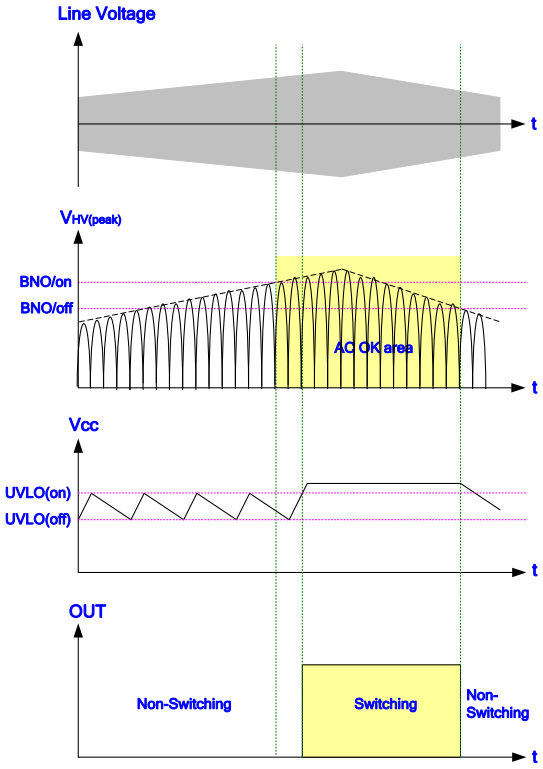


Fig 11.

Current Sensing, Leading-Edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD7765 detects the primary MOSFET current across the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.65V (typ.). Thus the MOSFET peak current can be calculated as:

$$I_{PEAK\,(MAX)} = \frac{0.65V}{R_S}$$

A 250ns (typical) leading-edge blanking (LEB) time is provided in the input of CS pin to prevent false-triggering from the current spike. In the low power applications, the total pulse width of the turn-on spike is determined by the output power, circuit design and PCB layout. It is strongly recommended to add a small R-C filter (as shown

in Fig 12) for large power applications to avoid the VCS < -0.3V from being damaged by the negative turn-on spike.

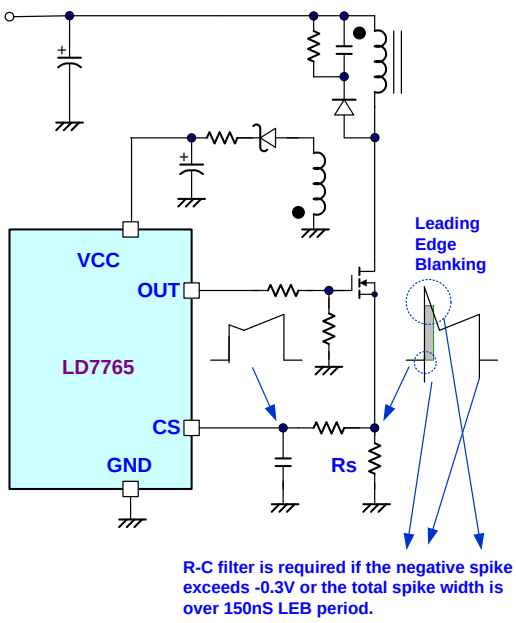


Fig 12.

OCP Compensation Design Tip

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD7765 detects the primary MOSFET current across the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit.

In general, the power converter provides various current in reflect to the input voltage during signal propagation delay time. To compensate it, LD7765 varies the current limit in corresponding to Vcs_off with the duty cycles. As shown Fig 13, Vcs_off (corresponding to current limit) is in direct proportion to duty ratio in certain segment and is fixed at high or low as duty ratio is over or below threshold values respectively. As a result, the current limit will be reduced at high-line inputs. This compensation control mechanism is developed and protected with Leadtrend's patents. (Patent pending),

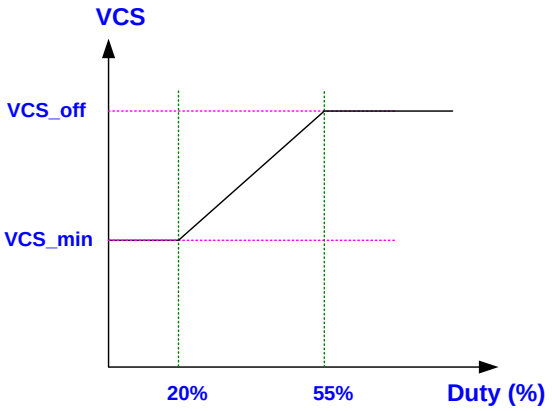


Fig 13.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 on the secondary side through the photo-coupler to the COMP pin of LD7765 The input stage of LD7765, like UC384X, is with 2 diodes voltage offset to feed the voltage divider with 1/4 ratio, that is,

$$V_{CS(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally to optimize the external circuit.

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is operated for more than 50%. To stabilize the control loop, the slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. In LD7765, the internal slope compensation circuit has been implemented for a compact external circuit design.

Oscillator and Switching Frequency

The switching frequency of LD7765 is fixed at 65KHz to provide optimized operations in considering the EMI performance, thermal treatment, component sizes and transformer design. The frequency swapping is internally pre-set for ±4kHz when incorporating with 65KHz switching frequency.

Green-Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own IP.

Maximum Duty-Cycle

The maximum duty-cycle of LD7765 is limited to 75% to avoid the transformer saturation.

On/Off Control

The gate driver of LD7765 can be disabled immediately by pulling COMP pin voltage level lower than Zero Duty Trip Level. The disable-mode can be released when Comp pin voltage level is pulled high above Zero Duty Trip Level.

Over Load Protection (OLP)- Auto Recovery

To protect the circuit from being damaged at over load condition, short or open loop condition, the LD7765 is implemented with smart OLP function. LD7765 features auto recovery function, see Fig 14 for the waveform. In the example of the fault condition, the feedback system will force the voltage loop enter toward saturation and then pull the voltage high across COMP pin (VCOMP). When the VCOMP ramps up to the OLP tripped level (4.6V) for more than the OLP delay time, the protection will be activated to turn off the gate output and to stop the switching of power circuit. The OLP delay time is set by internal high frequency counter. It is to prevent the false triggering during the power-on and turn-off transient.

A divide-2 counter is implemented to reduce the average power under OLP behavior. Whenever OLP is activated, the output is latched off and the divide-2 counter starts to count the number of UVLO(off). The latch will not be released and the output will not be resumed until the 3rd UVLO(off) level is tripped. With the protection mechanism, the average input power will be less than ever, so that the component temperature and stress can be controlled within the safe operating area.

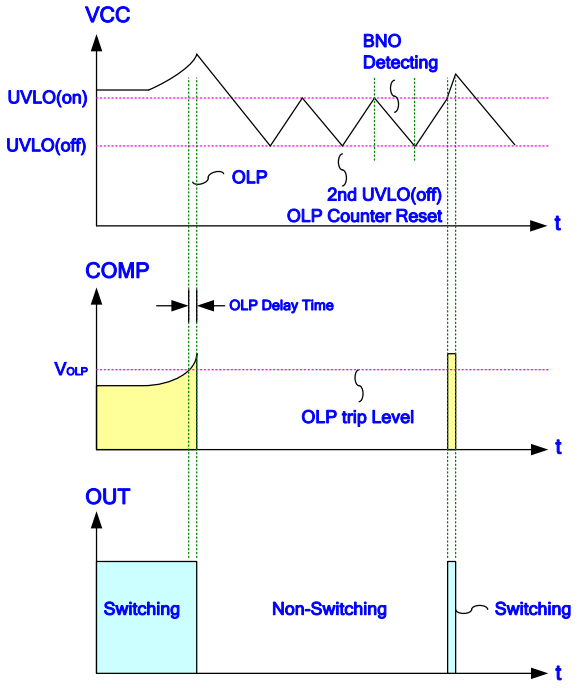


Fig 14.

OVP (Over Voltage Protection) on Vcc - Auto Recovery

The maximum Vcc ratings of the LD7765 are mostly for 30V. To protect the controller in over-voltage condition, LD7765 is implemented with OVP function on VCC. Once the VCC voltage ramps over the OVP threshold, it will shut off the output gate drive circuit right away and disable the power MOSFET until the 2nd UVLO(ON) is tripped.

The Vcc OVP function is auto-recoverable. If the OVP condition, usually caused by open-loop of feedback, is not released, the Vcc will trip the OVP level again and re-shutdown the output to resume. That makes the Vcc work in hiccup mode. Fig 15 shows its operation.

After the OVP condition is removed, the Vcc will resume its operation level and the output in the normal operation.

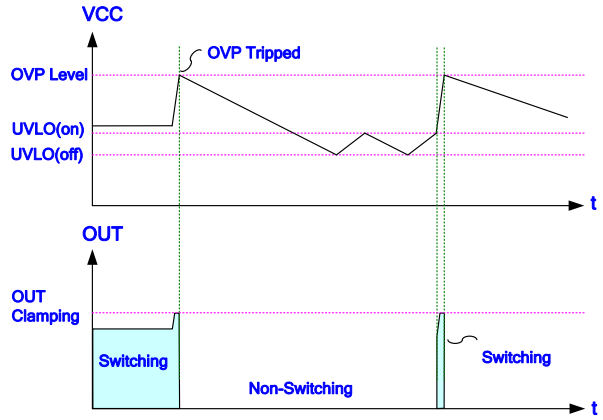


Fig 15.

On-Chip OTP - Auto Recovery

An internal OTP circuit is embedded in the LD7765 to provide the worst-case protection for this controller. When the chip temperature ramps higher than the trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window.

X-Cap Discharge Function

The EMI filter has a paralleled discharging resistor across X-capacitor. To meet Safety requirement, this component is required to be discharged in less than 1sec, that is,

$$\tau_{Discharge} = C_{X-Cap} \times R_{Discharge} \leq 1sec$$

The power loss of this resistor is in direct proportion to square of input voltage. For example, if the input voltage is 264Vac and the discharging resistance ~ 2MΩ, 35mW power loss can be calculated by follow equation.

$$P_{Loss} = \frac{V_{AC(RMS)}^2}{R_{Discharge}}$$

To eliminate the significant power loss from this discharging resistor, LD7765 applies the innovative patent technology to discharge X-cap's energy through HV current source when AC line is disconnected. Fig 16 shows the operation.

Applying this technology, the system can easily pass the safety test without discharging resistor and reduced power loss

After the plug is pulled out, the AC voltage on X-cap would still remain. The LD7765 senses the HV pin to detect the state of the AC voltage on X-cap. LD7765 sets a threshold voltage to judge whether the AC voltage on X-cap is higher than this threshold with no rising cross in a de-bouncing time. If so, LD7765's HV device will sink constant current source to GND. This discharging function is applicable at all load conditions in a de-bouncing time of X-cap function around 55ms.

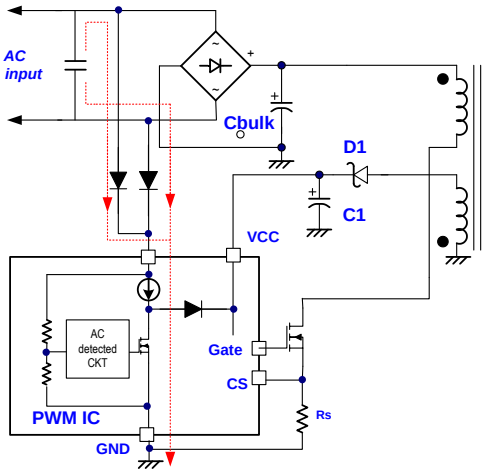


Fig 16.

External OTP - Latched Mode Protection

The OTP circuit is implemented to sense whether there is any hot-spot of power circuit like power MOSFET or output rectifier. Once an over-temperature condition is detected, the OTP is enabled to shut down the controller to protect the controller.

Typically, a NTC is recommended to connect with OTP pin. The NTC resistance will decrease as the device or ambient in high temperature. The relationship is as below.

$$V_{OTP} = 50\mu A \cdot R_{NTC}$$

When V_{OTP}<VOTP-off (typ. 0.5V), it will trigger the protection to shut down the gate output and latch off the power supply. The controller will remain latched unless

the Vcc drops below PDR (power down reset) and Vcc stay on UVLO condition. Two conditions are required to restart the IC successfully, cool down the circuit so that the NTC resistance will increase and raise V_{OTP} above 0.525V. Then re-plug on AC power. The detailed operation is show in Fig 17.

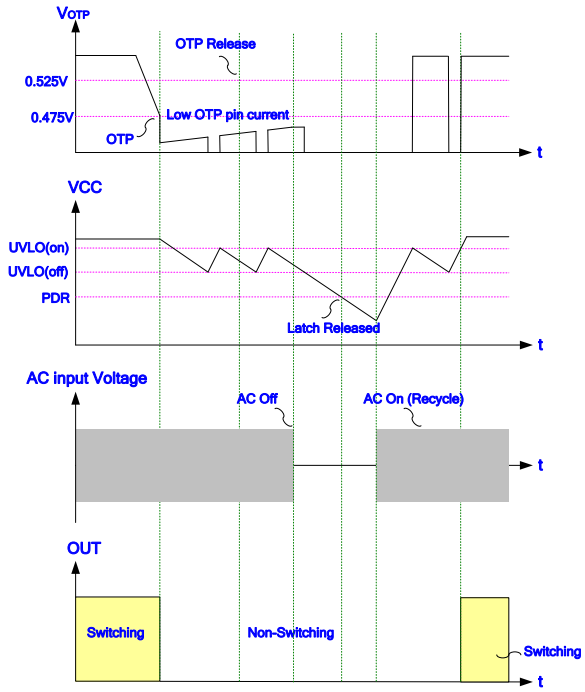


Fig 17.

Pull-Low Resistor on the Gate Pin of MOSFET

The LD7765 consists of an anti-floating resistor on the OUT pin to protect the output from abnormally operation or false triggering by MOSFET. Even so, we still recommend to add an external one on the MOSFET gate terminal to provide more protection in case of disconnection of gate resistor R_G during power-on.

In such single-fault condition, as shown in Fig 18, the resistor R8 can provide a discharge path to avoid the MOSFET from being false-triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the MOSFET should be pulled low and placed in the off-state no matter that the gate resistor is disconnected or opened.

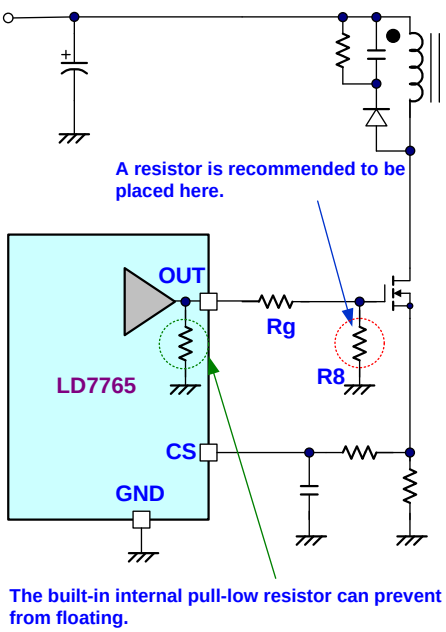


Fig 18.

MOSFET Characteristic

The MOSFET is divided into three operation regions, ohmic region, saturation region, and the cut-off region, shown as Fig 19.

For switching power supply applications, it shall operate in ohmic and cut-off region. Never reach the region of saturation; it would cause damage for acting beyond the maximum safety operating area. It's necessary to check the characteristic of MOSFET.

Fig 20 shows a totem pole architecture for the circuit of OUT. The output high level of OUT is at around VCC-1.5V. The maximum voltage for VS is equal to V_{CS_OFF}. So we obtain the minimum VGS high level ($VGS_{H(MIN)}$) as below.

$$VGS_{H(MIN)} = UVLO(off) - 1.5 - Vcs\_off$$

The maximum peak current of MOSFET can be calculated as:

$$I_{PEAK\,(MAX)} = \frac{Vcs\_off}{R_S}$$

Refer to on-region characteristics of the MOSFET (like Fig 19), check the saturation current of $VGS_{H(MIN)}$ to make

sure the saturation current is higher than $I_{PEAK(MAX)}$. In order not to decrease the voltage across VG, it's recommended not to connect a forward diode between the gate of the MOSFET and OUT pin, for example like Fig 21.

In addition, pulling VCC level high can keep VGS_H in high level, for example:

1. Refer to Fig 20, increase N_X to pull VCC level high.
2. Refer to Fig 22, increase VCC capacitance to improve VCC's performance to drop at startup transient, shows as Fig 22.

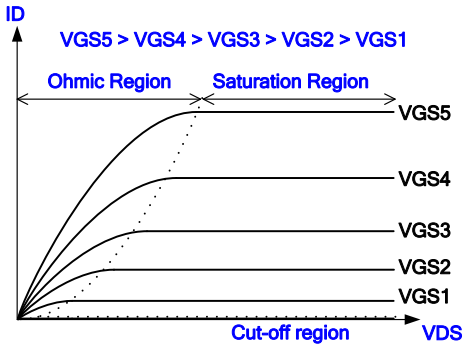


Fig 19.

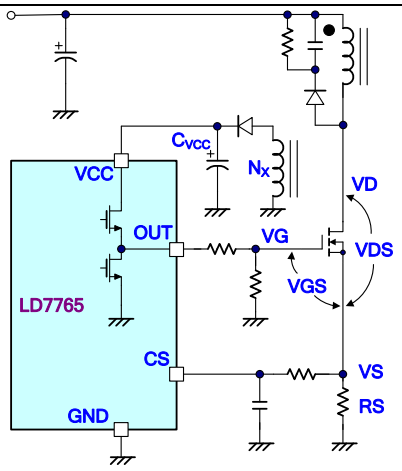


Fig 20.

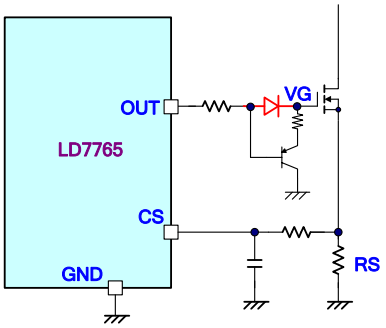


Fig 21.

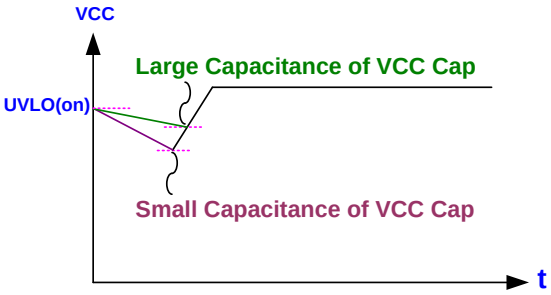
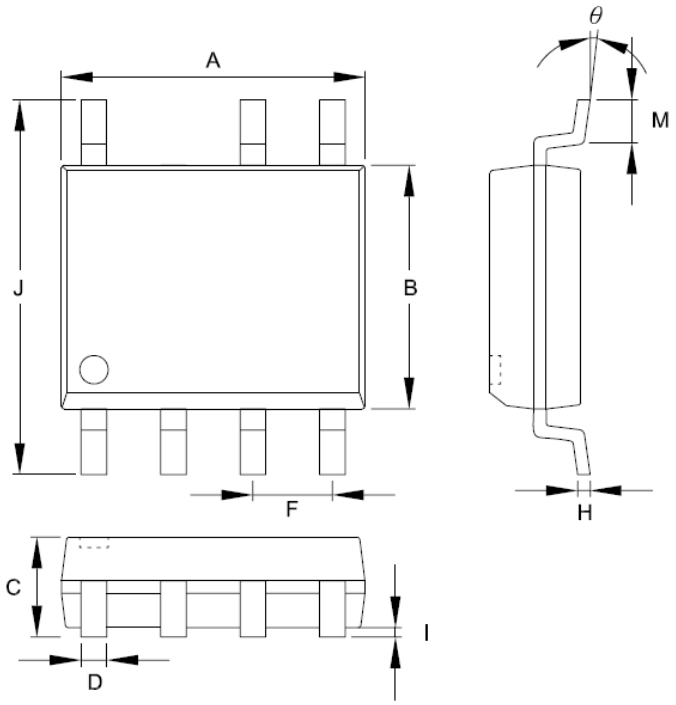


Fig 22.

Package Information

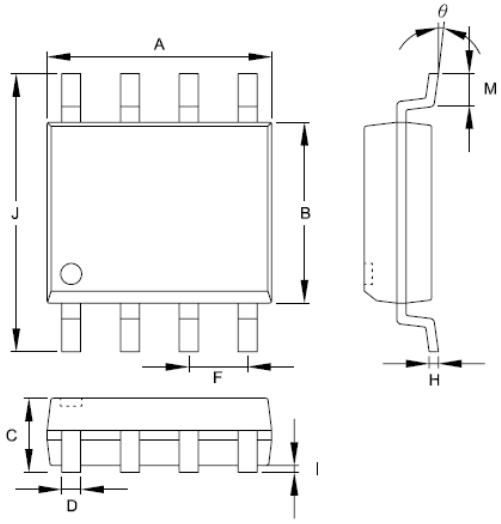
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	10/29/2012	Original Specification.