LD7820

04/08/2012

Primary-Side PWM Controller with CV/CC Operation for LED

REV:00

General Description

The LD7820 is a primary-side feedback controller in CV/CC operation for LED lighting applications. It minimizes the components counts and is available in tiny packages. Those make it an ideal design for low cost applications.

The LD7820 provides constant voltage, constant current (CV/CC) operation requiring neither photo-coupler nor secondary control circuit. Also, the LD7820 features OTP (Over Temperature Protection) and OVP (Over Voltage Protection) to prevent the circuit from being damaged under abnormal conditions.

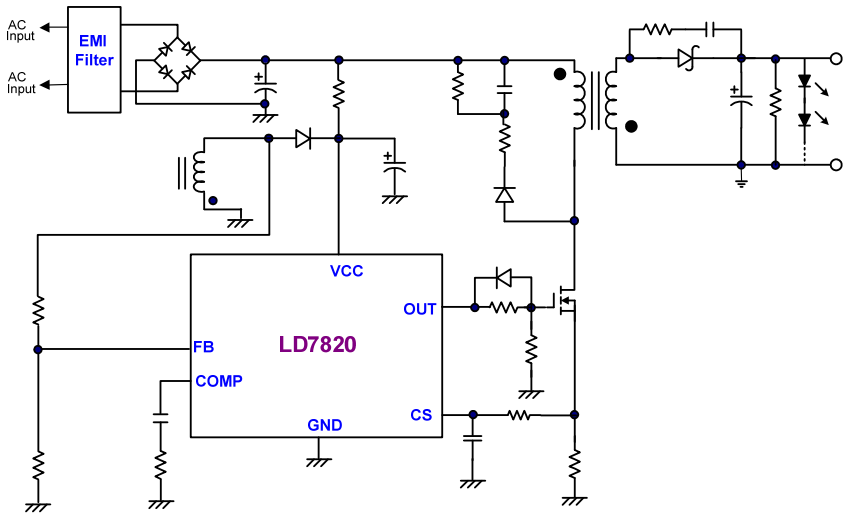
Features

- Primary-side Feedback Control
- Constant Current Control
- Built-in Load Regulation Compensation
- Built-in Primary Winding Inductance Compensation
- Low Startup Current (<16μA)
- Current Mode Control with Cycle-by-Cycle Current Limit
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- OVP (Over Voltage Protection) on Vcc
- OTP (Over Temperature Protection)
- 300mA Driving Capability

Applications

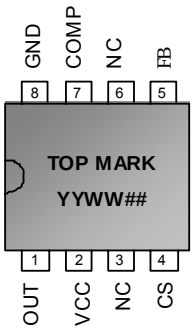
- AC-DC LED Driver

Typical Application

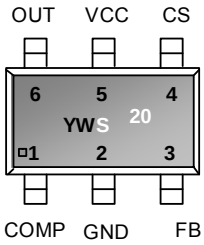


Pin Configuration

DIP-8 (TOP VIEW)



SOT-26 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005.....)
WW, W: Week code
: Production family code
S20 : LD7820

Ordering Information

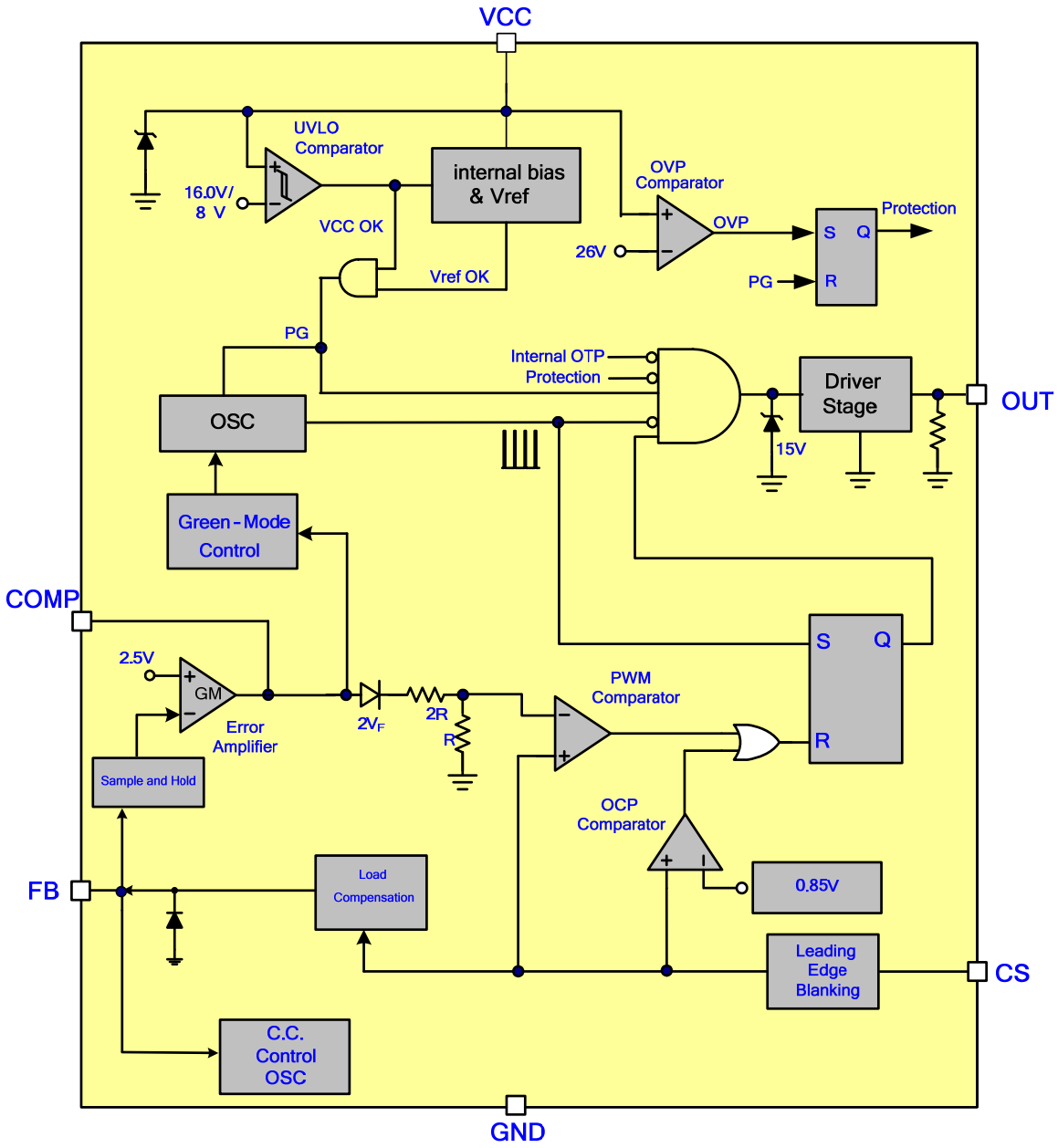
Part number	Package	TOP MARK	Shipping
LD7820 GL	SOT-26	YWS/20	3000 /tape & reel
LD7820 GN	DIP-8	LD7820GN	3600 /tube /Carton

The LD7820 is green packaged.

Pin Descriptions

NAME	PIN (SOT-26)	Pin (DIP-8)	FUNCTION
COMP	1	8	Output of the error amplifier for voltage compensation
GND	2	7	Ground
FB	3	5	Voltage Feedback Sense. This pin detects the output voltage information based on voltage of auxiliary winding.
CS	4	4	Current sense pin, connect to sense the MOSFET current
VCC	5	2	Supply voltage pin
OUT	6	1	Gate drive output to drive the external MOSFET
NC	–	3	Not connected
NC	–	6	Not connected

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC,	-0.3 ~29V
OUT	-0.3 ~VCC+0.3
COMP, FB, CS	-0.3 ~6V
Maximum Junction Temperature	150°C
Operating Ambient Temperature	-40°C to 85°C
Operating Junction Temperature	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	250°C/W
Package Thermal Resistance (DIP-8, θ_{JA})	100°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	160mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	400mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage Vcc	9	24	V
Start-up capacitor	2.2	22	μF

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)					
Startup Current			10	16	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		1.8		mA
	V_{COMP}=3.5V,		3.0		mA
	OVP tripped		0.65		mA
UVLO (off)		7.0	8	9	V
UVLO (on)		15	16	17	V
Vcc OVP Level		25	26	27	V
Error Amplifier (CV mode, Comp pin, FB pin)					
Reference Voltage, Vref		2.47	2.500	2.53	V
Transconductance			14		μmho
Output Sink Current	V_{FB}=3.2V, V_{COMP}=2.5V		75		μA
Output Source Current	V_{FB}=1.8V, V_{COMP} =2.5V		-75		μA
Output Upper Clamp Voltage	V_{FB}=2.3V	4.0	4.1	4.2	V
Load Compensation Current	V_{CS}=0.75V	10.5	13.5	16.5	μA
Load Compensation Cut-off Voltage	Load compensation current=0A*		0.2		V
Sample and Hold					
Sampling Delay Time	*		1.8		μs
Sampling Time	*		0.4		μs
Current Sensing (CS Pin)					
Maximum Input Voltage, Vcs(off)		0.83	0.85	0.87	V
Vcs-min	V_{COMP} < 1.8V		0.2		V
Leading Edge Blanking Time		350	420	490	ns
Input impedance		1			MΩ
Delay to Output	*		80		ns

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency (CV mode, COMP Pin)					
Frequency	COMP=3.6V	61	65	69	kHz
Green Mode Frequency		18	20	24	kHz
Minimum Frequency		0.9	1.4	1.8	kHz
Trembling Frequency	COMP=3.6V		± 4		kHz
Temp. Stability	(-20°C ~125°C)*		5		%
Voltage Stability	(V_{CC}=9V-24V)*		1		%
Maximum Frequency Mode Threshold VCOMP, V_{Smax}	*		3.0		V
Green Mode Threshold V_{COMP1}, V_{SG1}	*		2.7		V
Green Mode Threshold V_{COMP2}, V_{SG2}	*		1.9		V
Minimum Frequency V_{COMP}, V_{Smin}	*		1.6		V
Oscillator for Switching Frequency (CC mode)					
Max. Frequency		61	65	69	kHz
Minimum Frequency		18	20	24	kHz
Trembling Frequency			± 6		%
Gate Drive Output (OUT Pin)					
Output Low Level	V_{CC}=15V, Io=20mA	0		1	V
Output High Level	V_{CC}=15V, Io=20mA	8		VCC	V
Rising Time	V_{CC}=15V C_L=1000pF		200	350	nS
Falling Time	V_{CC}=15V C_L =1000pF		80	150	nS
Output High Clamp Level	Vcc=20V	14	16	18	V
Maximum duty		55	60	65	%
On Chip OTP (Over Temperature)					
OTP Level	*		140		°C
OTP Hysteresis	*		30		°C

*: These parameters are guaranteed by design.

Typical Performance Characteristics

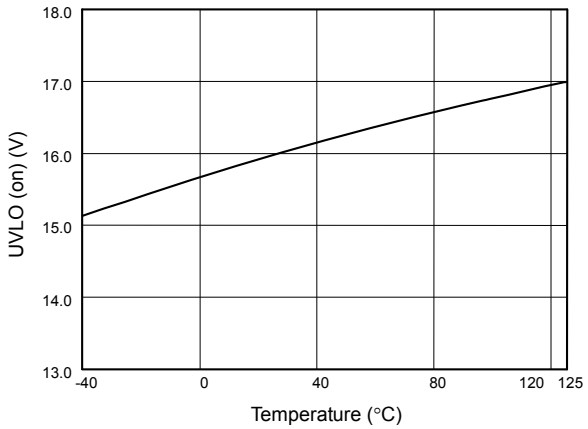


Fig. 1 UVLO (on) vs. Temperature

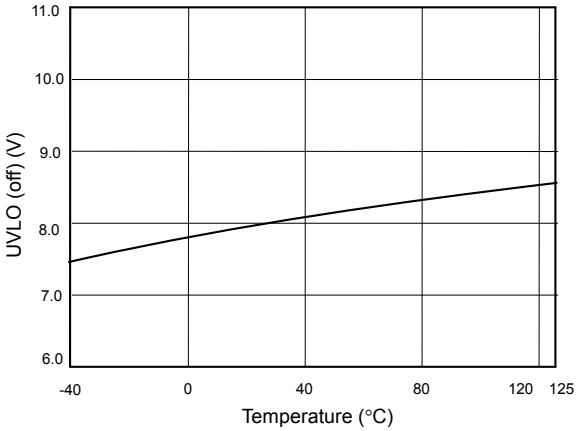


Fig. 2 UVLO (off) vs. Temperature

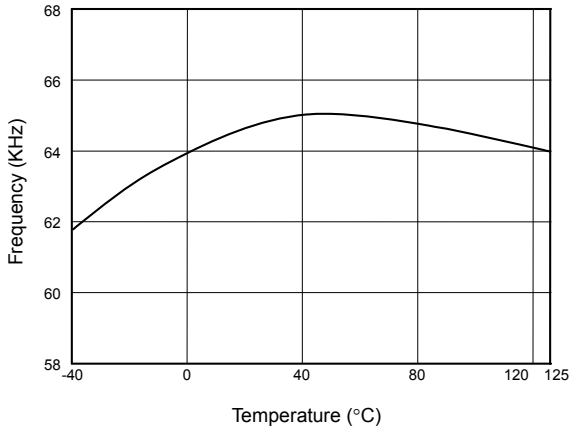


Fig. 3 Frequency vs. Temperature

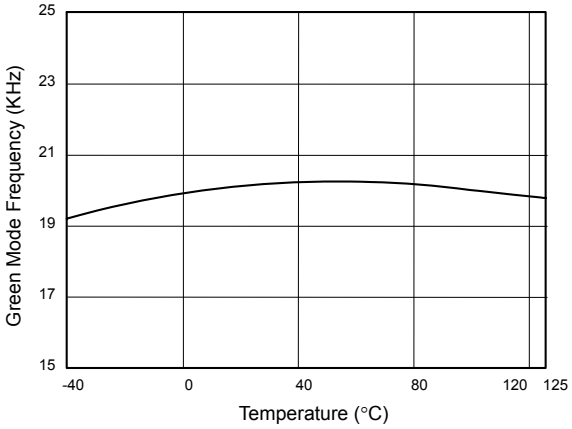


Fig. 4 Green Mode Frequency vs. Temperature

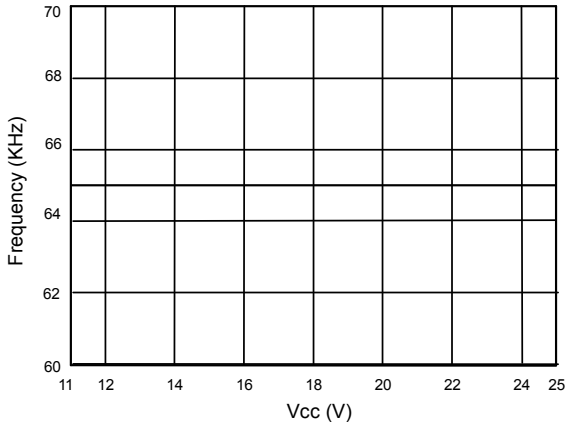


Fig. 5 Frequency vs. Vcc

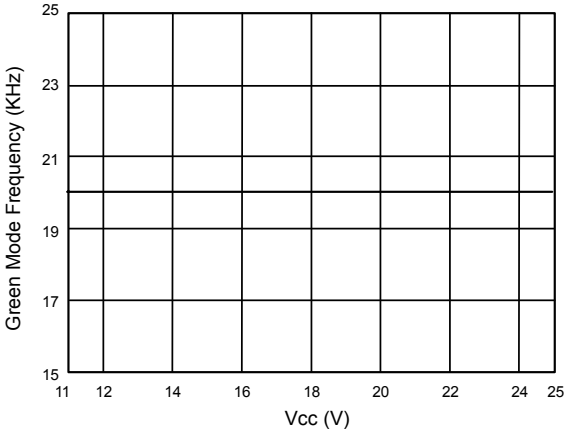


Fig. 6 Green Mode Frequency vs. Vcc

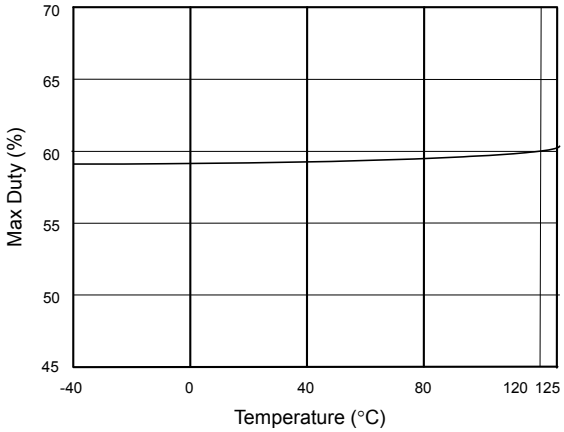


Fig. 7 Max Duty vs. Temperature

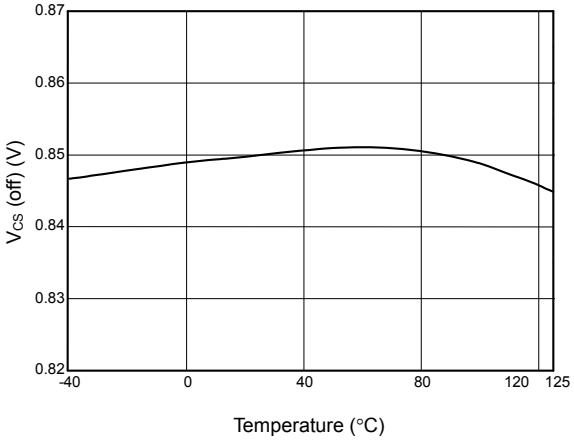


Fig. 8 V_{CS} (off) vs. Temperature

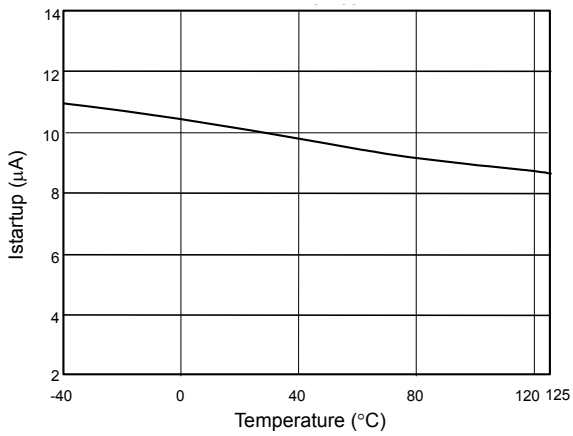


Fig. 9 Startup Current (Istartup) vs. Temperature

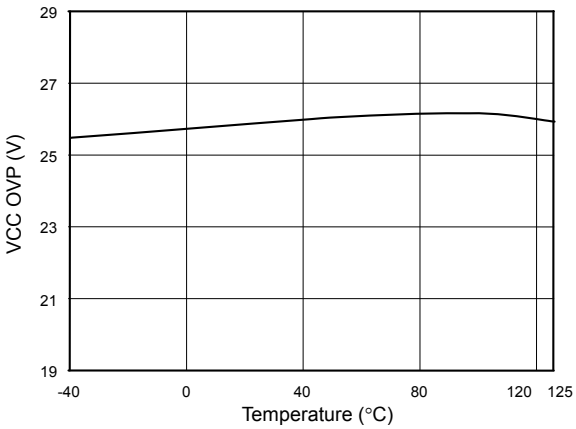


Fig. 10 VCC OVP vs. Temperature

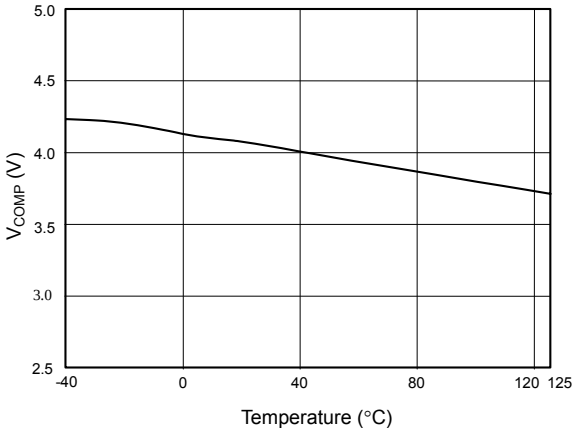


Fig. 11 V_{COMP} open loop voltage vs. Temperature

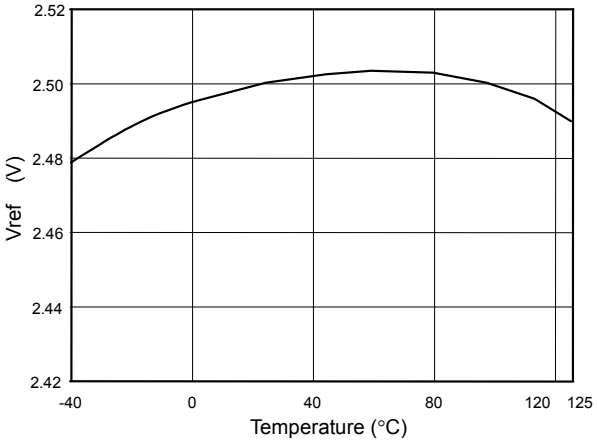


Fig. 12 Vref vs. Temperature

Application Information

Operation Overview

The LD7820 is an excellent primary-side feedback controller in C.V./C.C. operation for the off-line low power AC/DC applications of battery chargers and adapters. It meets the green-power requirement and is intended for the use in those modern switching power suppliers and linear adaptors that demand higher power efficiency and power-saving. The LD7820 provides constant voltage, constant current (CV/CC) operation requiring neither photo-coupler nor secondary control circuit. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented to detect the voltage on VCC pin. It would assure the supply voltage enough to turn on the LD7820 PWM controllers and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is built in to prevent shutdown from the voltage dip during startup.

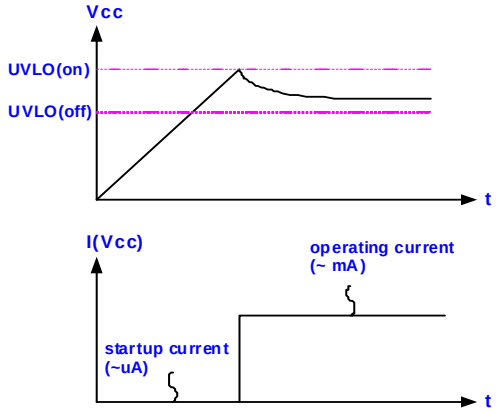


Fig. 13

Startup Current and Startup Circuit

The typical startup circuit to generate the LD7820 Vcc is shown in Fig. 14. During the startup transient, the Vcc is below UVLO threshold thus there is no gate pulse produced from LD7820 to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the Vcc voltage is high enough to turn on the LD7820 and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD7820 requires only 10μA (Typ.). If a higher resistance value of R1 is chosen, it usually takes more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time. If less start-up time is required, a two-step start-up circuit is recommended for it, as shown in Fig. 15. In this circuit example, a smaller capacitor C1 can be used to minimize startup time. The energy supporting the controller after start-up is mainly from a larger capacitor C2.

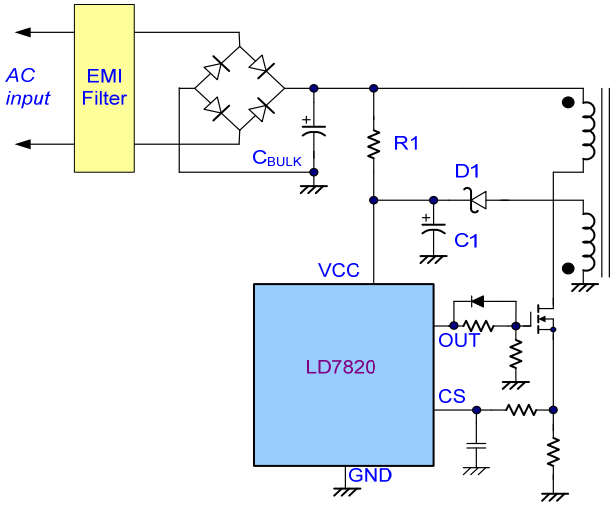


Fig. 14

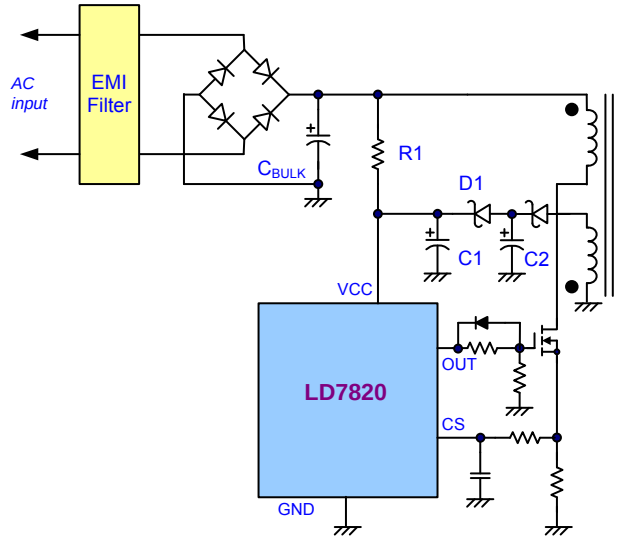


Fig. 15

Principle of CV Operation

In the DCM flyback converter, the output voltage can be sensed by the auxiliary winding. LD7820 samples the auxiliary winding on the primary-side to regulate the output voltage, as shown in the Fig 16. The voltage induced in the auxiliary winding is a reflection of the secondary winding voltage while the MOSFET is in off state. Via a resistor divider connected between the auxiliary winding and FB pin, the auxiliary voltage is sampled after the sample delay time and will be hold until the next sampling. The sampled voltage is compared with internal reference V_{ref} (2.5V) and the error will be amplified. The error amplifier output COMP reflects the load condition and controls the duty cycle to regulate the output voltage, thus constant output voltage can be achieved. The output voltage is given as:

$$V_{OUT} = 2.5V(1+\frac{Ra}{Rb})(\frac{Ns}{Na}) - V_F$$

Where V_F indicates the drop voltage of the output Diode, Ra and Rb are top and bottom feedback resistor value, Ns and Na are the turns of transformer secondary and auxiliary.

In case that the output voltage is sensed through the auxiliary winding; the leakage inductance will induce ringing to affect output regulation. Optimizing the drain voltage clamp circuit to minimize the high frequency ringing will achieve the best regulation. Fig. 17 shows the desired drain voltage waveform in compare to Fig. 18 with a large undershoot due to the leakage inductance induced ring. This will make the sample error and cause poor performance for output voltage regulation. A proper selection for resistor R_S, in series with the clamp diode, may reduce any large undershoot, as shown in Fig. 19.

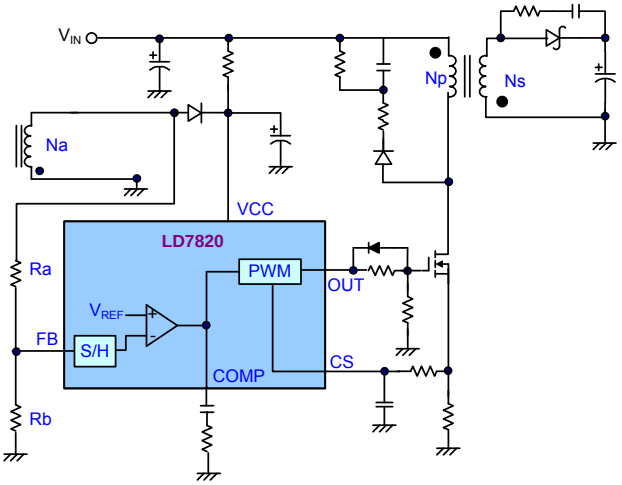


Fig.16

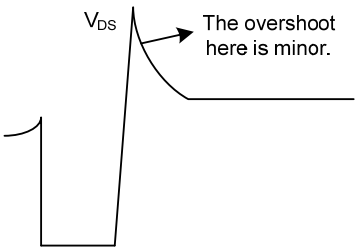


Fig.17

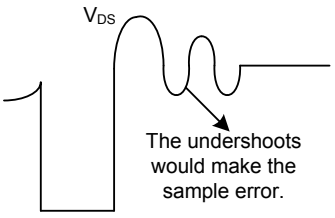


Fig.18

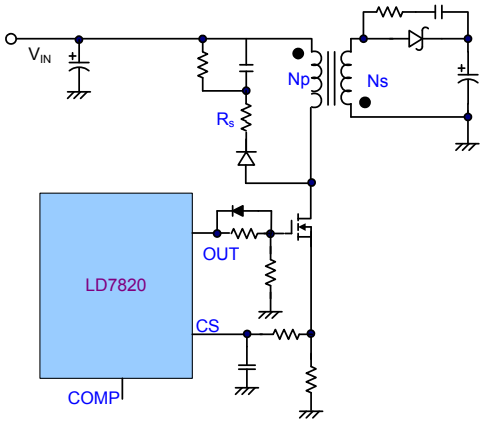


Fig.19

Load Regulation Compensation

In LD7820, load regulation compensation is implemented to compensate the cable voltage droop and to achieve a better voltage regulation. An offset voltage is generated at FB by an internal sink current source flowing into the FB during the sample period. The built-in sink current source is proportional to the peak value of Vcs. As a result, it is proportional to the output load current, thus the drop due to the cable loss can be compensated. As the load current decreases from full-load to no-load, the offset voltage at FB will decrease. It can also be programmed by adjusting the resistance of the divider to compensate the drop for various cable lines used. The equation of internal sink current source is shown as:

$$I_{FB} = (V_{CS,pk} - 0.2) * 24.5\ (\mu A)$$

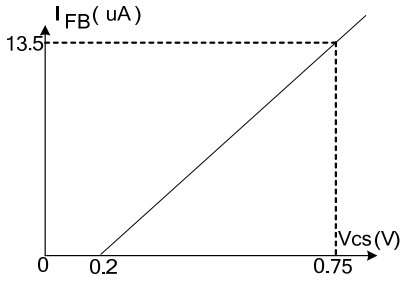


Fig. 20

Principle of C.C. Operation

To support with the proprietary CC/CV control of the LD7820, a system designed in DCM mode is required for flyback converter, as shown in Fig. 21. The output current Io can be expressed as:

$$Io = \frac{1}{2}\frac{i_{S,PK} \times T_{DIS}}{T_S} = \frac{1}{2}\frac{N_P}{N_S} \times i_{P,PK} \times \frac{T_{DIS}}{Ts} = \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS-OFF}}{R_S} \times \frac{T_{DIS}}{T_S}$$

As a result, the output current Io can be controlled by the Vcs-off and Ts. In the C.C. mode, Vcs-off will be controlled as a constant, 0.85V and the ratio of Tdis/Ts will be modulated as a constant (Tdis/Ts=0.4). In order to let T_{DIS}/T_S=0.4, the switching frequency will be programmed according to T_{DIS}, as shown as flows:

$$f_S = \frac{1}{T_S} = \frac{0.4}{T_{DIS}}$$

The C.C. point and maximum output power can be externally adjusted through external current sense resistor Rs of CS pin. Larger Rs will produce smaller CC point and less output power or otherwise shown in Fig. 22.

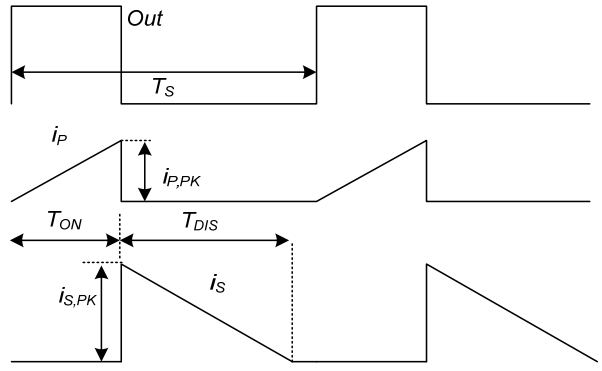


Fig. 21

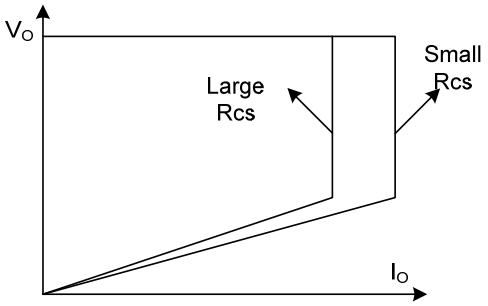


Fig. 22

Current Sensing, load compensation, and Leading-edge Blanking

The typical current mode of PWM controller feeds back with current signal and voltage signal to close the control loop and achieves regulation. The LD7820 detects the primary MOSFET current from the CS pin for the peak current mode control and the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained as below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from current spike. In those low power applications, if the total pulse width of the turn-on spikes is less than LEB time and the negative spike on the CS pin doesn't exceed -0.3V, the R-C filter is free to eliminate. (as shown in the Fig. 23). However, the total pulse width of the turn-on spike is determined by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter for higher power application to avoid the CS pin from being damaged by the negative turn-on spike.

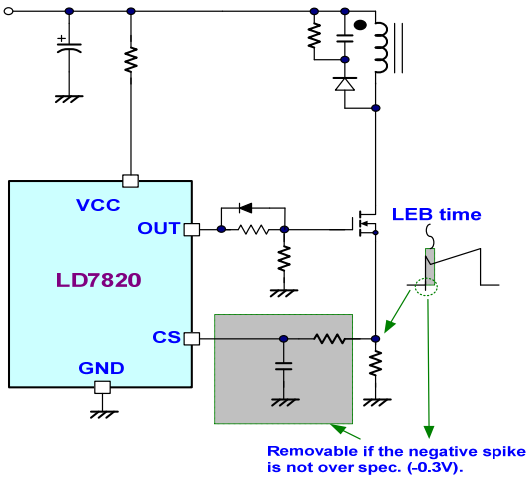


Fig. 23

Oscillator and Switching Frequency (CV Mode)

The switching frequency of LD7820 is various to provide the optimized operations in consideration of heavy load or light load. In heavy load conditions, the switching frequency is fixed at 65 kHz. In light load conditions, the LD7820 operates at a lower frequency to reduce the switching loss. Fig. 15 shows the characteristics of the switching frequency vs. the comp pin voltage (V_{COMP}). In heavy load conditions, the V_{COMP} is higher than V_{SMAX} and the switching frequency

will start to linearly increase from 20 kHz to 65 kHz. In light load conditions, the V_{COMP} is lower than V_{SG2} and the switching frequency will start to linearly decrease from 20 kHz to 1.4kHz. The switching frequency is reduced to a minimum frequency of 1.4kHz, enhancing power saving to meet international power conservation requirements.

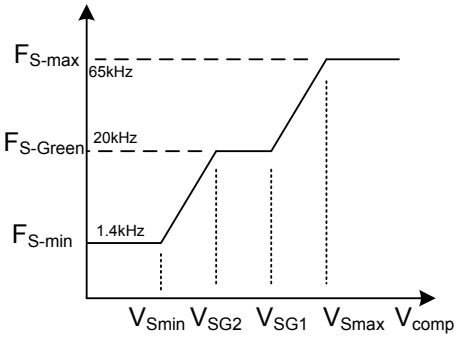


Fig. 24

Frequency Swapping (LD property)

The LD7820 is built-in with frequency swapping function, which enables the power supply designers to optimize EMI performance and system cost. The swapping frequency was internally set between ±6% of switching frequency.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with 300mA of driving capability typically, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7820 is limited to 60% (V_{COMP} > 3.0V) to avoid the transformer saturation.

OVP (Over Voltage Protection) on Vcc

The V_{GS} ratings of the nowadays power MOSFETs are often limited up to max. 30V. To prevent the V_{GS} from fault condition, LD7820 is implemented with OVP function on Vcc.

If the Vcc voltage rises above the OVP voltage threshold, the output gate drive circuit will be shutdown simultaneously and to stop the switching of the power MOSFET until the next UVLO(on). The Vcc OVP function of LD7820 is an auto-recovery type protection. The Fig. 25 shows its operation. As soon as OVP condition is removed, the Vcc level will resume to normal and the output will automatically return to the normal operation.

Over-Temperature Protection (OTP)

An internal OTP circuit is embedded inside the LD7820 to provide the worst-case protection for this controller. When the chip temperature rises higher than the trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window

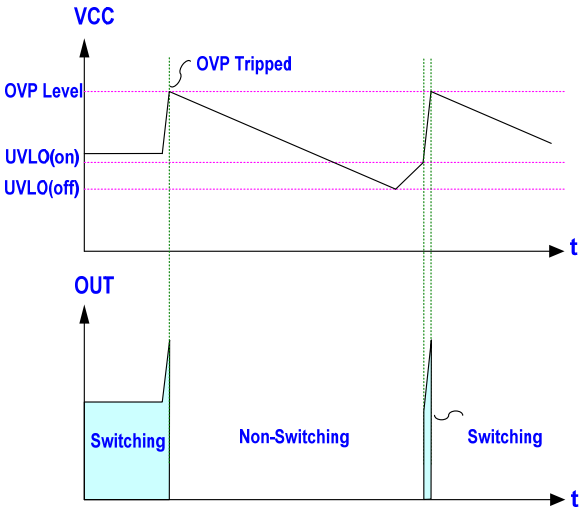
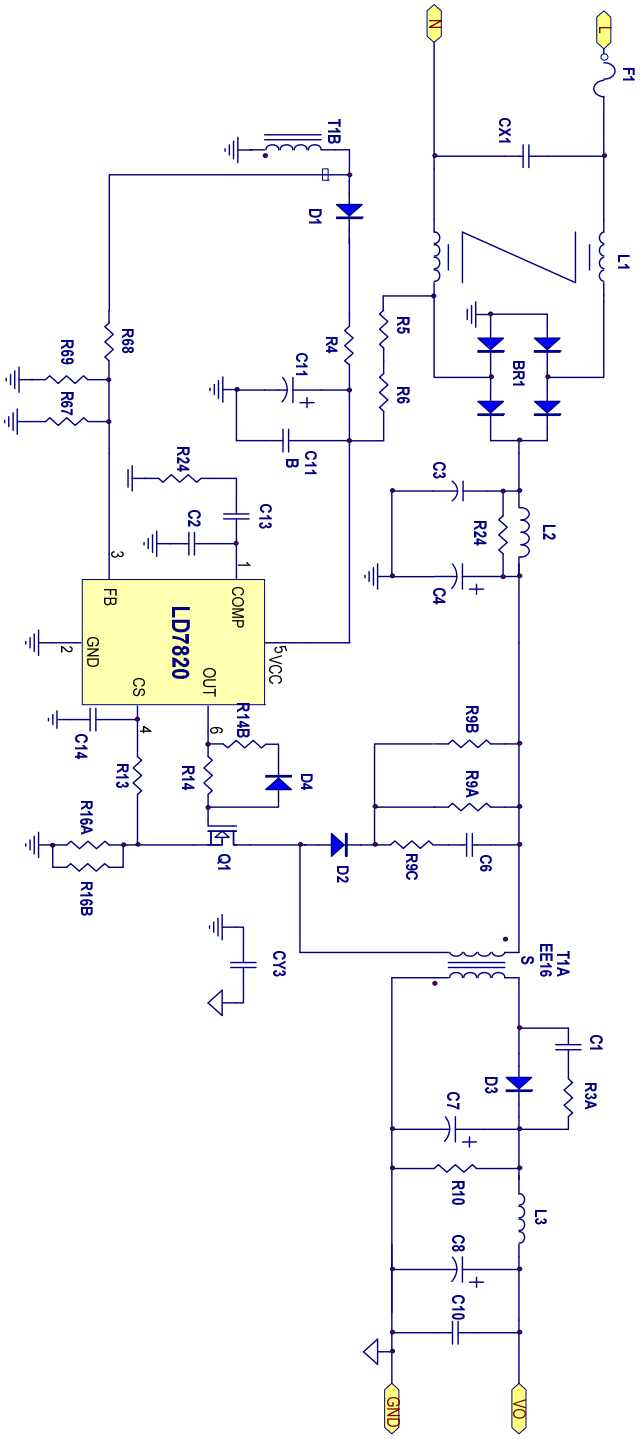


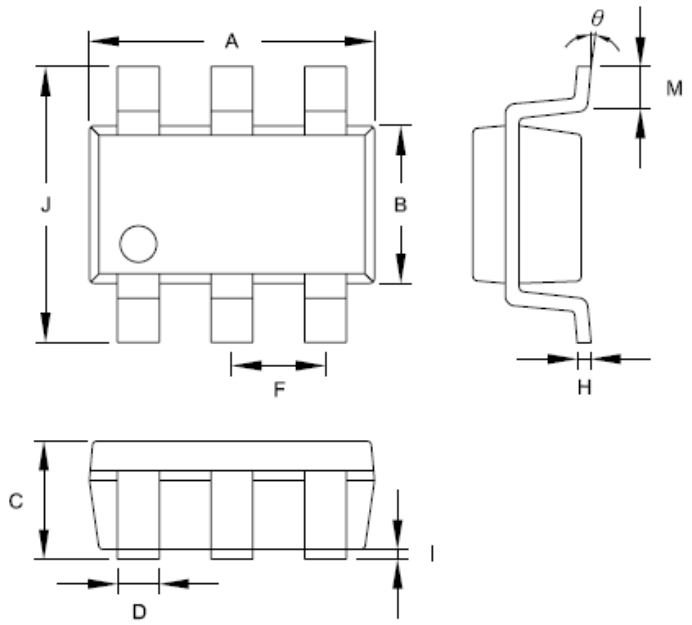
Fig. 25

Reference Application Circuit --- 6W (17.5V/360mA)



Package Information

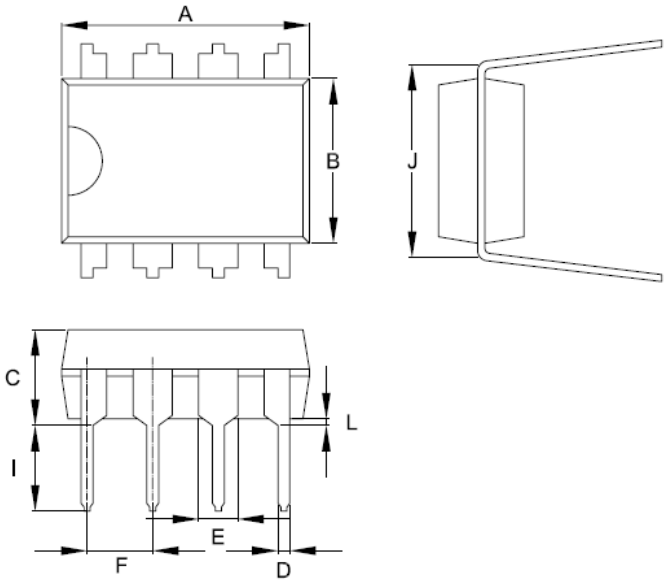
SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP.		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	4/8/2012	Original Specification