High Power Factor Flyback LED Controller with HV Start-up

Rev: 00

General Description

The LD7830H is a HV start-up Flyback PFC controller, specially designed for LED lighting appliances. It operates in transition(TM) mode and integrates with complete protections required for safety and therefore it's an excellent solution to minimize the components counts. Those make it ideal for cost- effective applications.

With HV start-up technology, high power factor and TM control, it's capable to reduce the start-up time and resistor loss greatly. The circuit can easily achieve PF>0.90 to meet most internal standard requirements.

With completed protection built inside this IC, such as over voltage protection (OVP), over current protection (OCP), over load protection (OLP), over temperature protection (OTP), and short circuit protection (SCP), It enable the circuit to meet most safety requirements either in normal and abnormal test.

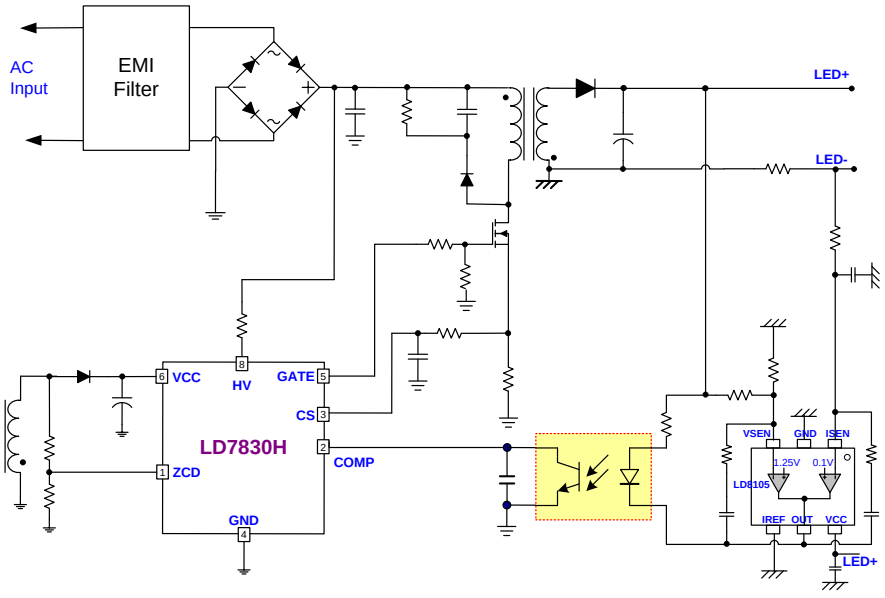
Features

- High voltage (600V) startup circuit
- High Power Factor Flyback PFC controller
- High-Efficiency Transition mode operation
- Wide UVLO (16V_{ON} and 7.5 V_{OFF})
- VCC OVP (Over Voltage Protection)
- OLP(Over Load Protection)
- OCP (Cycle by Cycle Current Limiting) Vcs=0.5V
- Internal OTP (Over Temperature Protection)
- 500/-800mA Driving Capability
- Internal OTP function

Applications

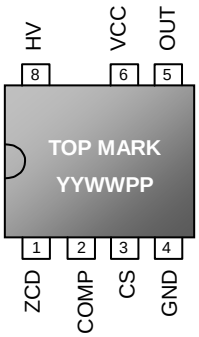
- LED Power Supply
- Flyback PFC Power Supply

Typical Application

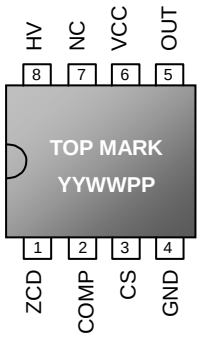


Pin Configuration

SOP-7 (TOP VIEW)



SOP-8 / DIP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package	Top Mark	Shipping
LD7830H GR	SOP-7	LD7830HGR	2500 /tape & reel
LD7830H GS	SOP-8	LD7830HGS	2500 /tape & reel
LD7830H GN	DIP-8	LD7830HGN	3600 /tube /Carton

The LD7830H is RoHs compliant/ Green Packaged.

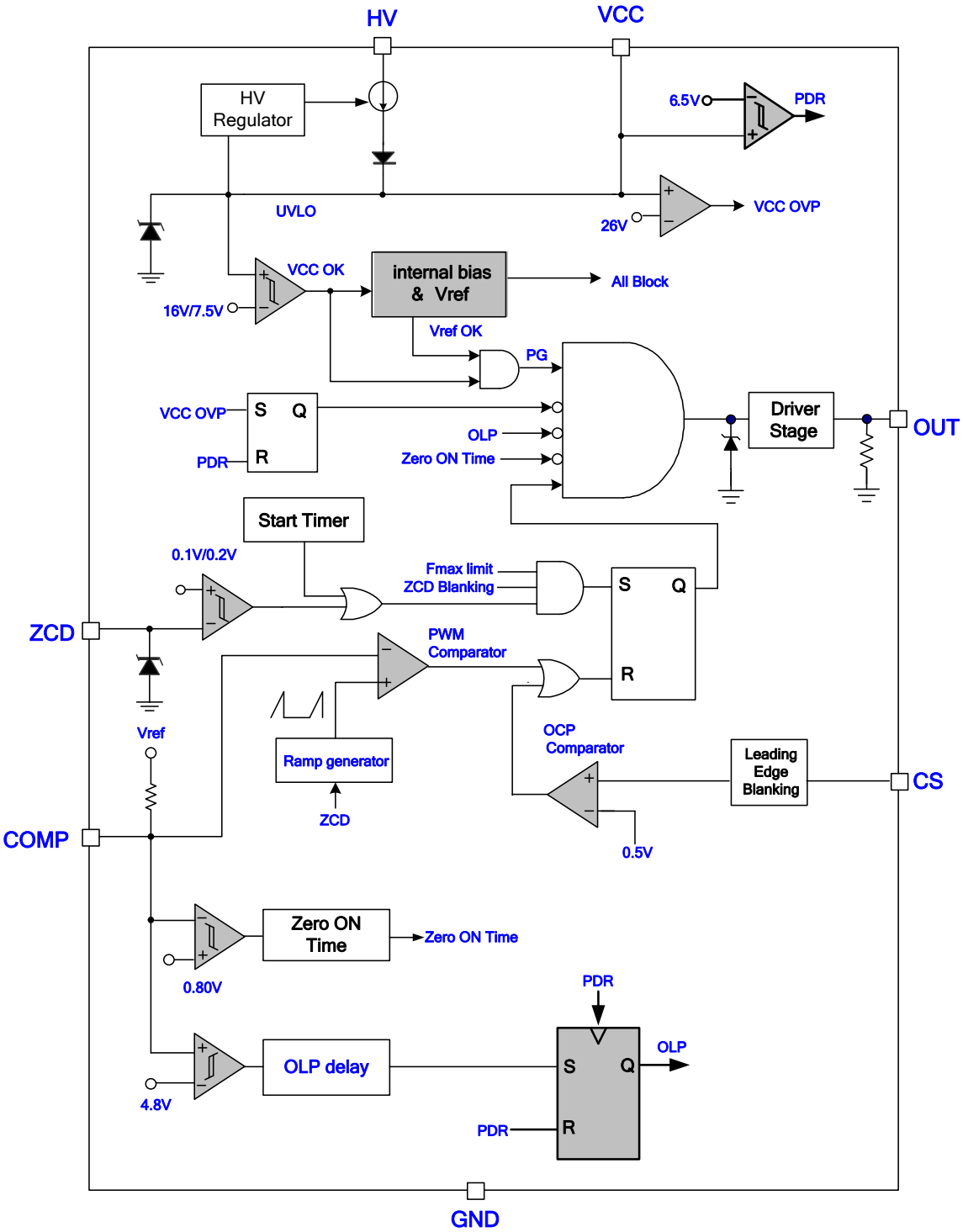
Protection Mode

Part number	VCC OVP	OLP
LD7830H	Latch	Latch

Pin Descriptions

Pin	NAME	FUNCTION
1	ZCD	Quasi resonance detector and programmable maximum ON-time.
	COMP	Feedback pin. Connect with a photo-coupler to close the control loop and achieve regulation.
3	CS	Current sense pin, to sense the MOSFET current for OCP
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Power source VCC pin
7	NC	Not connected.
8	HV	Connect this pin to positive terminal of main bulk cap to provide startup current for controller. Once Vcc is UVLO on , the HV loop will open and turn off internal current source to minimize the power loss.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3 ~30V
High voltage pin, HV	-0.3~600V
OUT	-0.3 ~VCC +0.3V
COMP, CS, ZCD	-0.3 ~6V
Maximum Junction Temperature	150°C
Operating Junction Temperature Range	-40°C to 125°C
Operating Ambient Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8, SOP-7 θ_{JA})	160°C/W
Package Thermal Resistance (DIP-8, θ_{JA})	100°C/W
Power Dissipation (SOP-8, SOP-7, at Ambient Temperature = 85°C)	250mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	400mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV pin)	2.5KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Vcc pin capacitor	4.7	47	μF
Comp pin capacitor	1	10	μF

Electrical Characteristics

(V_{CC}=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High voltage Supply (HV Pin)					
High-voltage current Source	V_{CC}=4V , HV=80V	1.0	1.3	1.6	mA
	V_{CC}=9V,HV=80V	2.6	3.1	3.6	mA
Off-state Leakage current	V_{CC}>$UVLO_{(ON)}$, HV=500V	0		35	μA
Supply Voltage (VCC Pin)					
Startup Current	V_{CC}<UVLO ON	55	75	95	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V, ZCD=0		1		mA
	V_{COMP}=3V, ZCD=0		1.45		mA
	V_{CC} OVP		0.3		mA
	OLP		0.3		mA
UVLO (OFF)		6.9	7.5	8.1	V
UVLO (ON)		15.0	16	17.0	V
HV Self Bias (Linear Regulator)		8.1	8.8	9.5	V
De-Latch VCC Voltage	PDR (Power Down Reset)	6.0	6.5	7.0	V
VCC OVP Level		25	26	27	V
Voltage Feedback(Comp Pin)					
Short circuit current	V_{COMP}=0	0.4	0.5	0.6	mA
Open loop voltage		5.0	5.3	5.8	V
OLP Trip Level		4.65	4.8	4.95	V
Zero ON-time Threshold			0.8		V
Zero ON-time Hysteresis			25		mV
OLP Delay Time		225	270	315	ms
Current Sensing (CS Pin)					
Current Sense Input Threshold Voltage	I_{ZCD}<110μA	0.47	0.5	0.53	V
	I_{ZCD}>490μA	0.322	0.35	0.378	V
Soft Start Time	*		8		ms
Input bias current	V_{CS}=0V~0.5V	0		1.5	μA
LEB time		240	300	360	ns

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Current Detector (ZCD Pin)					
Upper Clamp Voltage	I_{DET}=100μA	5.0	5.6	6.0	V
Lower Clamp Voltage	$I_{DET=}$-2mA	0		-0.35	V
Input Voltage Threshold		0.05	0.1	0.15	V
	Hysteresis	0.05	0.15	0.2	V
Input bias current	V_{ZCD}=1V~4V, OUT=OFF	0.0		1.0	μA
Programming Maximum ON-Time, Ton-max (ZCD Pin)					
Programming Maximum ON-time	ZCD R_{ZCD}=6kΩ,	4.8	5.82	6.8	μs
Maximum ON-time	ZCD R_{ZCD}≥34kΩ,	13.6	16	18.4	μs
Minimum (ON+OFF)-Time					
Minimum (ON+OFF)-Time	F_{MAX}(250kHz),	3.2	4	4.8	μs
Minimum OFF-Time		1.2	1.6	2.0	μs
Gate Drive Output (OUT Pin)					
Output Low Level	V_{CC}=15V, I_{SINK}=20mA	0		0.5	V
Output High Level	V_{CC}=15V, I_{SOURCE}=20mA	10		VCC	V
Output High Clamp Level	V_{CC}=16V		13		V
Rising Time	V_{CC} =15V, CL=1000pF		75	150	ns
Falling Time	V_{CC} =15V, CL=1000pF		25	50	ns
Starter					
Start Timer Period		100	150	200	μs
Internal OTP (Over Temp. Protection)					
OTP Trip level	*		140		°C
OTP Hysteresis	*		30		°C

*: These parameters are guaranteed by design.

Application Information

Operation Overview

The LD7830H is an excellent single-stage Flyback PFC controller for LED lighting applications. With several functions integrated, it's an ideal solution to minimize external components counts and the size.

In addition, the LD7830H is a voltage-mode TM PFC controller. The turn-on time of switch is fixed while the turn-off time is varied in the steady condition. Therefore, the switching frequency changes in accordance with the input voltage variation. The LD7830H provides functions of over-load protection, over-voltage protection, over-current protection, under-voltage lockout and integrated LEB of the current sensing. Also, the LD7830H requires no main-voltage sensing, superior to what the other traditional current mode PFC controllers behave for power saving.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides startup current through a startup resistor to power on the PWM controller. However, it consumes significant power for it. In most cases, startup resistors carry large resistance. And, larger resistance spends more startup time.

To achieve the optimized topology, as shown in figure 13, LD7830H is implemented with a high-voltage startup circuit for such requirement. During startup, a high-voltage current source sinks from the full-bridge rectifier to provide startup current to charge Vcc capacitor C1. On condition of VCC below PDR, it consumes only 1.3mA for charge current. This protects the IC from damage in case the VCC pin is shorted to ground. In short start-up time, the charge current will increases to 3.1mA once VCC rises above PDR voltage threshold during start up. Meanwhile, it consumes only 75μA for Vcc supply current, so most of the HV current is reserved to charge the Vcc capacitor. In using such configuration, the turn-on delay time will be almost no difference either in low-line or high-line conditions.

Once the Vcc voltage rises over UVLO(on), it will power on the LD7830H and further to deliver the gate drive signal. Then the high-voltage current source will be disabled and the supply current is provided from the auxiliary winding of the transformer. Therefore, the power loss is eliminated and power saving is enhanced.

An UVLO comparator is embedded to detect the voltage on Vcc pin to ensure the supply voltage enough to power on the LD7830H PWM controller and in addition to drive the power MOSFET. As shown in Fig. 14, a hysteresis is provided to prevent the shutdown from voltage dip during startup.

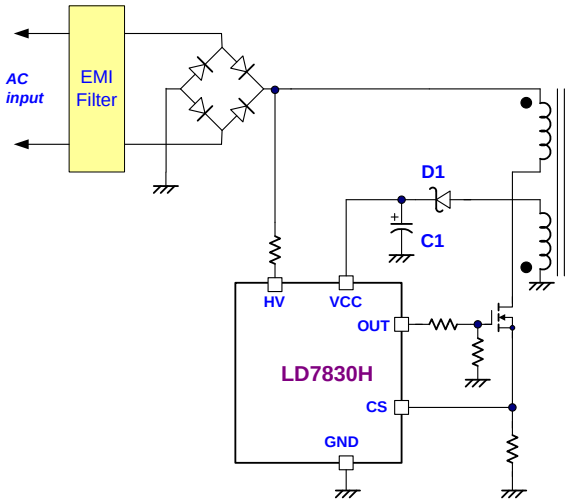


Fig. 13

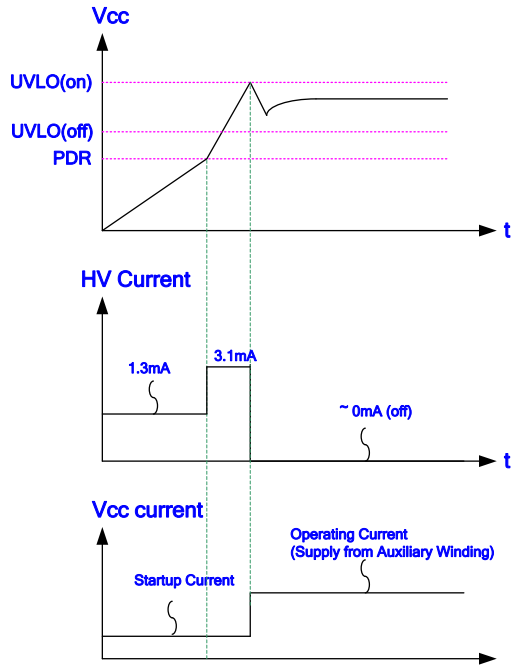


Fig. 14

Ramp Generator Block and Zero Current Detection (ZCD)

Fig. 15 shows typical ramp generator block and ZCD block. The COMP pin voltage and the output of the ramp generator block are compared to determine the MOSFET ON-time, as shown in Fig. 16.

A greater COMP voltage produces more ON-time. Using an external resistor to connect with ZCD pin to set the desired slope of the internal ramp, the user may program the maximum ON-time. Alternatively, the ON-time will also achieve its maximum when COMP pin voltage trip OLP trigger point.

The maximum ON-time should be set according to the condition of the transformer, lowest AC line voltage, and maximum output power. A choice of optimum resistor value would result in best performance.

It shuts down the drive output if COMP pin voltage falls below zero ON-time threshold. This optimizes the efficiency for power saving in most conditions.

The Zero Current Detection block will detect auxiliary winding signal to drive MOSFET as ZCD pin voltage drops to 0.1V. As ZCD pin voltage drops to 0.1V, the current through the transformer is below zero. This feature enables transition-mode operation. The ZCD comparator would not operate if ZCD pin voltage remains at above 0.2V. Once it drops below 0.1V, the zero current detector will act to turn on the MOSFET.

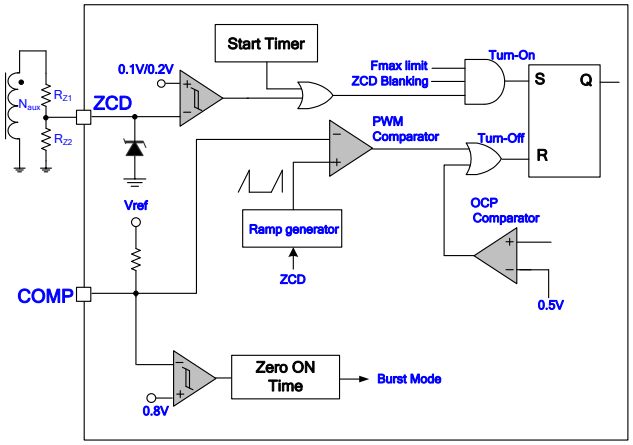


Fig. 15

The 150μs timer generates a MOSFET turn-on signal if the driver output drops to low level for more than 150μs from the falling edge of the driver output. Fig. 16 shows typical ZCD-related waveforms. Since ZCD pin carries some capacitance, it produces some delay to the turn-on time caused from Rz1. During delay time, the junction capacitor of the MOSFET resonates with the primary inductor of the transformer and the drain-source voltage (V_{DS}) decreases accordingly. So, the MOSFET consumes less voltage to turn on and it therefore minimizes the power dissipation.

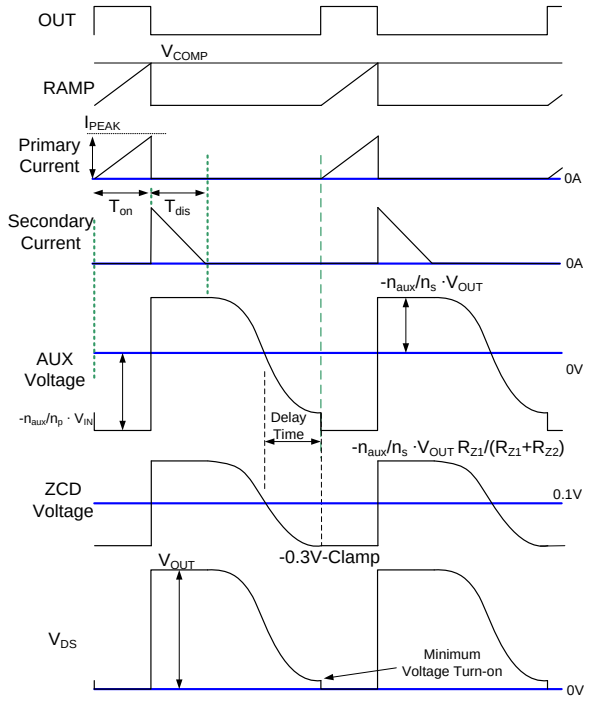
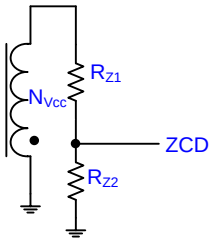


Fig. 16

Programming Maximum ON-time

LD7830H features adjustable maximum ON-time to limit power output in abnormal operation. The selection of maximum ON-time is subject to ZCD resistance as shown in Fig. 17. ZCD resistance can be obtained from below.



$$R_{ZCD} = \frac{R_{Z1} \cdot R_{Z2}}{R_{Z1} + R_{Z2}}$$

Fig. 17

The following table is a suggestion for maximum ON-time setting.

R_{ZCD}	Max. Ton (Typ.)	Suggestion
32k<R_{ZCD}	16μs	36k
28k<R_{ZCD}<32k	12.8μs	30k
24k<R_{ZCD}<28k	10.7μs	26k
20k<R_{ZCD}<24k	9.1μs	22k
16k<R_{ZCD}<20k	8.0μs	18k
12k<R_{ZCD}<16k	7.1μs	14k
8k<R_{ZCD}<12k	6.4μs	10k
R_{ZCD}<8k	5.8μs	6k

High/ Low Line OCP Compensation

LD7830H supports high/low line OCP compensation through aux-winding to reflect the magnitude of input voltage. When gate turns on, ZCD pin will source the current I_{ZCD} to clamp the voltage to zero as shown in Fig.18. According to this current information, OCP trigger level V_{CS-OFF} will be determined by R_{Z1} and input voltage. In order to avoid ZCD pin over rating, I_{ZCD} must be set less than 2mA. $I_{ZCD-max}$ can be calculated as below:

$$I_{ZCD-MAX} = \frac{V_{IN-PK}}{N_P / N_{VCC} \cdot R_{Z1}} < 2mA$$

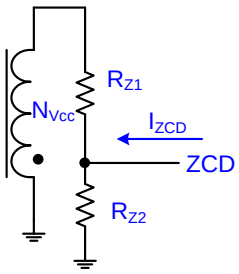


Fig. 18

The relation (typical) of V_{CS-OFF} and I_{ZCD} is shown in Table 1.

I_{ZCD} (μA)	V_{CS-OFF} (V)
<160	0.5
160~200	0.475
200~240	0.4625
240~290	0.45
290~350	0.425
350~390	0.4
390~450	0.375
>450	0.35

Table 1

Output Drive Stage

With typical 500mA/-800mA driving capability, an output stage of a CMOS buffer is incorporated to drive a power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage is larger than 13V.

Current Sensing and Leading-edge Blanking

The LD7830H detects the primary MOSFET current over CS pin for pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.5V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK\,(MAX)} = \frac{0.5V}{R_S}$$

A leading-edge blanking (LEB) time is imbedded in the input of CS pin to prevent false-triggering from the current spike. In those low power applications, if the total pulse width of the turn-on spikes is less than LEB and the negative spike on the CS pin isn't over -0.3V, it is free to eliminate the R-C filter.

However, the total pulse width of the turn-on spike is determined by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter for those large power applications to avoid CS pin being damaged from negative turn-on spike.

Over Load Protection (OLP) - Latch mode

The LD7830H features latch mode of smart OLP protection. Figure 19 shows the waveform under fault condition. The feedback system will force the voltage loop enter toward the saturation and thus pull the voltage high on COMP pin (VCOMP). When the VCOMP ramps up to the OLP threshold and stays there for more than OLP delay time, it will activate the protection to latch off the gate output and stop switching of the power circuit. The delay time is to prevent the false-triggering during power-on, turn-off transient or in peak load condition. Unless the over load condition is removed, the controller will remain latched until the Vcc drops below PDR. It is necessary to start another AC power-on recycling to resume the output.

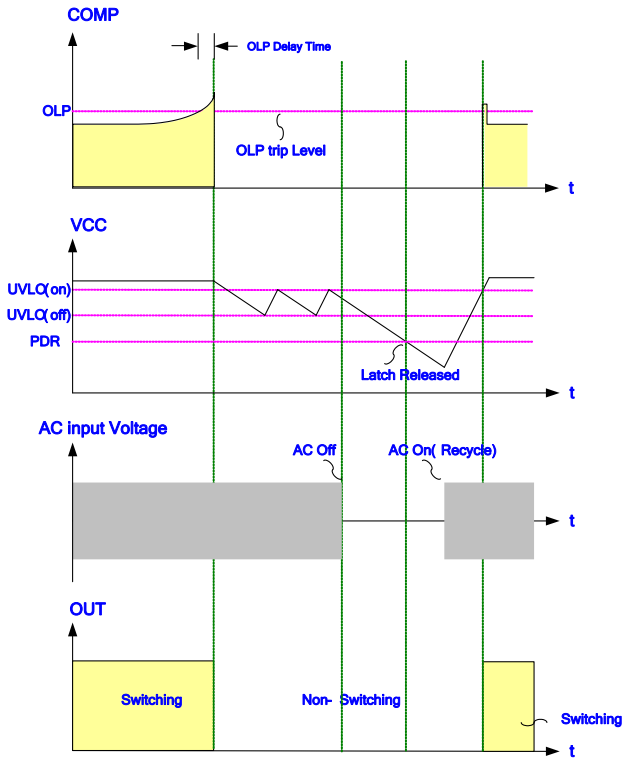


Fig. 19

OVP (Over Voltage Protection) on Vcc-Latched Mode Protection

The V_{GS} ratings of the nowadays power MOSFETs is mostly for 29V maximum. To protect the V_{GS} from fault conditions, LD7830H is implemented with OVP function on Vcc. If Vcc voltage is over the OVP threshold, the output gate drive circuit will be shut down simultaneously to stop switching of the power MOSFET.

The Vcc OVP function in LD7830H is a latch-off type protection. If the OVP condition occurs (usually caused by the feedback loop opened), Vcc will not recover until AC power turns off. Figure 20 shows its operation. The Vcc drops since there's no AC power present. The de-latch level of OVP is defined by internal PDR. Over voltage protection could be activated after Vcc is below PDR level.

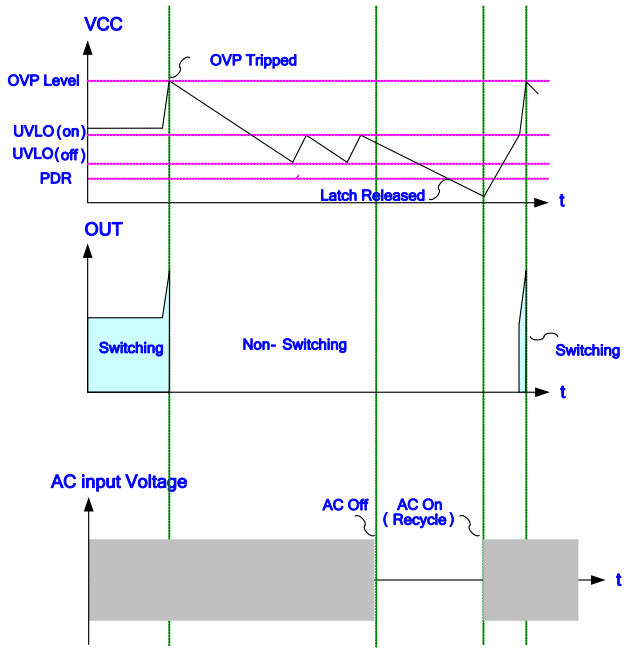


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Fig. 20

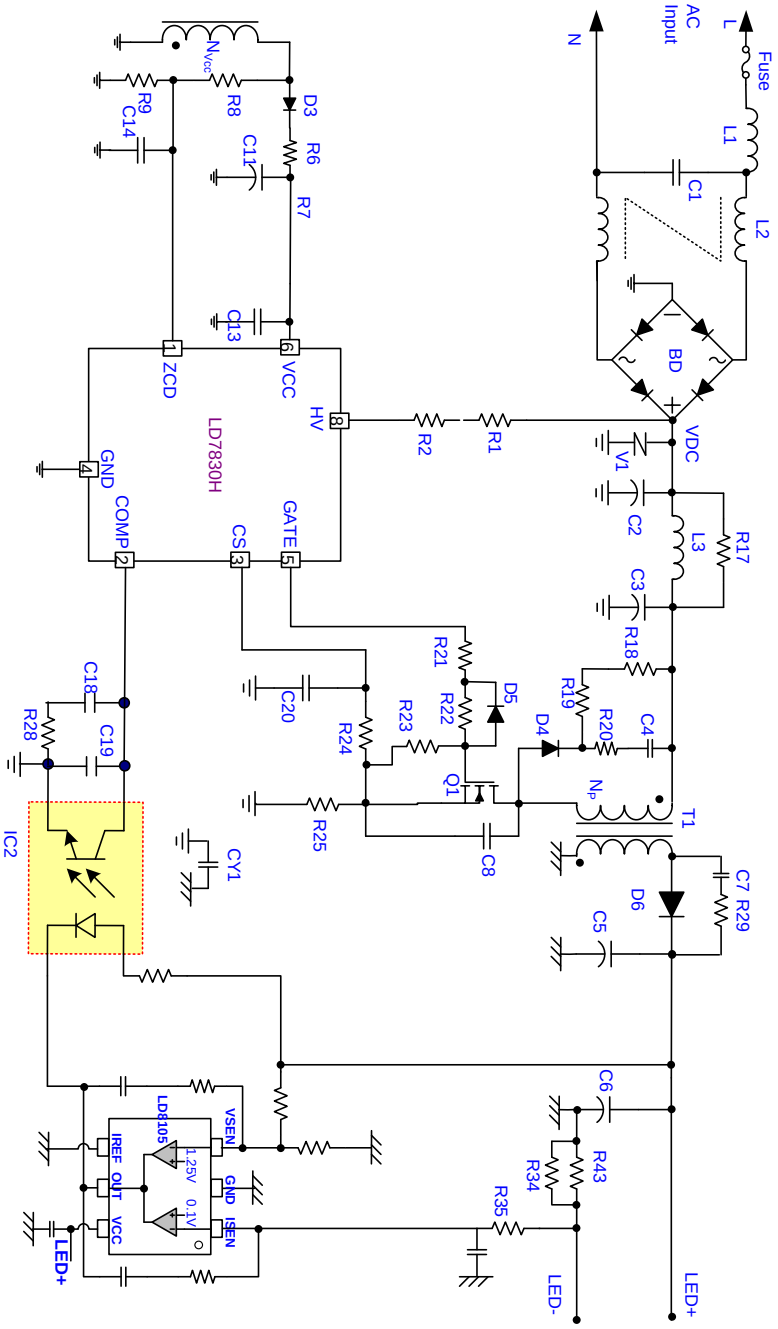
Fault Protection

There are several critical protections were integrated in the LD7830H to prevent the power supply or adapter from being damaged. Those damages usually come from open or short condition caused to LD7830H.

Once it happens in below conditions, the gate output will turn off immediately to protect the power circuit.

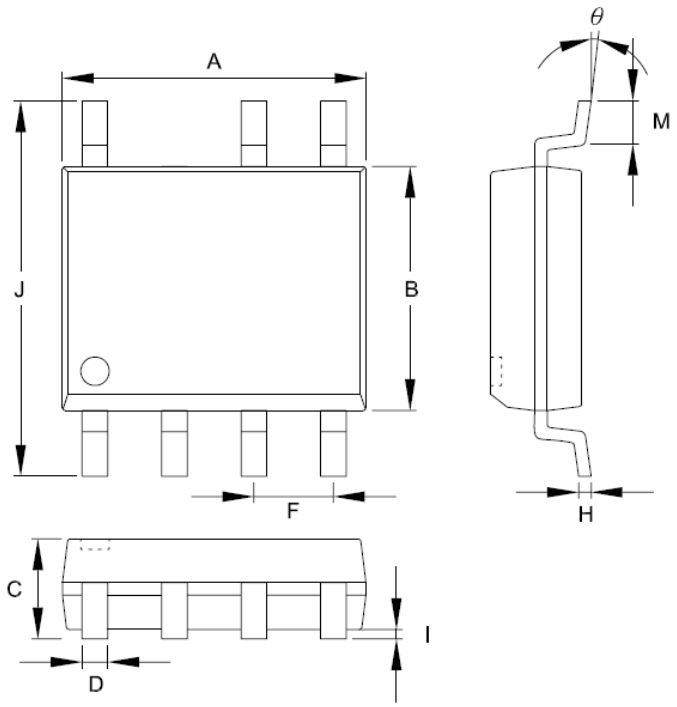
1. Comp pin floating
2. CS pin floating

Reference Application Circuit --- LED -24V/700mA (90~264V_{AC})



Package Information

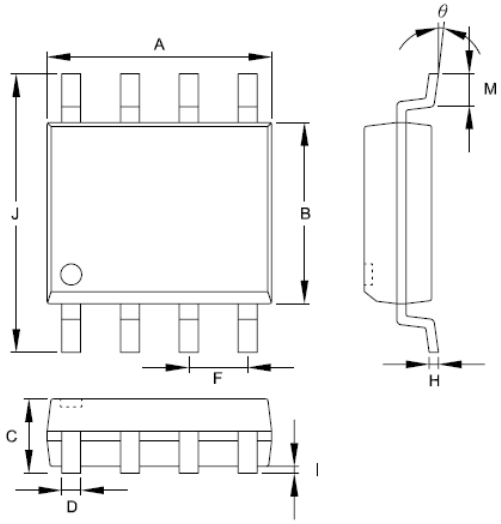
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

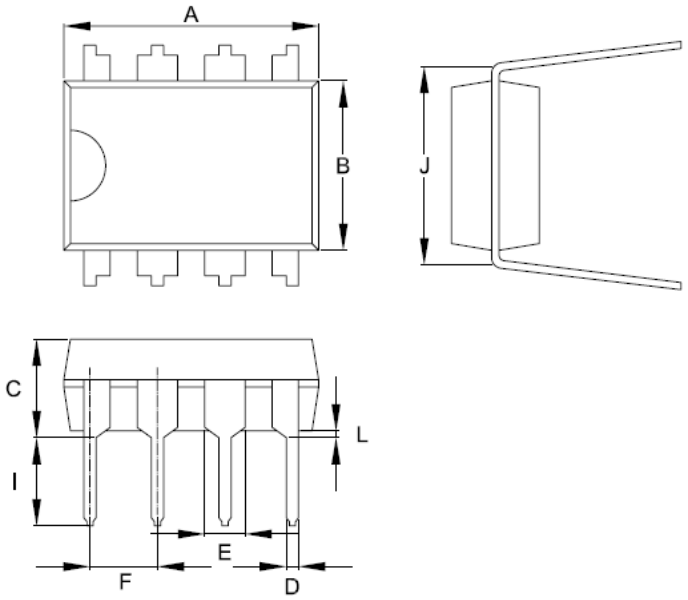
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	6/27/2012	Original Specification