High Power Factor Primary Side Flyback LED Controller With HV Start-up

REV: 00

General Description

The LD7831 is a high power factor primary side Flyback LED controller with HV start-up, specially designed for LED lighting. The LD7831 provides constant current (CC) operation requiring neither photo-coupler nor secondary control circuit. It minimizes the components counts in a SOP-7. Those make it easy to design for cost- effective applications.

With HV start-up technology, high power factor and TM control, the start-up time and resistor loss could be minimized efficiently. The circuit can easily achieve PF>0.90 to meet most of the international standard requirements.

With completed protection built in this IC, such as over voltage protection (OVP), over current protection (OCP) and short circuit protection (SCP), the device is capable to meet the safety requirements.

Features

- High Voltage (700V) Startup Circuit
- High Power Factor Flyback Primary Side PFC Controller
- High Efficiency Transition Mode Operation
- 28V VCC OVP (VCC Over Voltage Protection)
- OCP (Cycle by Cycle Current Limiting)
- SCP (Output Short Protection)
- OTP (Over Temperature Protection)
- CS Short Protection
- Adjustable Output OVP
- 250/-500mA Driving Capability
- Internal OTP Function

Applications

- LED Power Supply
- LED Light Bulb/Tube

Typical Application

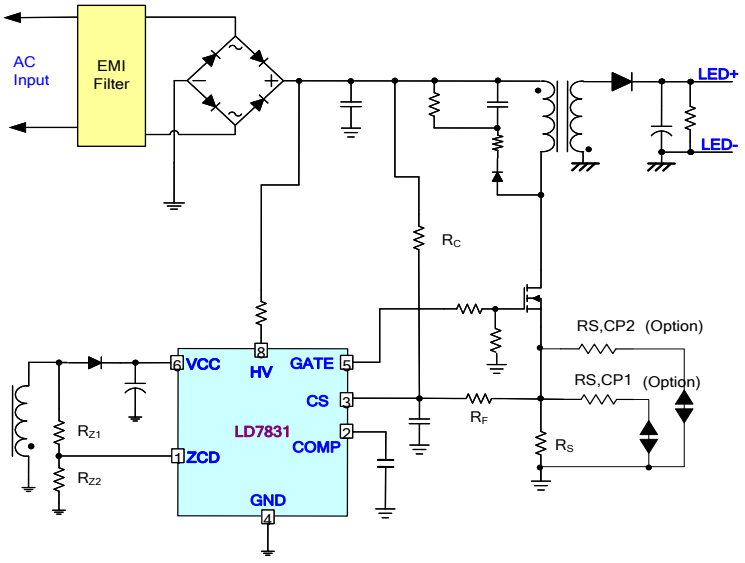
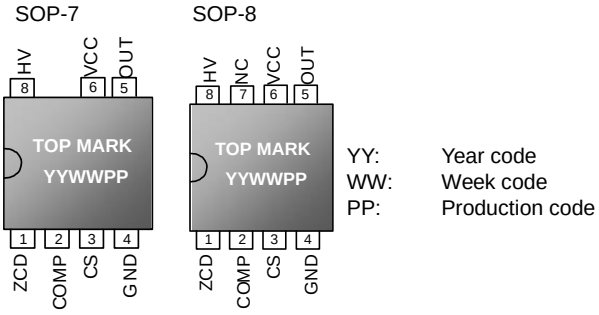


Fig. 1 Application circuit

Pin Configuration



Ordering Information

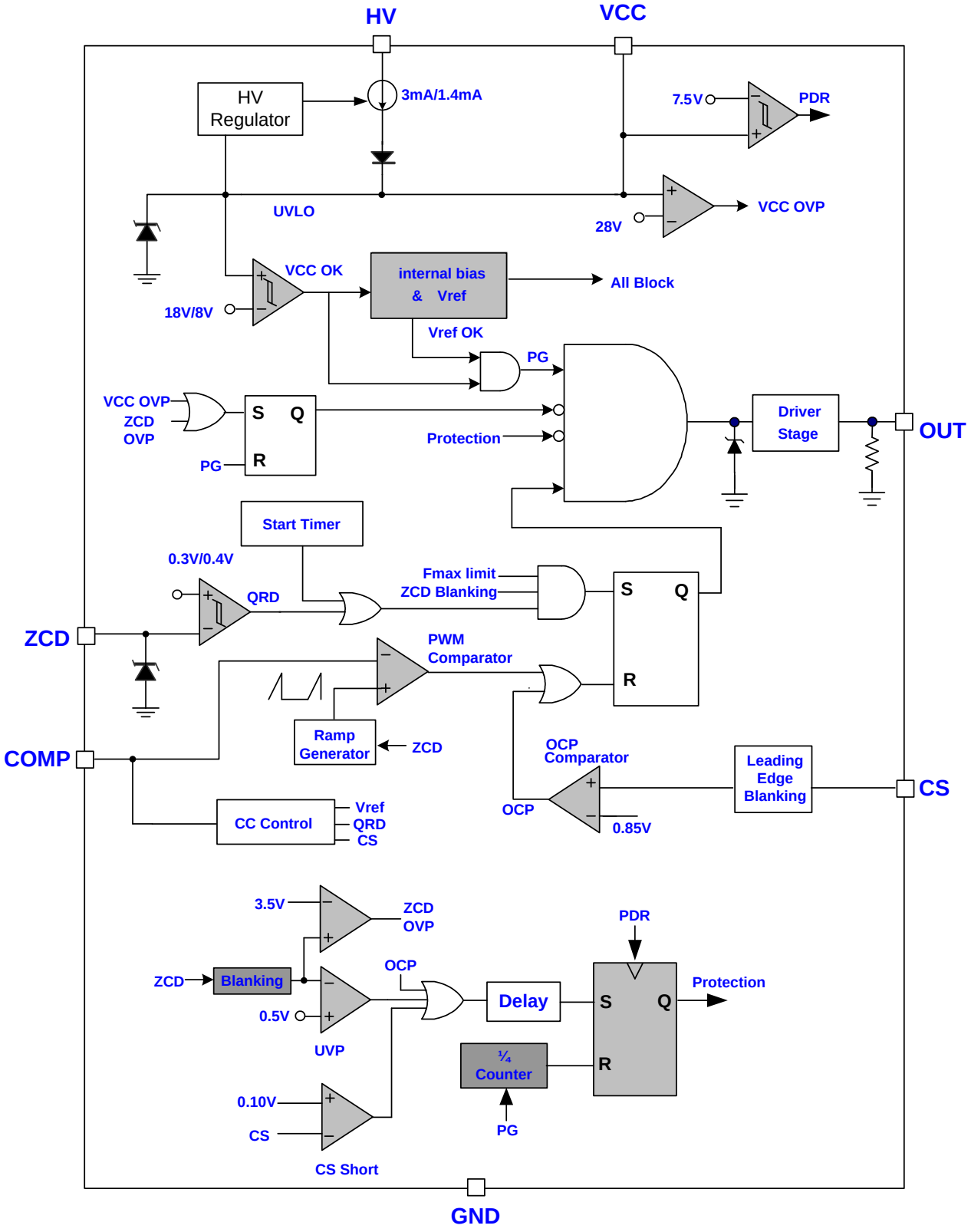
Part number	Package	Top Mark	Shipping
LD7831 GR	SOP-7	LD7831 GR	2500 /tape & reel
LD7831 GS	SOP-8	LD7831 GS	2500 /tape & reel

The LD7831 is ROHS compliant/ green packaged.

Pin Descriptions

Pin	NAME	FUNCTION
1	ZCD	Quasi resonance detector, which supports programmable maximum on-time. This pin receives the auxiliary winding voltage through a resister divider and detects the quasi resonance. It also provides protection for over-voltage output.
2	COMP	Loop compensation pin. Connect a capacitor with it to stabilize the control loop.
3	CS	Current sense pin, connect it to sense the MOSFET current for OCP
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Power source VCC pin
7	NC	Not connected.
8	HV	Connect this pin to the positive of main bulk cap to provide the startup current for controller.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3 ~30V
High voltage pin, HV	-0.3 ~700V
OUT	-0.3 ~30V
COMP, ZCD	-0.3 ~6V
CS,	-0.3 ~6V
ZCD Pin Clamping Current	-1.5m~100μA
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-7/SOP-8, θ_{JA})	160°C/W
Power Dissipation (SOP-7/SOP-8, Tj=125°C, Ta=85°C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV pin)	2.5KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-20	125	°C
Supply VCC Voltage	10	26	V
Vcc pin capacitor	4.7	22	μF
Comp pin capacitor	0.33	1	μF
CS pin capacitor	47	470	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(V_{CC}=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYM	MIN	TYP	MAX	UNITS
High voltage Supply(HV Pin)						
High-voltage current Source	V_{CC}=0V , HV=80V	I_{HV_LO}	1	1.4	1.8	mA
	V_{CC}=15V,HV=80V	I_{HV_HI}	2.2	3	3.8	mA
Off-state Leakage current	V_{CC}>UVLO(ON), HV=500V	I_{HV_OFF}	0		30	μA
Supply Voltage (VCC Pin)						
Startup Current	V_{CC}<UVLO ON	I_{ST}	-	160	250	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V, ZCD=0	I_{OP_LO}	-	0.8	1	mA
	V_{COMP}=3V, ZCD=0	I_{OP_HI}	-	1.3	1.6	mA
	V_{CC} OVP, UVP, CS short	I_{OP_OVP}	0.3	0.5	-	mA
UVLO (off)		V_{UV_OFF}	7	8	9	V
UVLO (on)		V_{UV_ON}	16	18	20	V
HV Self Bias (Linear Regulator)		V_{LDO}	8.5	9.5	10.5	V
De-Latch Voltage	PDR	V_{PDR}	7	7.5	8	V
VCC OVP Level		V_{CC_OVP}	26.5	28	29.5	V
CC Integrator (Comp Pin)						
Comp open		V_{CMP}	4.3	4.6	4.9	V
Zero On Time mode		V_{ZOT}	0.2	0.3	0.4	V
Reference Voltage	At CP condition	V_{REF}	3.94	4	4.06	V
Current Sensing (CS Pin)						
CS OCP Voltage		V_{OCP}	0.80	0.85	0.9	V
Soft Start Time	*	T_{SS}	-	10	-	ms
CS Short Protection		V_{CSSP}	0.05	0.1	0.15	V
CS Short Protection De-bounce Time	*	T_{CSSP}	-	40	-	ms
LEB time		T_{LEB}	150	300	450	ns

PARAMETER	CONDITIONS	SYM	MIN	TYP	MAX	UNITS
Zero Current Detector (ZCD Pin)						
Upper Clamp Voltage	I_{DET}=100μA	V_{ZH}	5	5.6	6.2	V
Lower Clamp Voltage	$I_{DET=}$-1.5mA	V_{ZL}	0	-	-0.3	V
Input Voltage Threshold		V_{ZCD}	0.15	0.3	0.45	V
	Hysteresis	H_{ZCD}	-	0.1	-	V
ZCD Blanking Time	*	T_{BNK_ZCD}	-	1.5	-	μs
UVP Detect Level		V_{UVP}	0.4	0.5	0.6	V
UVP De-bounce Time		T_{UVP}	-	40	-	ms
ZCD OVP		V_{ZOVP}	3.3	3.5	3.7	V
Programming Maximum ON-Time, Ton-max (ZCD Pin)						
Programming Maximum On Time	ZCD RT=80k (V_{CMP} open)	T_{ON_MAX}	-	26	-	μs
Programming Maximum On Time	ZCD RT=36kΩ,	T_{ON_MAX1}	-	15	-	μs
	ZCD RT=6kΩ,	T_{ON_MAX2}	-	3.3	-	μs
Minimum (ON+OFF)-Time						
Minimum ON+OFF-Time,	$F_{S,MAX}$(300kHz),	T_{S_MAX}	2.7	3.33	3.9	μs
Gate Drive Output (OUT Pin)						
Output Low Level	V_{CC}=15V, I_{SINK}=20mA	V_{G_LO}	0	-	0.5	V
Output High Level	V_{CC}=15V, I_{SOURCE}=20mA	V_{G_HI}	10	-	VCC	V
Output High Clamp Level	V_{CC}=20V	V_{G_CLAMP}	12	13	14	V
Rising Time	V_{CC} =15V, CL=1000pF*	T_{G_RISE}	-	90	-	ns
Falling Time	V_{CC} =15V, CL=1000pF*	T_{G_FALL}	-	50	-	ns
Timer						
Timer	After Soft Start	T_{IMER}	110	140	170	μs
Internal OTP (Over Temp. Protection)						
OTP Junction Trip level	*	OTP	-	140	-	°C
OTP Hysteresis	*	H_{OTP}	-	30	-	°C

*: Guaranteed by design.

Typical Performance Characteristics

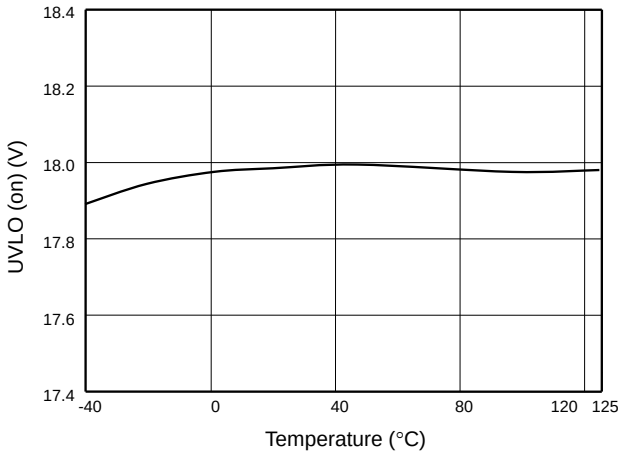


Fig. 2 UVLO (on) vs. Temperature

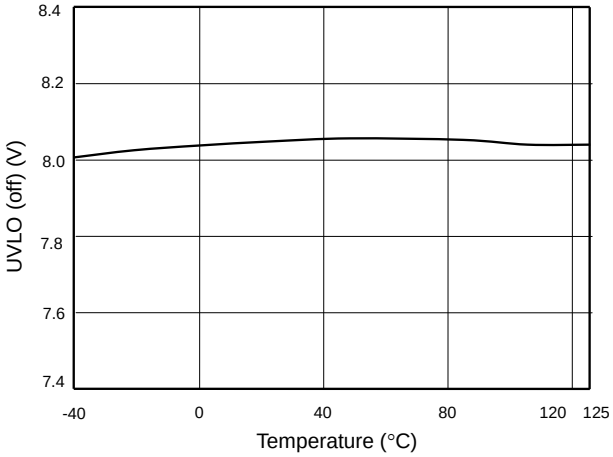


Fig. 3 UVLO (off) vs. Temperature

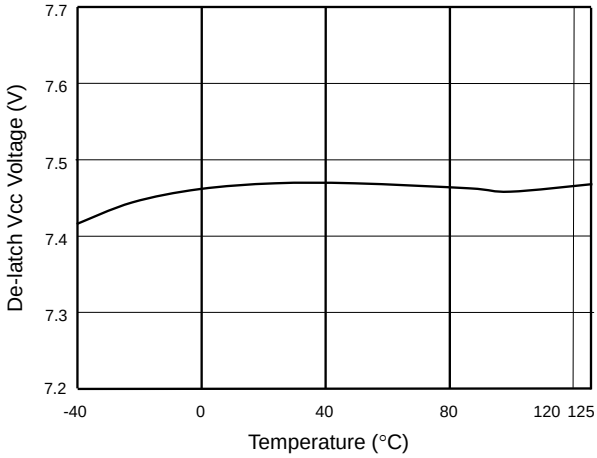


Fig. 4 De-latch Vcc Voltage vs. Temperature

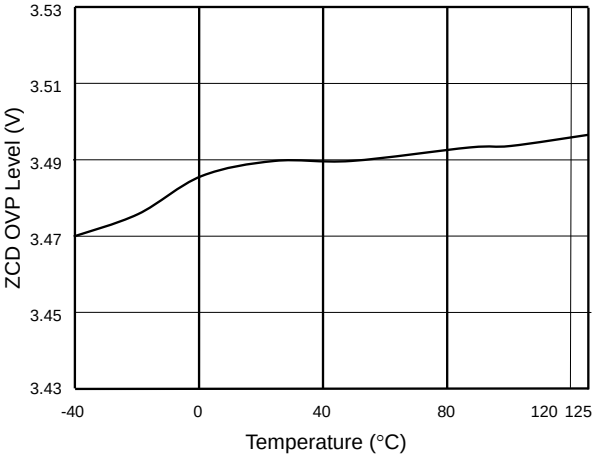


Fig. 5 ZCD OVP Level vs. Temperature

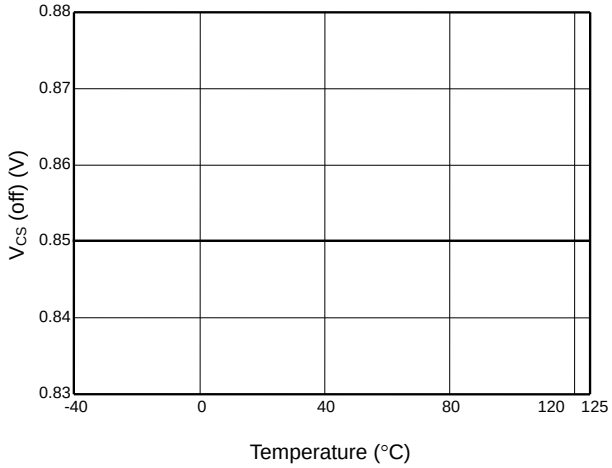


Fig. 6 V_{CS} (off) vs. Temperature

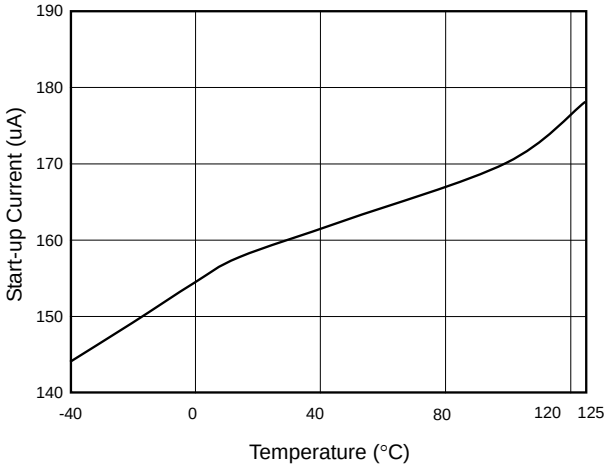


Fig. 7 Start-up Current vs. Temperature

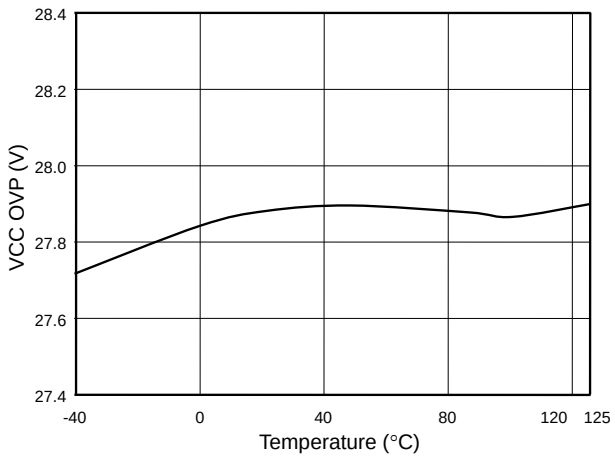


Fig. 8 VCC OVP vs. Temperature

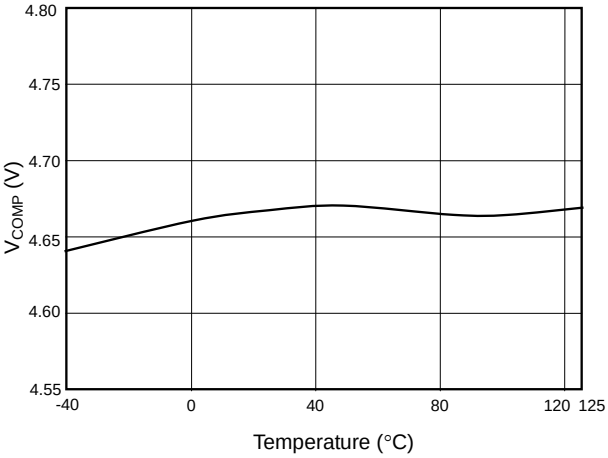


Fig. 9 V_{COMP} open loop voltage vs. Temperature

Application Information

Operation Overview

The LD7831 is a single-stage Flyback PFC controller for LED lighting applications. It provides constant current (CC) operation and requires neither photo-coupler nor secondary control circuit. It integrates more functions to reduce the external components counts and the size. Its major features are described as below.

The LD7831 can operate in voltage-mode. The turn-on time of the switch is fixed while the turn-off time is various in steady states. Therefore, the switching frequency changes in accordance with the input voltage variation. The LD7831 features output over-voltage protection, output short circuit protection, under voltage lockout and LEB of the current sensing.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The popular way to power up the PWM controller is to provide startup current through a startup resistor to power up the PWM controller. However, it consumes significant power to meet the power saving requirement. In most cases, startup resistors carry large resistance. And, a larger resistor will spend more time to start up.

To achieve optimized topology, as shown in Fig. 10 and Fig. 11, LD7831 is implemented with a high-voltage startup circuit to enhance it. During startup, a high-voltage current source sinks current from the full-bridge rectifier to provide the startup current and charge VCC capacitor C1 at the same time. On condition of VCC below PDR, the charge current will remain at 1.4mA to protect the circuit from being damaged, even in case VCC pin is shorted to ground. In contrast, the charge current will increase to 3mA once VCC rises above PDR voltage threshold during start up. Meanwhile, the VCC supply current kept at low level of 160μA that most of the HV current is reserved to charge the Vcc capacitor. By using such configuration, the turn-on delay time will be almost same no matter under low-line or high-line conditions.

The LD7831 will be soon turned on as the VCC's voltage rises over UVLO(ON). It will also drive the high voltage start-up circuit to operate as a regulator and maintain the VCC voltage at UVLO(ON) level. The current consumed is 3mA max. After 50ms of UVLO(ON), the high voltage regulator will be set at 9.5V to reduce the power loss. Well, in order to supply sufficient VCC voltage in normal condition, it required auxiliary voltage source to operate. The high voltage regulator will protect the controller from shut off at load transient when VCC voltage drops below UVLO-off. HV regulator will soon be disabled as the IC enter protection mode, as SCP, OVP, OTP, CS short protection…etc.

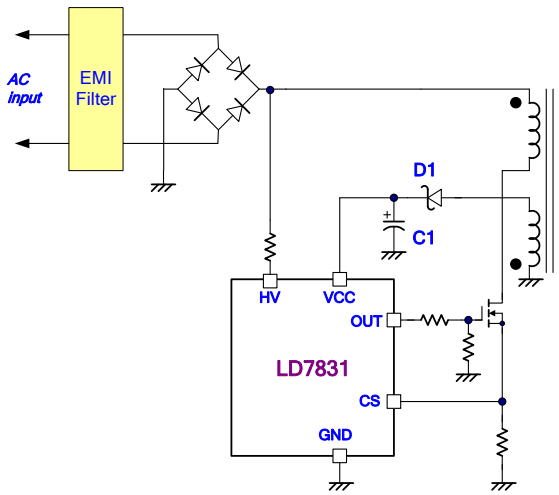


Fig. 10

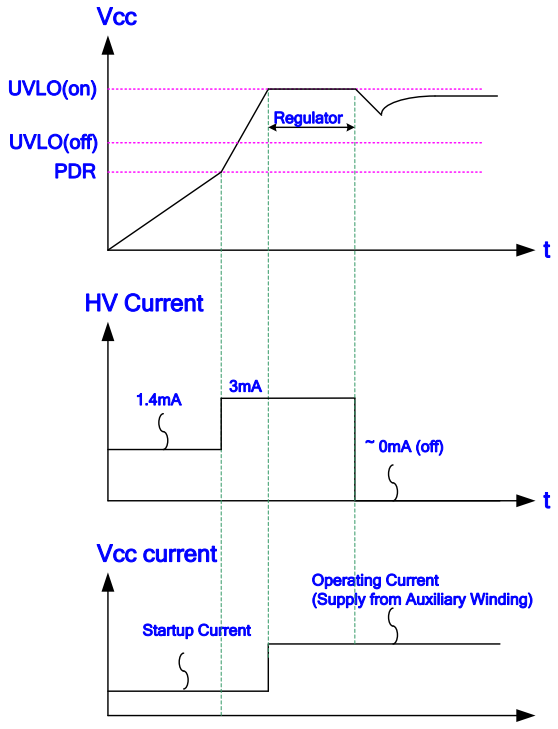


Fig. 11

Ramp Generator Block and Zero Current Detection (ZCD)

Fig. 12 shows typical ramp generator block and ZCD block. The COMP pin voltage and the output of the ramp generator block are compared to determine the MOSFET ON-time, as shown in Fig. 13.

A greater COMP voltage produces more ON-time. Using an external resistor connected to ZCD pin to set the desired slope of the internal ramp, the user may program the maximum ON-time.

The setting for maximum ON-time will be achieved according to the transformer, lowest AC line voltage, and maximum output power. A choice of optimum resistor value would result in best performance.

It will shut down the driving output if COMP pin voltage falls below the threshold of zero ON-time. This optimizes the efficiency in power saving in most conditions.

The Zero Current Detection block will detect auxiliary winding signal to drive MOSFET as ZCD pin voltage drops to 0.3V. As ZCD pin voltage drops to 0.3V, the current through the transformer is below zero. This feature enables transition-mode operation. The ZCD comparator would not operate if ZCD pin voltage remains above 0.4V. Once it drops below 0.3V, the zero current detector will activate to turn on the MOSFET.

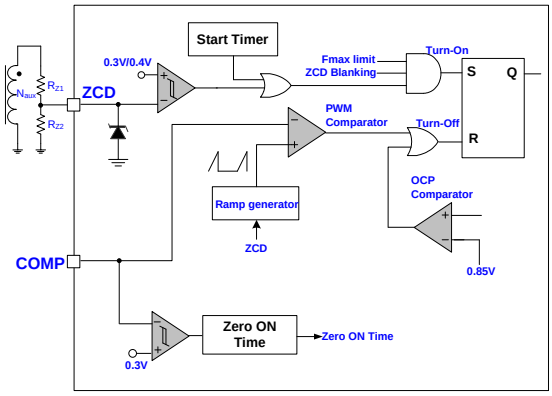


Fig. 12

The 140μs timer generates a MOSFET turn-on signal if the driver output drops to low level for more than 140μs from the falling edge of the driver output. Fig. 13 shows typical ZCD-related waveforms. Since ZCD pin carries some capacitance, it produces some delay to the turn-on time caused from Rz1. During delay time, the junction capacitor of the MOSFET resonates with the primary inductor of the transformer and the drain-source voltage (V_{DS}) decreases accordingly. So, the MOSFET consumes less voltage to turn on and it therefore minimizes the power dissipation.

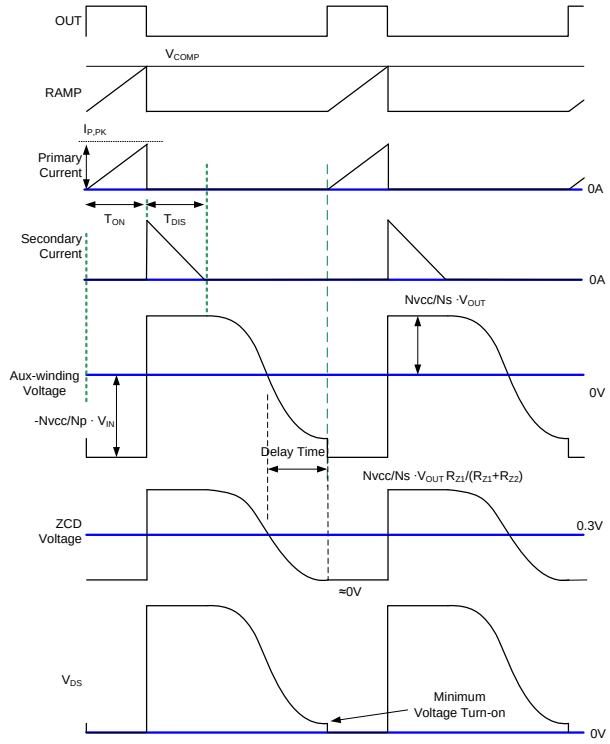
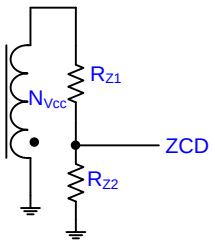


Fig. 13

Programming Maximum ON-time

LD7831 features adjustable maximum ON-time to limit power output in abnormal operation. The selection of maximum ON-time is subject to ZCD resistance as shown in Fig. 14. ZCD resistance can be obtained from below:



$$R_{ZCD} = \frac{R_{Z1} \cdot R_{Z2}}{R_{Z1} + R_{Z2}}$$

Fig. 14

The following table is a suggestion for maximum ON-time setting.

R_{ZCD}	Max. Ton (Typ.)	Suggestion
68k<R_{ZCD}	26μs	80k
52k<R_{ZCD}<68k	20.6μs	60k
40k<R_{ZCD}<52k	17.2μs	46k
30k<R_{ZCD}<40k	15μs	36k
22k<R_{ZCD}<30k	11.5μs	26k
14k<R_{ZCD}<22k	8.2μs	18k
8k<R_{ZCD}<14k	5.2μs	12k
R_{ZCD}<8k	3.3μs	6k

Output Drive Stage

An output stage of a CMOS buffer with typical 250mA/-500mA driving capability is incorporated to drive a power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage is higher than 13V.

Current Sensing and Leading-edge Blanking

The LD7831 detects the primary MOSFET current over CS pin for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike.

Principle of C.C. Operation

Primary side control is applied to eliminate secondary feedback circuit or photo-coupler to reduce the circuit cost. The switching waveforms are shown in Fig.15.

The output current I_O can be expressed as below.

$$Io = \frac{1}{2}\frac{i_{S,PK} \times T_{DIS}}{T_S} = \frac{1}{2}\frac{N_P}{N_S} \times i_{P,PK} \times \frac{T_{DIS}}{Ts} = \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS}}{R_S} \times \frac{T_{DIS}}{T_S}$$

The primary peak current $i_{P,PK}$, inductor current discharge time (T_{DIS}) and switching period (T_S) can be detected by the IC.

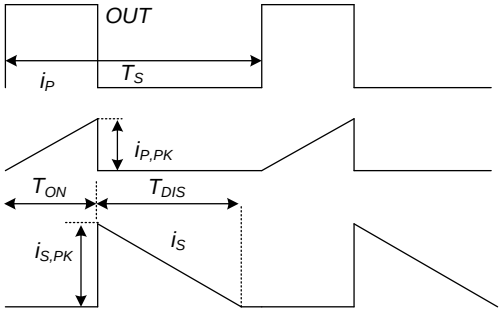


Fig. 15

Compensation of Line Regulation

The output current will vary as the input voltage changes due to sample delay from CS pin, other delay or transformer coupling factor etc.

In order to regulate the output current accurately while the AC input voltage varies in full range, a proper selection for R_C can compensate the output directly as shown in Fig. 1.

The compensation can be expressed as:

$$\Delta V_{CS} = V_{BUS} \times \frac{R_F + R_S}{R_C + R_F + R_S}$$

Where R_C is the compensation resistor, R_F is the filter resistor of CS pin, R_S is the sense resistor.

Current Accuracy Correction

Primary side control is a base on an aux-winding on primary side to feedback a similar as output current. But this feedback value is determined according to leakage inductance of transformer, switching condition (MOSFET parameters), layout pattern, inductance tolerance etc. In order to narrow down the tolerance of output current, it's recommended to add a correction circuit ($R_{S,CP1}$, $R_{S,CP2}$) as shown in Fig. 1 or a variable resistor to modify R_S value. This corrective percentage is about 5%.

$$R_{S'} = 0.95 \times R_S = \frac{(R_S \times R_{S,CP1})}{(R_S + R_{S,CP1})}$$

$$R_{S''} = 0.90 \times R_S = \frac{(R_S \times R_{S,CP2})}{(R_S + R_{S,CP2})}$$

CS Short Protection (CSSP) – Auto Recovery

In order to protect the LED driver from damage due to the shorted sense resistor (R_S), CS pin is built in with CS short protection. See Fig. 16 for it. Once the fault occurs, the CS voltage will drop to GND level instantaneously and enable the protection with CS short protection delay time to avoid from false-triggering.

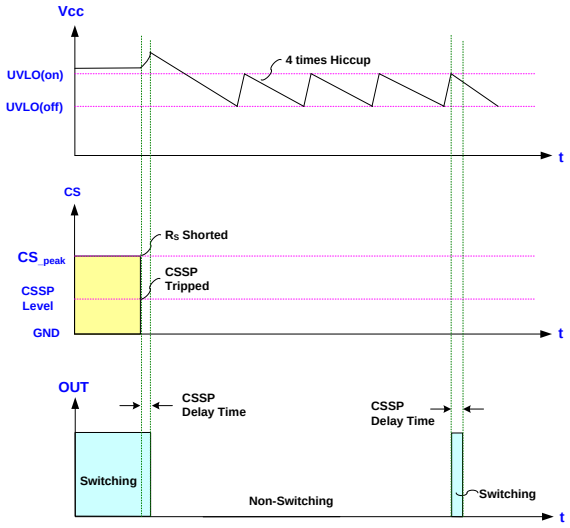


Fig. 16

Output OVP on ZCD

When the LED string open circuit occurs, the reflected output voltage of aux-winding will cause ZCD voltage up. If the ZCD voltage runs up to 3.5V, LD7831 will shut the gate off until the 2nd cycle of Vcc hiccup is tripped, as shown in Fig. 17. The selection of output OVP level is subject to ZCD divide resistance as the below equation:

$$V_{OVP} \times \frac{N_{VCC}}{N_S} \times \frac{R_{Z2}}{R_{Z1}+R_{Z2}} = 3.5V$$

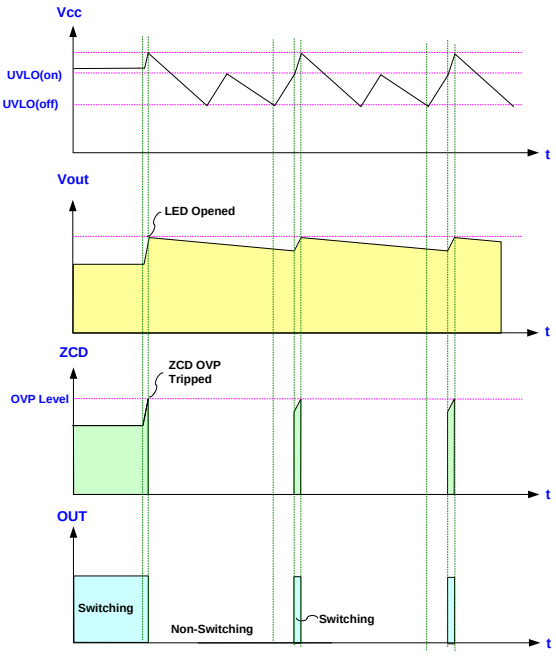


Fig. 17.

LED Short Protection (ZCD UVP) – Auto Recovery

To protect the circuit from damage due to LED short, an auto-recovery type of ZCD UVP protection is implemented for it. Fig. 18 shows the waveforms of the ZCD UVP operation. As LED shorts, the reflected output voltage of aux-winding will cause ZCD voltage drop. If the ZCD voltage decreases below 0.5V for over the delay time of ZCD UVP, the protection will be activated to turn off the gate until the 4th cycle of Vcc hiccup is tripped. The ZCD UVP delay time is to prevent the false-triggering.

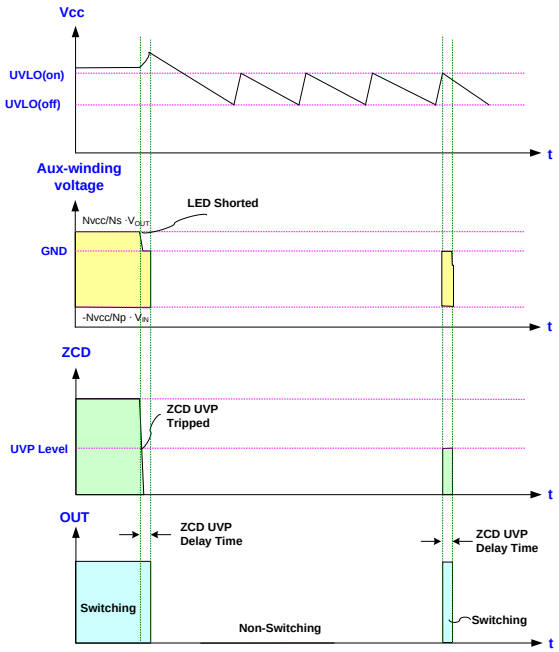


Fig. 18.

OVP (Over Voltage Protection) on Vcc

The maximum rating of the VCC pin is limited below 28V. To protect VCC from damage due to fault condition, the LD7831 is implemented with OVP function on Vcc pin. As soon as the VCC voltage is over OVP threshold (28V), the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the second UVLO(on) arrives. The Vcc OVP function of the LD7831 is an auto-recovery protection. The Fig. 19 shows its operation. Upon removal of the OVP condition will resume the VCC level and the output operation.

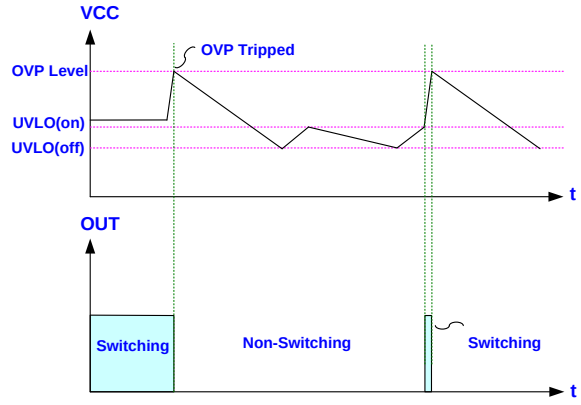


Fig. 19

Fault Protection

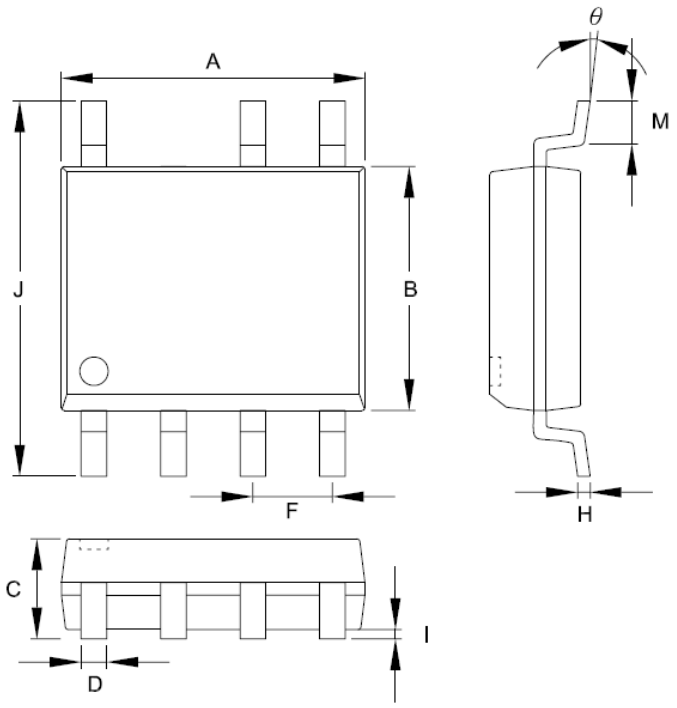
There are several critical protections integrated in the LD7831 to protect the power supply or adapter from being damaged. Those damages usually come from open or short condition on the pins of LD7831.

Under the conditions listed below, the gate output will turn off immediately to protect the power circuit ---

1. CS pin short and floating
2. Comp pin short and floating
3. ZCD short

Package Information

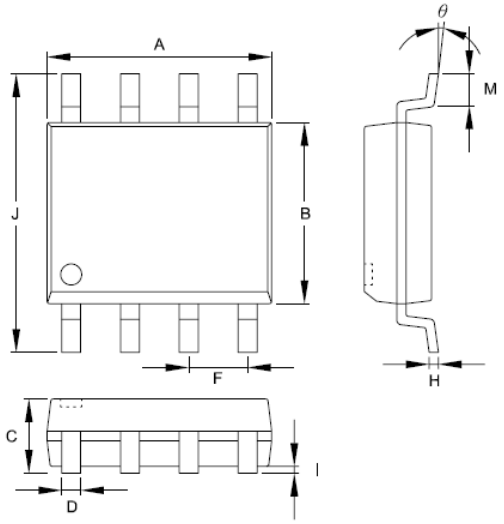
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

SOP-8



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Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	2014/04/14	Original Specification.