High Power Factor LED Controller with HV Start-up

REV: 00

General Description

The LD7832 is a buck solution with high PFC control for LED lighting. It features HV start-up, easy to design with minimum cost and PCB size. The device operates in transition(TM) mode and integrates with complete safety requirement protections.

With HV start-up technology, high power factor and TM control, the system is enabled to achieve high PF and high efficiency to meet most of the international standard. The LD7832 also features LED open protection (OVP), LED short protection (ZCD UVP), over current protection (OCP), CS short protection (CSSP), open feedback protection and over temperature protection (OTP). It makes the circuit designers easily to meet most safety requirements in either normal or abnormal test.

Features

- Built-in 600V HV startup
- High power factor controller integrated
- High efficiency transition mode operation
- Accurate current regulation
- Wide range of UVLO (17.5 V_{ON} and 8 V_{OFF})
- VCC OVP (VCC over Voltage Protection)
- ZCD OVP (Adj. Output Voltage Protection)
  (Option: with ZCD OVP disabled, LD7832A)
- ZCD UVP (ZCD under voltage protection)
- OCP (Cycle by cycle current limit)
- CSSP (CS short protection)
- Open feedback protection
- OTP (Over Temperature Protection)
- 250/-500mA Driving Capability

Applications

- LED Lamp、LED bulb Application

Typical Application

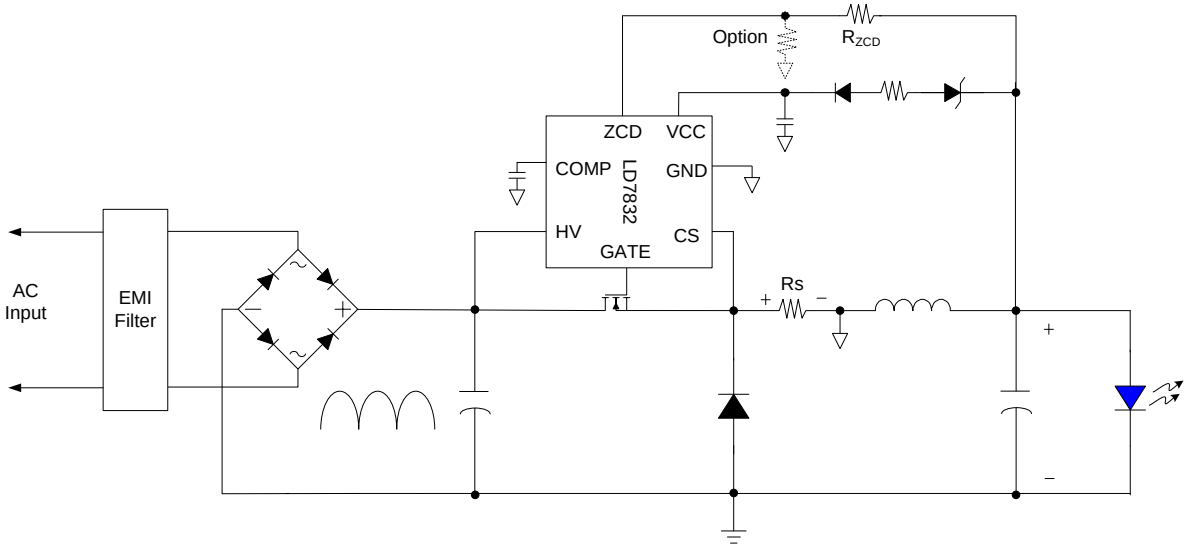
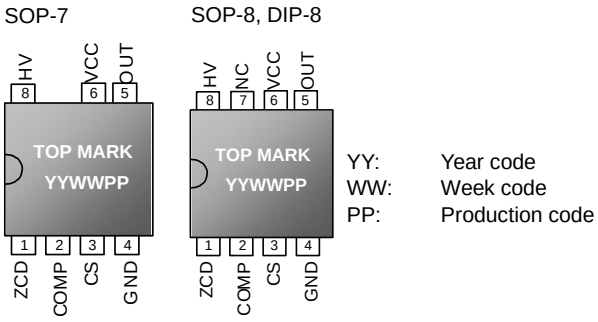


Fig. 1 Application circuit

Pin Configuration



Ordering Information

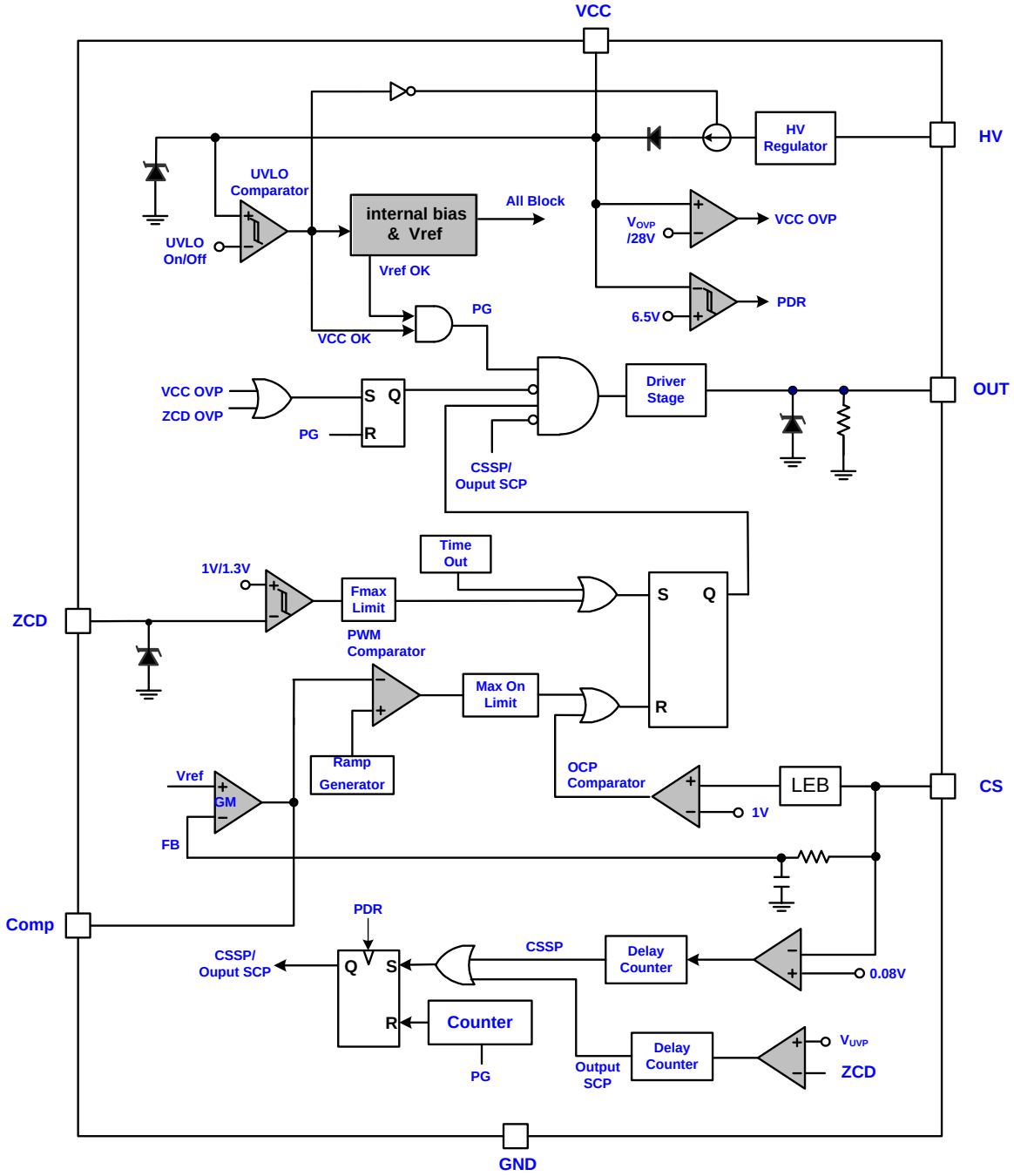
Part number	Package	Top Mark	Shipping
LD7832 GR	SOP-7	LD7832 GR	2500 /tape & reel
LD7832 GS	SOP-8	LD7832 GS	2500 /tape & reel
LD7832 GN	DIP-8	LD7832 GN	3600 /tube /Carton

The LD7832 is ROHS compliant/ green packaged.

Pin Descriptions

Pin	NAME	FUNCTION
1	ZCD	Quasi resonance detector
2	COMP	Compensation pin for internal error amplifier
3	CS	Current sense pin, connect to sense the MOSFET current for FB and OCP.
4	GND	Ground
5	OUT	Gate signal output
6	VCC	Power supply to VCC
7	NC	No connection
8	HV	Connect this pin to the positive of main bulk cap to provide the startup current for controller. When VCC is UVLO on, the HV loop will open and turn off internal current source to minimize the power loss.

Block Diagram



Absolute Maximum Ratings

VCC	-0.3 ~ 30V
CS	-3 ~ 6V
ZCD	-0.3 ~ 6V
IZCD	-4 ~ 2mA
HV	-0.3 ~ 600V
COMP	-0.3 ~ 6V
OUT	-0.3 ~ 30V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-7/SOP-8, θ_{JA})	160°C/W
Package Thermal Resistance (DIP-8, θ_{JA})	100°C/W
Power Dissipation (SOP-7/SOP-8)	250mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	400mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV pin)	2.5KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Vcc	13	24	V
Vcc pin capacitor	4.7	22	μF
Comp pin capacitor	0.1	2.2	μF
Operating Junction Temperature Range	-40	125	°C
Operating Ambient Temperature Range	-40	85	°C

Electrical Characteristics

(V_{CC}=14.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High voltage Supply(HV Pin)					
High-voltage Current Source	V_{CC}<6V , HV=80V	0.8	1	1.2	mA
	6V<V_{CC}<$UVLO_{(ON)}$	2.5	3	3.5	mA
Off-state Leakage Current	V_{CC}>UVLO(ON), HV=600V	-	-	35	μA
Supply Voltage (VCC Pin)					
Startup Current	V_{CC}<$UVLO_{(ON)}$ @V_{CC}=14V	-	280	350	μA
Operating Current	COMP pin open, ZCD=12V	-	1.2	1.6	mA
(with 1nF Load on OUT pin)	V_{CC} OVP tripped	-	0.4	0.6	mA
$UVLO_{(OFF)}$		7.5	8	8.5	V
$UVLO_{(ON)}$		16.5	17.5	18.5	V
VCC OVP Level		26	28	30	V
HV Self Bias (Linear Regulator)		12	13	14	V
De-latch V_{CC} Voltage	PDR	6.0	6.5	7.5	V
Compensation (COMP Pin)					
Open Loop Voltage	COMP pin open	5	5.5	6	V
On Time	V_{COMP}=2V	5	6	7	μs
Current Sensing (SOURCE Pin)					
Reference Voltage(V_{REF})		0.194	0.2	0.206	V
OCP Threshold (cycle-by-cycle)		0.9	1	1.1	V
LEB Time[1]		-	250	-	ns
The trip level for Rs Short protection		0.05	0.08	0.1	V
Delay Counter for RsSP		-	20	-	ms
Zero Current Detector (ZCD Pin)					
I_{ZCD_OVP} Threshold		180	200	220	μA
Upper Clamp Voltage	ZCD_{IN}=12V	4.9	5.3	5.7	V
Lower Clamp Voltage	ZCD_{IN}=0V	0.2	0.3	0.4	V
Input Voltage Threshold[1]		-	1	-	V
	Hysteresis	-	0.3	-	V
I_{ZCD_OVP} Threshold at ZCD pin	V_{ZCD_OVP}=I_{ZCD}*R_{ZCD}+5.3V	180	200	220	μA
The trip level for ZCD UVP[1]		-	4.2	-	V
Delay Counter of ZCD UVP		-	20	-	ms

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum (ON+OFF)-Time, $F_{SW,MAX}$ (ZCD Pin)					
$F_{SW,MAX}$[1]	Minimum (ON+OFF)-Time	200	-	300	KHz
Gate Drive Output (OUT Pin)					
Output Low Level	V_{CC}=15V, I_O=20mA	-	-	0.5	V
Output High Level	V_{CC}=15V, I_O=20mA	8	-	VCC	V
Output High Clamp Level	V_{CC}=16V	12	13	14	V
Rising Time[1]	V_{CC} =15V, C_L=1nF	-	100	-	ns
Falling Time[1]	V_{CC} =15V, C_L=1nF	-	25	-	ns
Starter					
Start Timer Period		60	75	90	μs
OTP (Over Temp. Protection)					
OTP Trip Level[1]		135	145	155	°C
OTP Hysteresis[1]		20	30	40	°C

Note: (1) Guaranteed by design

Typical Performance Characteristics

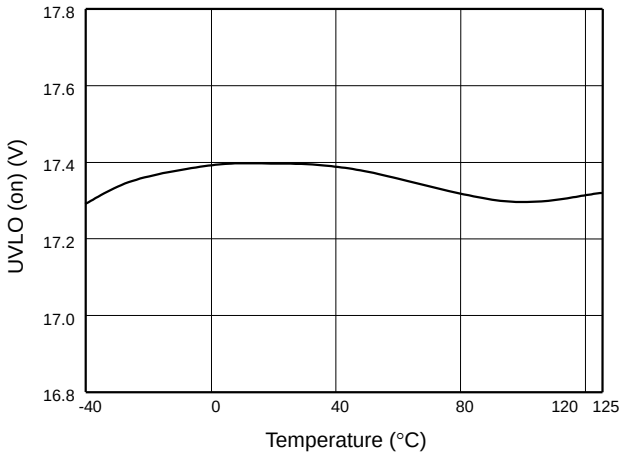


Fig. 1 UVLO (on) vs. Temperature

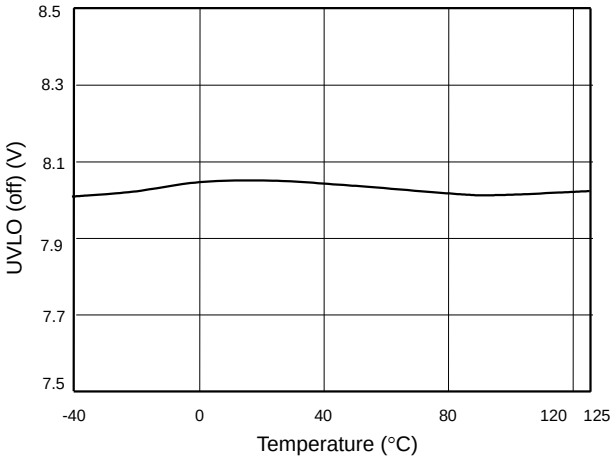


Fig. 2 UVLO (off) vs. Temperature

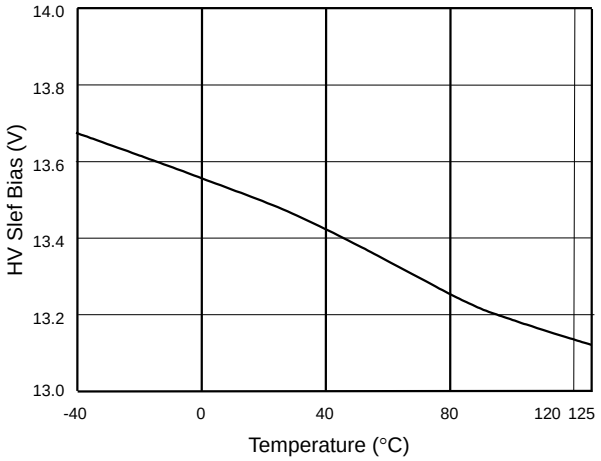


Fig. 3 HV Slef Bias vs. Temperature

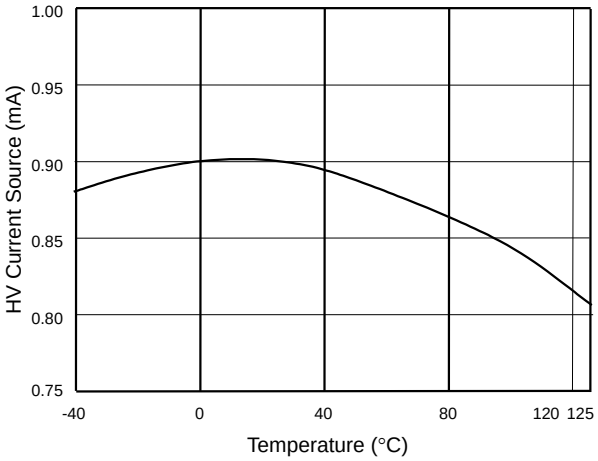


Fig. 4 HV Current source(Vcc=1V) vs. Temperature

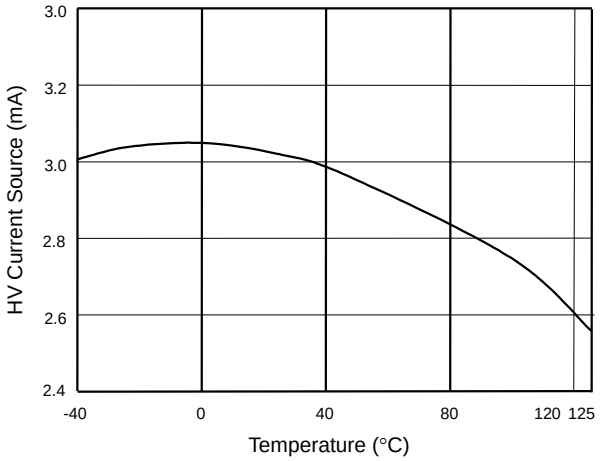


Fig. 5 HV Current source(Vcc=14V) vs. Temperature

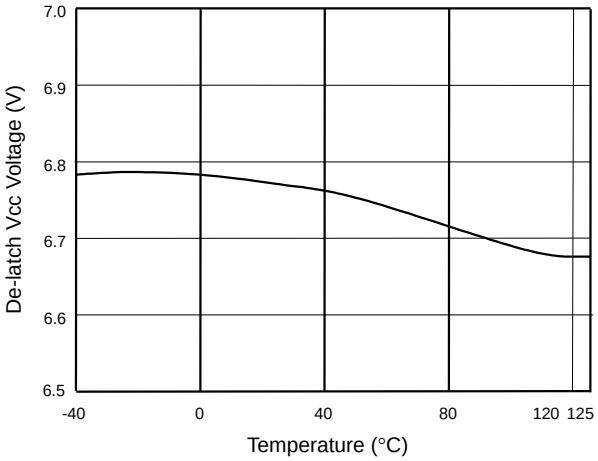


Fig. 6 De-latch Vcc Voltage vs. Temperature

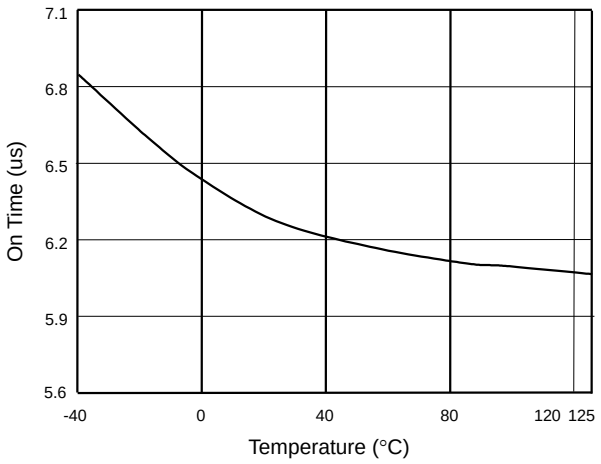


Fig. 7 On Time(Comp=2V) vs. Temperature

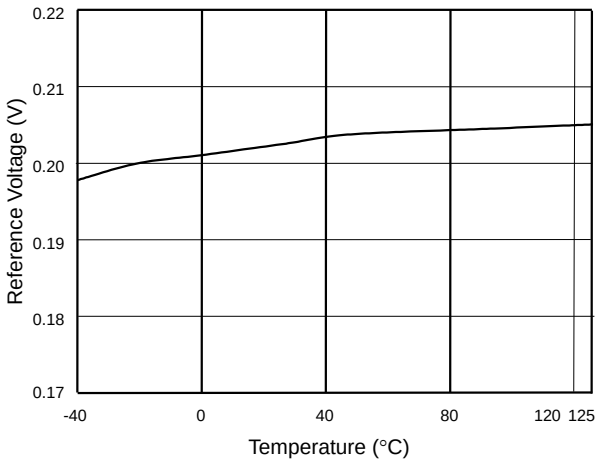


Fig. 8 Reference Voltage vs. Temperature

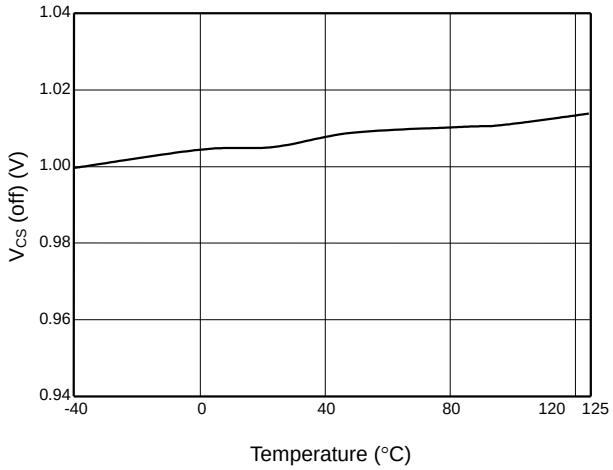


Fig. 9 V_{CS} (off) vs. Temperature

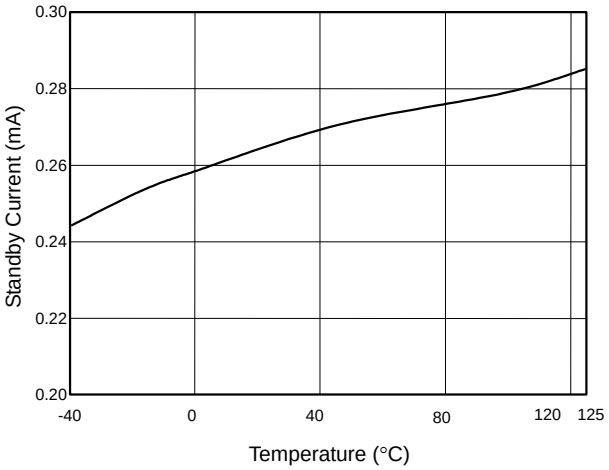


Fig. 10 Standby Current vs. Temperature

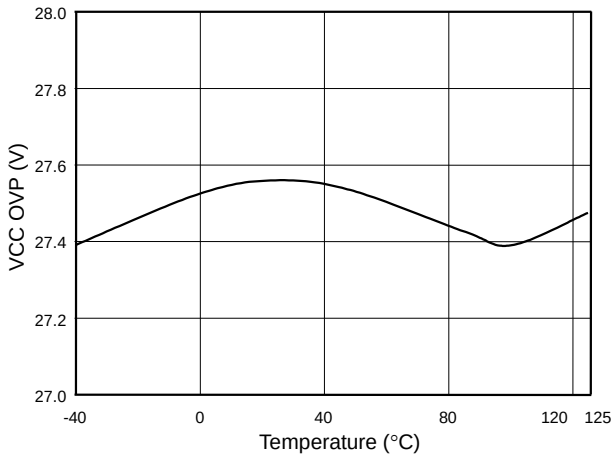


Fig. 11 VCC OVP vs. Temperature

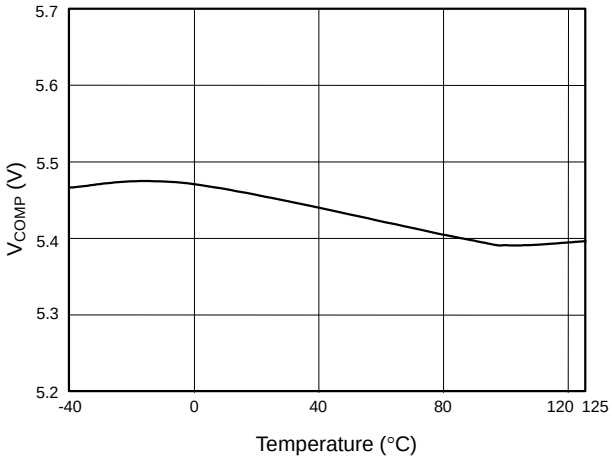


Fig. 12 V_{COMP} open loop voltage vs. Temperature

Application Information

Operation Overview

LD7832 is an LED controller for lighting application. The transition mode (TM) technique meets the requirement of high power factor in high efficiency. It minimizes the external component counts and the PCB size for compact application.

LD7832 is also designed to operate in voltage-mode TM mode. The switch turn-on time is fixed while the turn-off time varies in steady state. Therefore, the switch frequency changes in response to the different voltages. The affected frequency reduces EMI noise. LD7832 also features LED open protection, LED short protection, over current protection, CS short protection, open feedback protection, and over temperature protection. No extra mains voltage sensing is required as what the traditional current mode PFC controllers behaves for power saving.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a resistor to power up the PWM controller. However, it consumes too significant power to meet the current power saving requirement. In most cases, larger resistor carries larger resistance; it wastes more time to startup.

To achieve the optimized topology, as shown in Fig.1, LD7832 is implemented with a high-voltage startup circuit on HV pin for it. During startup, a high-voltage current source sinks current from the output of full-bridge rectifier to provide the startup current and charge the VCC capacitor. Once VCC drops below PDR, the charge current will remain at 1mA to protect the circuit from being damaged, even in case VCC pin is shorted to ground. In contrast, the charge current will increase to 3mA once VCC rises above PDR voltage threshold during start-up. Meanwhile, the VCC supply current is as low as 280μA that most of the HV current is reserved to charge the VCC capacitor. By using such configuration, the turn-on delay time will be almost same no matter under low-line or high-line conditions.

As the VCC voltage rises higher than UVLO(on) to power the LD7832 and further to deliver the gate drive signal, the high-voltage current source will be disabled and the supply current is provided from the inductor. Therefore, it would reduce the power loss on the startup circuit and perform highly power saving.

An UVLO comparator is embedded to detect the voltage on the VCC pin to ensure the supply voltage enough to power on the LD7832 controller and in addition to drive the power MOSFET. As shown in Fig. 2, a hysteresis is provided to prevent the shutdown from the voltage dip during startup.

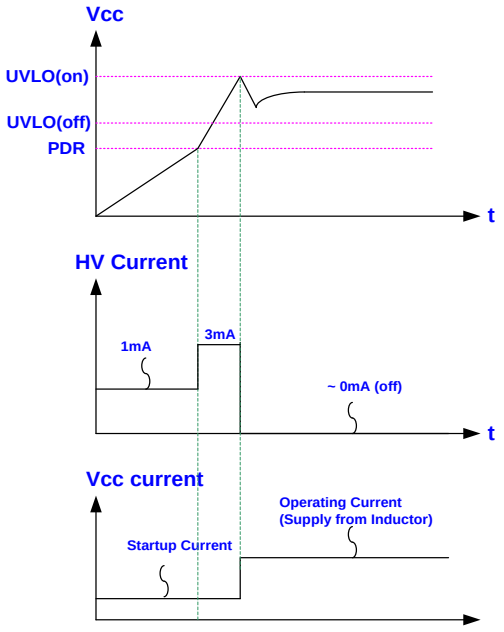


Fig. 2

Ramp Generator Block and Zero Current Detection (ZCD)

Fig. 3 shows typical ramp generator block and ZCD block. The COMP pin voltage and the output of the ramp generator block are compared to determine the MOSFET On-time, as shown in Fig. 4.

The LD7832 features transition mode operation. The zero current detection block circuit detects the ZCD signal to turn on the MOSFET soon after the voltage across ZCD falls to 1V and also the current through the inductor reaches zero. Instead, if there's no signal detected within 70μs, the time-out will generate a signal to turn on MOSFET to ensure the system operate properly.

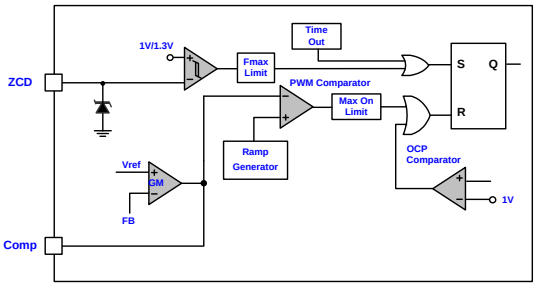


Fig. 3

During the delay time as shown in Fig. 4, the junction capacitor of the MOSFET resonates with the inductor and the drain-source voltage (VDS) decreases accordingly. So, the MOSFET consumes less voltage and the power dissipation will be minimized.

As recommended in Fig. 1, only one resistor (RZCD) is required to connect ZCD pin in series with the inductor to detect the inductor signal and protect ZCD pin from damage. It makes the circuit simple and easy to design with. Fig. 4 shows the related waveforms between the changing inductor voltage and ZCD voltage. ZCD pin is clamped at 5.3V or 0.3V in accordance with various inductor voltages.

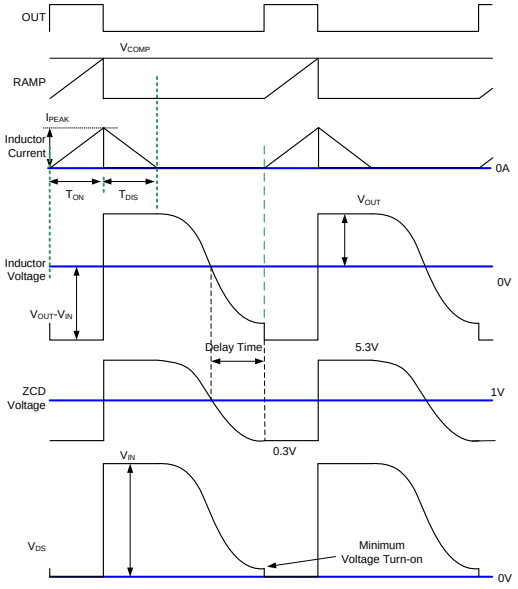


Fig. 4

LED Short Protection (ZCD UVP) – Auto Recovery

To protect the circuit from damage due to LED short condition, an auto-recovery type of ZCD UVP protection is implemented for it. Fig. 5 shows the waveforms of the ZCD UVP operation. In LED short condition, the reflected output voltage of inductor will cause ZCD voltage drop. If the ZCD voltage sinks below 4.3V for more than the delay time of ZCD UVP, the protection will be activated to turn off the gate until the 4th cycle of Vcc hiccup is tripped. The ZCD UVP delay time is to prevent the false-triggering.

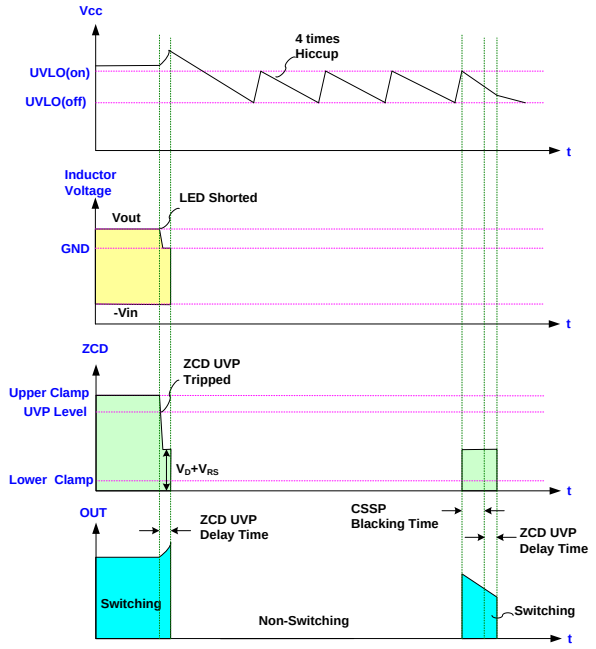


Fig. 5

Over Current Protection (OCP)

The LD7832 detects the MOSFET current from the CS pin, which is for the pulse-by-pulse current limit and output current feedback. The maximum voltage threshold of the CS pin is set at 1.0V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK\,(MAX)} = \frac{1.0V}{R_S}$$

CS Short Protection (CSSP) – Auto Recovery

In order to prevent the LED driver from damage due to the shorted sense resistor (Rs), CS pin is built in with CSSP protection. See Fig. 6. Once the fault condition occurs, the CS voltage will drop to GND level instantaneously and it will enable the protection with CSSP delay time to avoid the false-trigger. When VCC achieves the UVLO(on), the LD7832 will start the CSSP blanking time to ignore CSSP function to pass the start-up transient.

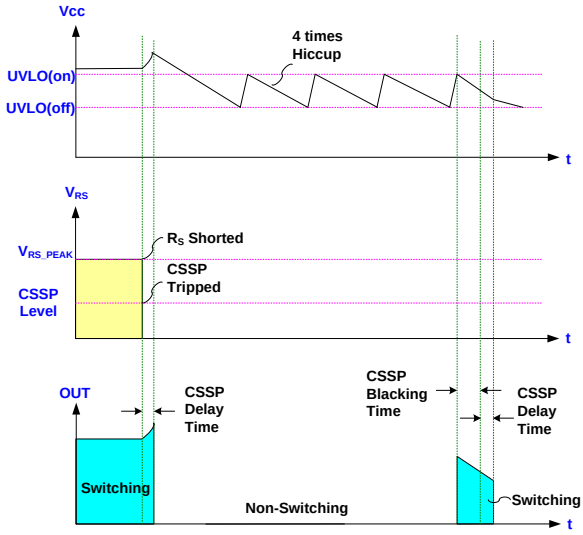


Fig. 6

Over Voltage Protection (VCC OVP)

The maximum rating of the VCC pin is limited below 30V. To prevent VCC from damage due to fault condition, the LD7832 is implemented with OVP function on VCC pin. As soon as the VCC voltage is over OVP threshold voltage, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(on) arrives. The VCC OVP function of the LD7832 is an auto-recovery protection. The Fig. 7 shows its operation. Upon removal of the OVP condition will resume the VCC level and the output operation

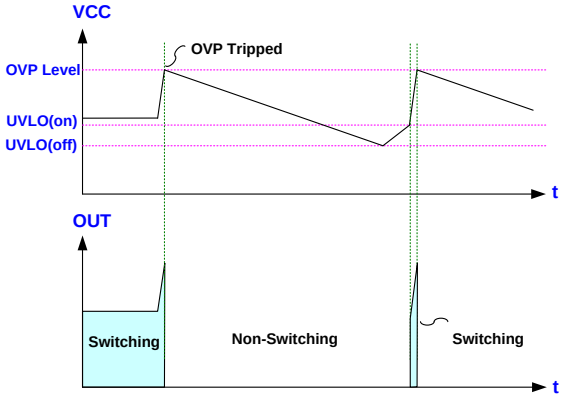


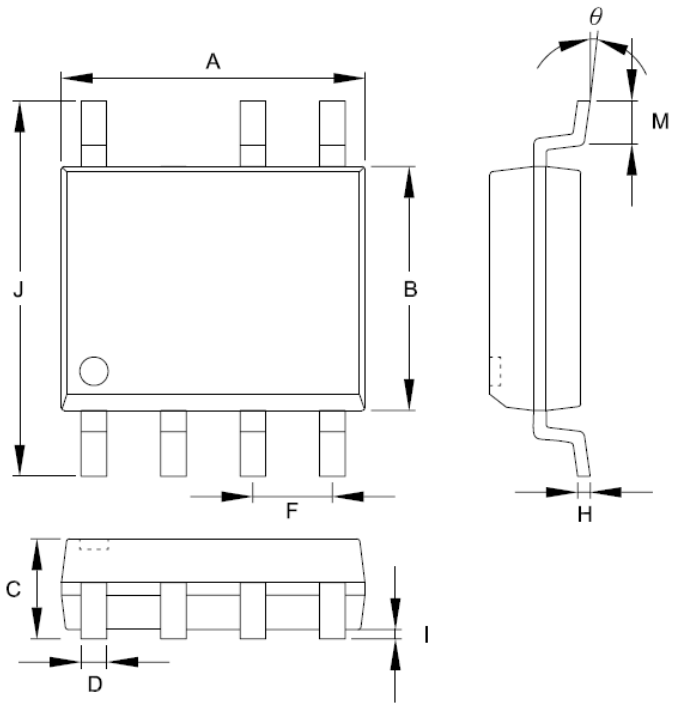
Fig. 7

Output Drive Stage

An output stage of a CMOS buffer, with typical 250mA/-500mA driving capability, is incorporated to drive the power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage rises over 13V.

Package Information

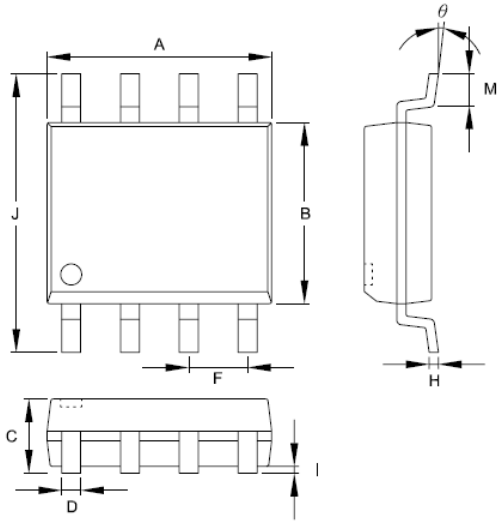
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

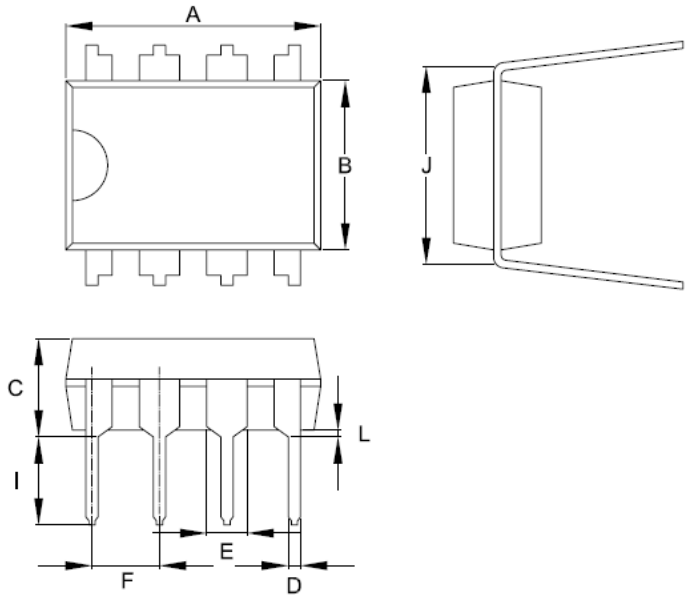
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	2013/04/12	Original Specification.