High Power Factor Primary Side Flyback LED Controller With TRIAC Dimming

REV: 00

General Description

The LD7833 is a primary side regulation Flyback controller with power factor for TRIAC dimmable LED driver. The LD7833 provides constant current (CC) operation requiring neither photo-coupler nor secondary control circuit. It minimizes the components counts in a tiny package. Those make it easy to design for cost-effective applications.

With high voltage start-up technology, high power factor and TM control, the start-up time and MOSFET switching losses could be minimized efficiently.

With completed protection built in this IC, such as over-voltage protection (OVP), over-current protection (OCP) and short circuit protection (SCP), the device is capable to meet the safety requirements.

Features

- High Voltage (700V) Startup Circuit
- Transition Mode Operation
- High Power Factor
- Dimmable by TRIAC dimmer
- VCC Over Voltage Protection
- Over Current Protection
- Output Short Circuit Protection
- Over Temperature Protection
- Built-in Phase Angle Cut-off Function
- Adjustable Output OVP
- 250/-500mA Driving Capability
- Internal Over Temperature Protection
- SOP-7/8 Package

Applications

- LED Lighting System

Typical Application

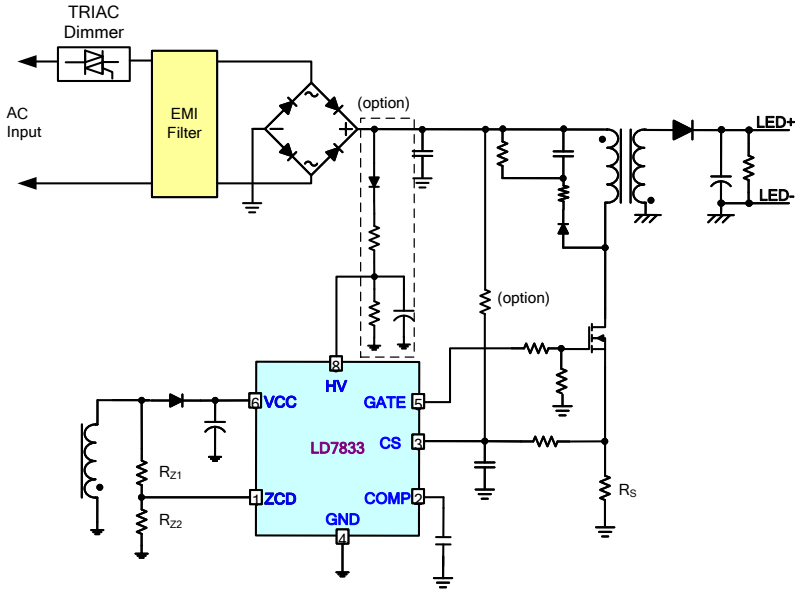
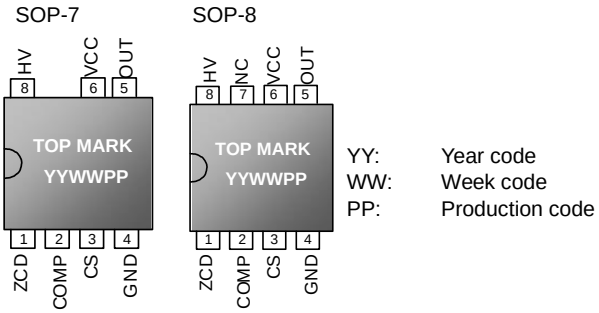


Fig. 1 Application Circuit

Pin Configuration



Ordering Information

Part number	Package	Top Mark	Shipping
LD7833 GR	SOP-7	LD7833 GR	2500 /tape & reel
LD7833 GS	SOP-8	LD7833 GS	2500 /tape & reel

The LD7833 is ROHS compliant/ green packaged.

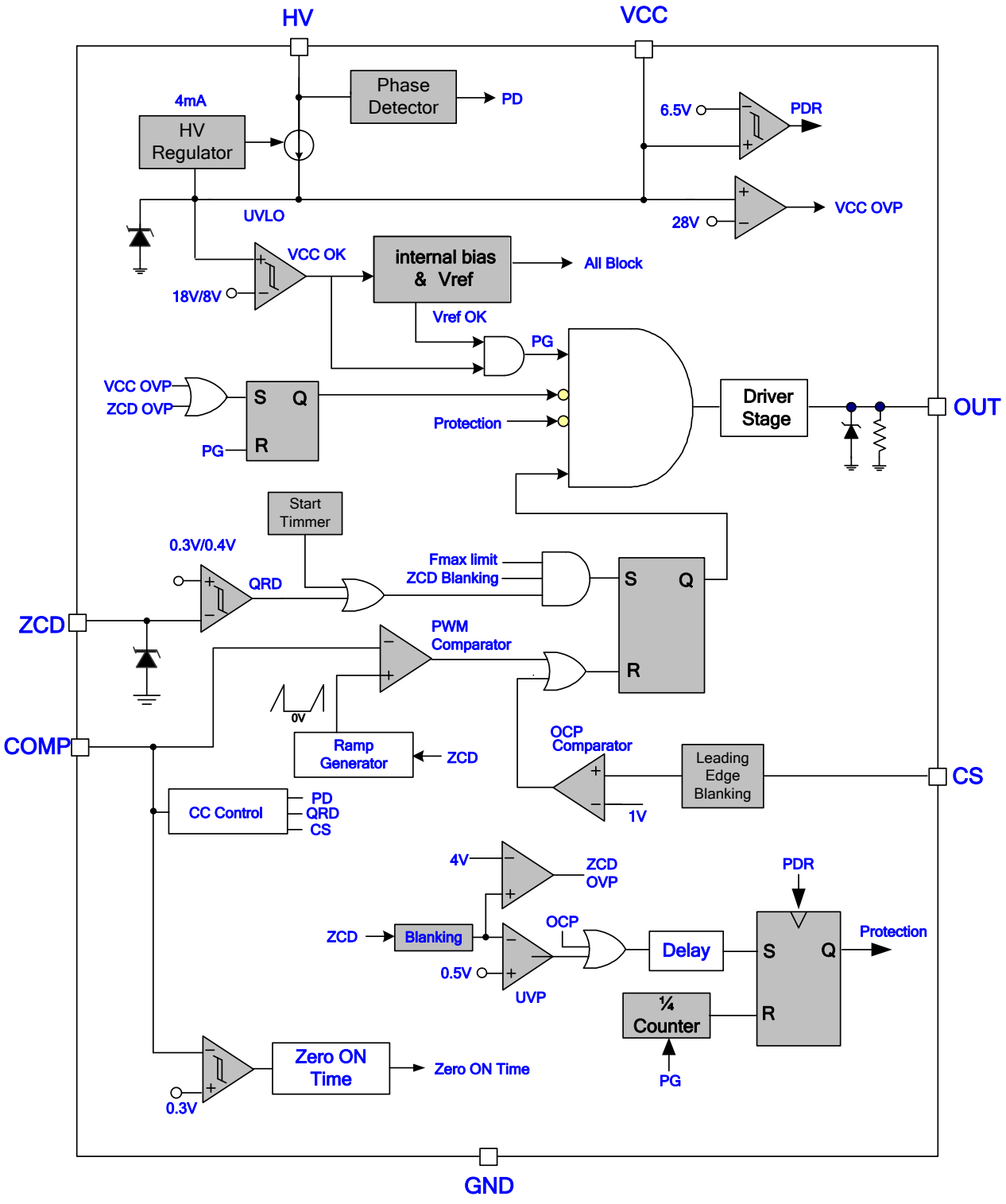
Protection Mode

Part number	VCC_OVP	ZCD_OVP	CS Open/short	OLP/ Output Short
LD7833	Auto recovery	Auto recovery	Auto recovery	Auto recovery

Pin Descriptions

Pin	NAME	FUNCTION
1	ZCD	Quasi resonance detector, which supports programmable phase angel cut-off setting. This pin receives the auxiliary winding voltage through a resister divider and detects the quasi resonance. It also provides protection for over-voltage output.
2	COMP	Loop compensation pin, connect a capacitor with it to stabilize the control loop.
3	CS	Current sense pin, connect it to sense the MOSFET current for CC loop and OCP.
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Power source VCC pin
7	NC	Not connected.
8	HV	Connect this pin to the positive of main bulk cap to provide the startup current for controller and detects phase angle of TRIAC.

Block Diagram



Absolute Maximum Ratings

VCC	-0.3 ~30V
HV	-0.3 ~700V
OUT	-0.3 ~30V
COMP, ZCD	-0.3 ~6V
CS,	-0.3 ~6V
ZCD Pin Clamping Current	-1.5mA~100μA
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-7/SOP-8, θ_{JA})	160°C/W
Power Dissipation (SOP-7/SOP-8, Tj=125°C, Ta=85°C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV pin)	2.5KV
ESD Voltage Protection, Human Body Model (HV pin)	1KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-20	125	°C
Supply VCC Voltage	10	26	V
Vcc pin capacitor	4.7	22	μF
Comp pin voltage	0.8	4	V
Comp pin capacitor	0.47	2.2	μF
CS pin capacitor	47	470	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(VCC=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High voltage Supply(HV Pin)						
High-voltage Current Source	VCC=4V , HV=80V	I_{HV_LO}	-	1.3	-	mA
	VCC=15V,HV=80V	I_{HV_HI}	-	4.5	-	mA
Off-state Leakage Current	VCC>UVLO(ON), HV=500V	I_{HV_OFF}	-		60	μA
Detection Threshold for TRIAC Phase Low		V_{DC2L_110V}	8.5	10	-	V
		V_{DC2L_220V}	18.5	20	-	V
Delay Time for BNI to BNO	*	T_{BNIO}	-	60	-	ms
Delay Time for BNO to BNI	*	T_{BNOI}	-	120	-	ms
Supply Voltage (VCC Pin)						
Startup Current	VCC<UVLO(ON)	I_{ST}	-	70	90	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V, ZCD=0	I_{OP_LO}	-	1	-	mA
	VCC OVP	I_{OP_OVP}	0.42	0.5	-	mA
	ZCD UVP	I_{OP_UVP}	0.9	1.15	-	mA
UVLO(OFF)		V_{OFF}	7.5	8	8.5	V
UVLO(ON)		V_{ON}	17	18	19	V
HV Self Bias for Normal Operation		V_{LDO_LO}	-	10	-	V
HV Self Bias for Start-up		V_{LDO_HI}	-	16	-	V
De-Latch Voltage	PDR	V_{PDR}	6.0	6.5	7	V
VCC OVP Level		V_{OVP}	26.5	28	29	V
VCC OVP De-bounce Time *		T_{DEB_OVP}	-	250	-	μs
Protection De-Latch Counter *	ZCD UVP	T_{CONT}	-	4	-	cycle
CC Integrator (COMP Pin)						
COMP open		V_{CMP}	4.5	4.7	4.9	V
Burst Level		V_{BST}	0.24	0.3	0.36	V
Maximum On Time	COMP open	T_{ON_MAX}	9.5	11.5	13.5	μs

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Current Sensing (CS Pin)						
Current Sense Input Threshold Voltage		V_{OCP}	0.94	0.97	1	V
	During phase low	V_{OCP_L}	-	0.1	-	V
Soft Start Time *	V_{OCP}:0.4~1.0	V_{OCP_ST}	5	10	15	ms
LEB Time*		T_{LEB}	350	450	550	ns
Constant Current Accuracy tolerance by chip (Except component variation, as X'FMR , Rcs, Input voltage, TRIAC phase …etc . parameters of system)		K%	-3.5	-	3.5	%
Zero Current Detector (ZCD Pin)						
Upper Clamp Voltage		V_{ZH}	4.3	4.6	4.9	V
Lower Clamp Voltage		V_{ZL}	-0.3	-	0	V
Input Voltage Threshold		V_{ZCD}	-	0.2	-	V
	Hysteresis	Δ_{ZCD}	-	0.1	-	V
ZCD Blanking Time		T_{BNK_ZCD}	2	2.5	3	µs
UVP Detect Level		V_{UVP}	0.3	0.5	0.8	V
UVP Delay Time*		T_{UVP}	20	40	60	ms
ZCD OVP		V_{ZOVP}	3.8	4	4.2	V
ZCD OVP De-bounce*		T_{ZOVP}	170	270	370	µs
Minimum (ON+OFF)-Time						
Minimum ON+OFF-Time	$F_{S,MAX}$(300kHZ)	T_{S_MAX}	2.83	3.33	3.83	µs
Gate Drive Output (OUT Pin)						
Output High Clamp Level	VCC=16V	V_{G_CLAMP}	10.5	12	13	V
Rising Time *	VCC =15V, CL=1000pF	T_{G_RISE}	-	90	-	ns
Falling Time *	VCC =15V, CL=1000pF	T_{G_FALL}	-	50	-	ns
Time Out						
Time Out	After Soft Start	$T_{IMEOUT2}$	-	150	-	µs
	During Soft Start	$T_{IMEOUT1}$	45	55	65	µs
Internal OTP (Over Temp. Protection)						
OTP Trip Level *		OTP	-	140	-	°C
OTP Hysteresis *		Δ_{OTP}	-	30	-	°C

*: Guaranteed by design.

Typical Performance Characteristics

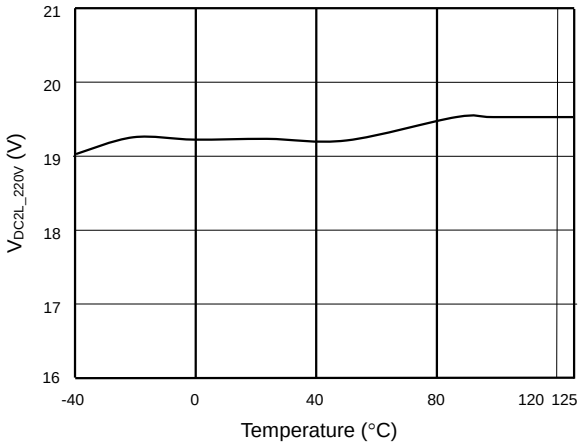


Fig. 2 V_{DC2L_220V} vs. Temperature

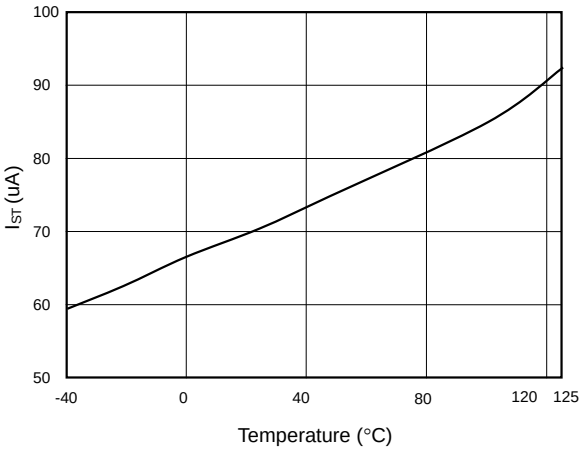


Fig. 3 I_{ST} vs. Temperature

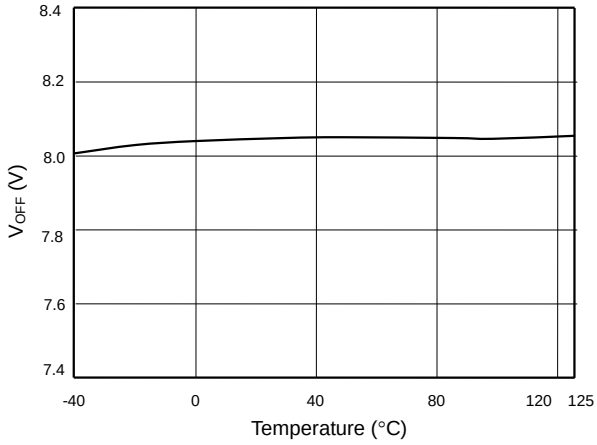


Fig. 4 V_{OFF} vs. Temperature

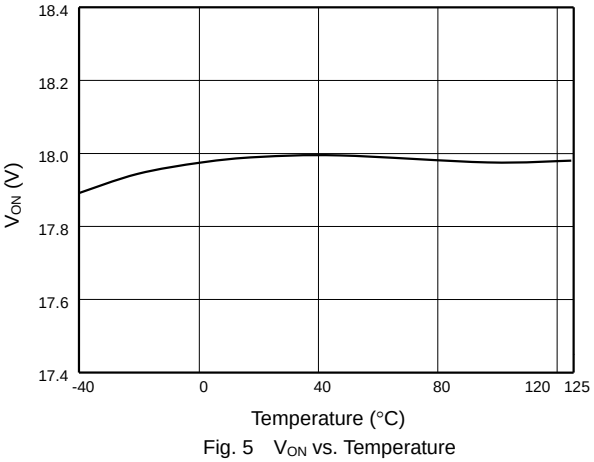


Fig. 5 V_{ON} vs. Temperature

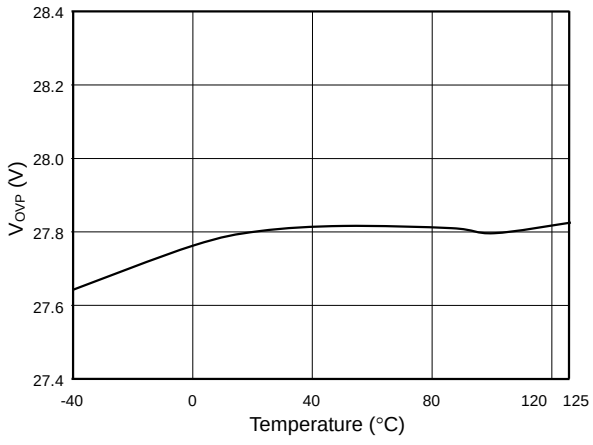


Fig. 6 V_{OVP} vs. Temperature

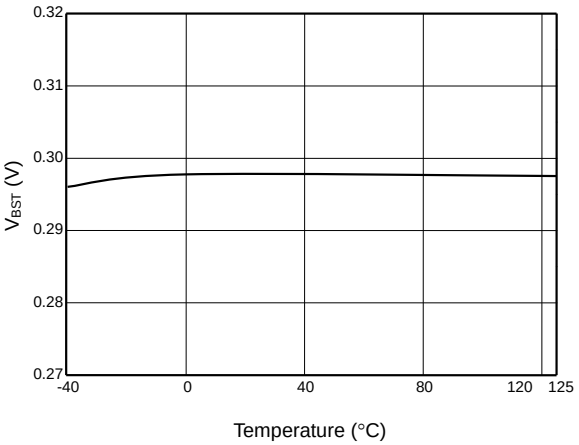


Fig. 7 V_{BST} vs. Temperature

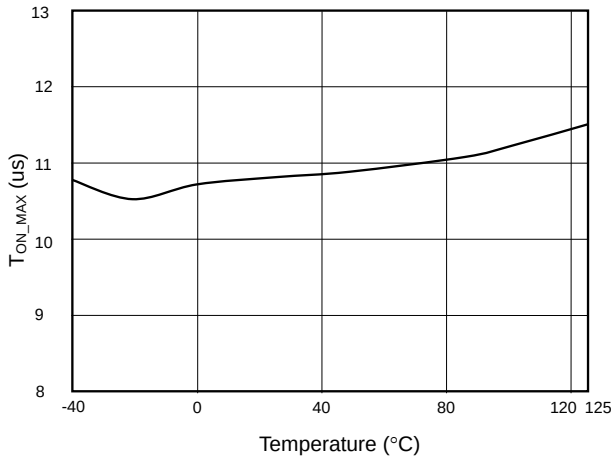


Fig. 8 T_{ON_MAX} vs. Temperature

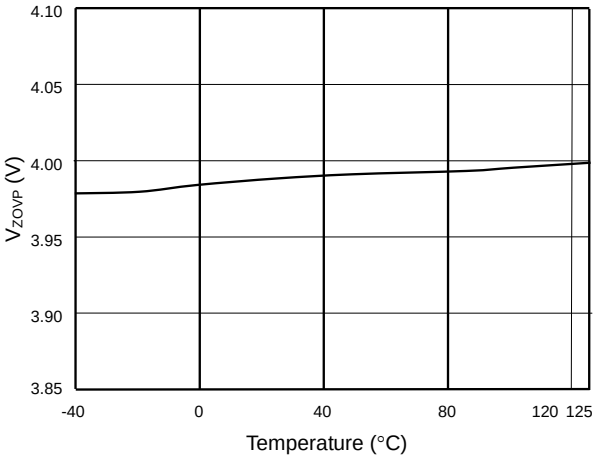


Fig. 9 V_{ZOVP} vs. Temperature

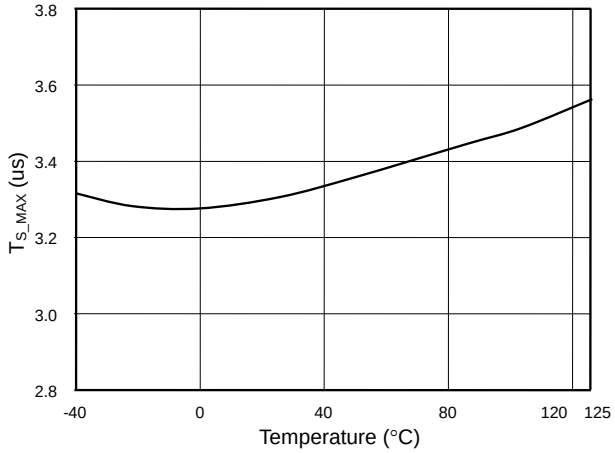


Fig. 10 T_{S_MAX} vs. Temperature

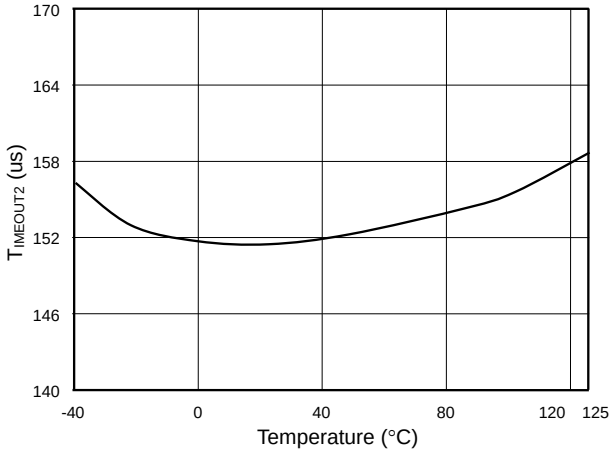


Fig. 11 $T_{IMEOUT2}$ vs. Temperature

Application Information

Operation Overview

The LD7833 is a primary side regulation Flyback controller with power factor for TRIAC dimmable LED driver. It provides constant current (CC) operation and requires neither photo-coupler nor secondary control circuit. It integrates lots of functions to reduce the external components counts and the size. Its major features are described as below.

The LD7833 can operate in voltage-mode. The turn-on time of the switch is fixed while the turn-off time is various in steady states. Therefore, the switching frequency changes in accordance with the input voltage variation. It also features HV pin to achieve fast start up and TRIAC phase detection.

Internal High-Voltage Startup Circuit

In order to achieve fast start-up and keep VCC energy enough in deep dimming situation, the HV pin is built in LD7833 as shown in Fig. 12 and Fig. 13. At startup transient, a high-voltage current source sinks current from the full-bridge rectifier to provide the startup current and charge VCC capacitor C1 at the same time. If VCC is below PDR, the charge current will remain at 1.3mA to protect the circuit from being damaged, even as VCC pin is shorted to ground. In contrast, the charge current will increase to 4mA as VCC rises above PDR voltage threshold during start up.

The LD7833 will be turned on soon as the VCC's voltage rises over UVLO(ON). It will also drive the high voltage start-up circuit to operate as a regulator and maintain the VCC voltage at UVLO(ON) level, particularly in deep dimming condition. The current consumed is 4mA max. After 40ms of UVLO(ON), the high voltage regulator will be set at 10V to reduce the power loss. Well, in order to supply sufficient VCC voltage in normal condition, it requires auxiliary voltage source to operate. The high voltage regulator will protect the controller from shut-off at load transient as VCC voltage drops below UVLO-off. HV regulator will be disabled soon as the IC enters protection mode, as SCP, OVP, OTP protection…etc.

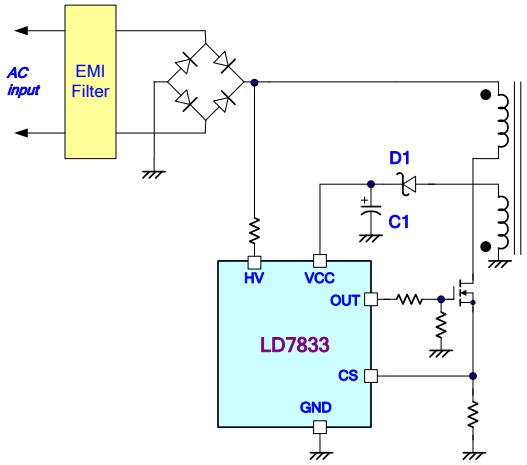


Fig. 12

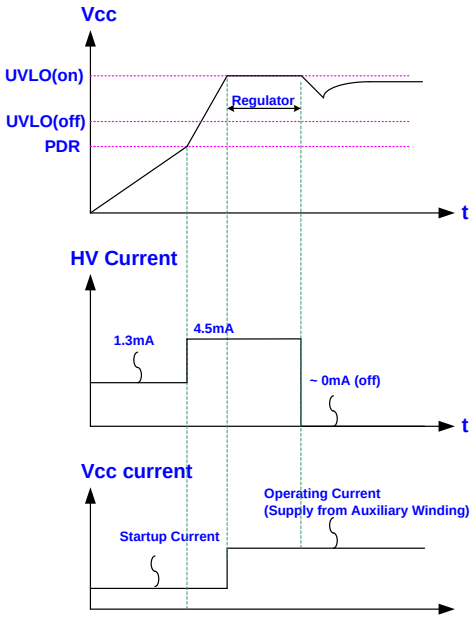


Fig. 13

Ramp Generator Block and Zero Current Detection (ZCD)

Fig. 14 shows typical ramp generator block and ZCD block. The COMP pin voltage and the output of the ramp generator block are compared to determine the MOSFET ON-time, as shown in Fig. 15.

It will shut down the driving output if COMP pin voltage falls below the threshold of zero ON-time. This optimizes the efficiency in power saving in most conditions.

As ZCD pin voltage decrease to 0.3V, the current through the transformer will drops below zero. The Zero current detector will detect auxiliary winding signal to drive MOSFET that will activate the LD7833 to enter transition-mode. The ZCD comparator would not operate if ZCD pin voltage remains above 0.4V.

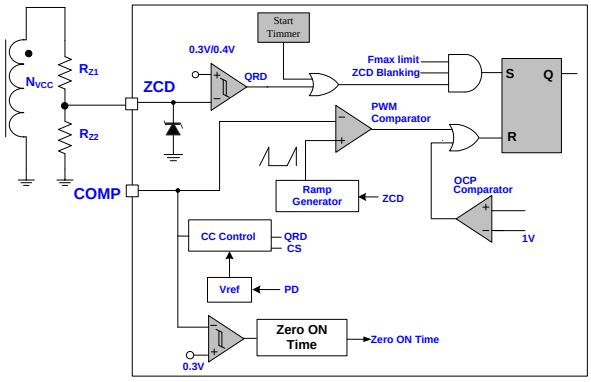


Fig. 14

The 150μs timer generates a MOSFET turn-on signal if the driver output drops to low level for more than 150μs from the falling edge of the driver output. Fig. 15 shows typical ZCD-related waveforms. Since ZCD pin carries some capacitance, it produces some delay to the turn-on time caused from R_{Z1}. During delay time, the junction capacitor of the MOSFET resonates with the primary inductor of the transformer and the drain-source voltage (V_{DS}) decreases accordingly. So, the MOSFET consumes less voltage to turn on and it therefore minimizes the power dissipation.

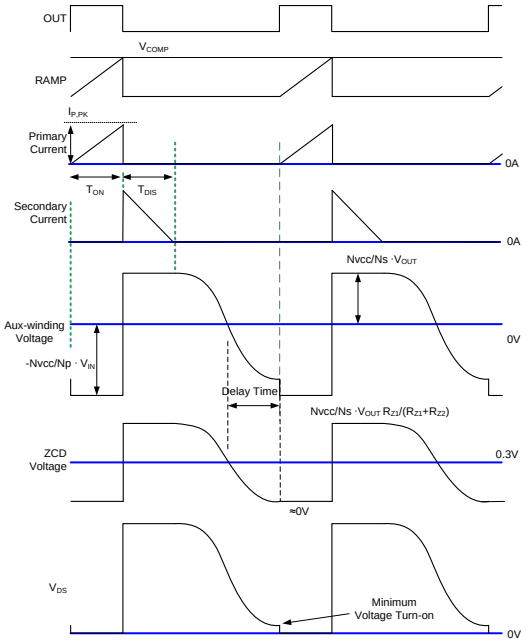


Fig. 15

Principle of C.C. Operation

Primary side control is applied to eliminate secondary feedback circuit or photo-coupler to reduce the circuit cost. The switching waveforms are shown in Fig. 16.

The output current I_O can be expressed as below.

$$Io = \frac{1}{2}\frac{i_{S,PK} \times T_{DIS}}{T_S} = \frac{1}{2}\frac{N_P}{N_S} \times i_{P,PK} \times \frac{T_{DIS}}{Ts} = \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS}}{R_S} \times \frac{T_{DIS}}{T_S}$$

The primary peak current $i_{P,PK}$, inductor current discharge time (T_{DIS}) and switching period (T_S) can be detected by the IC.

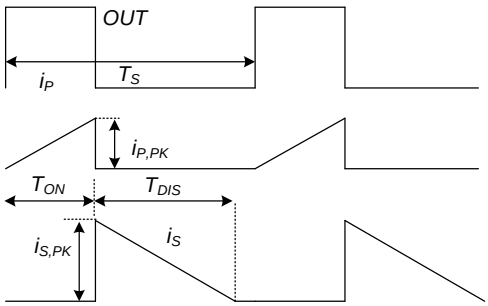


Fig. 16

Output OVP on ZCD

As the LED string circuit opens, the reflected output voltage of aux-winding will cause ZCD voltage increase. If it's above 4V, LD7833 will shut the gate off until the next cycle of Vcc hiccup is tripped, as shown in Fig. 17. The selection of output OVP level is determined according to ZCD divide resistance as the below equation:

$$V_{OVP} \times \frac{N_{VCC}}{N_S} \times \frac{R_{Z2}}{R_{Z1}+R_{Z2}} = 4V$$

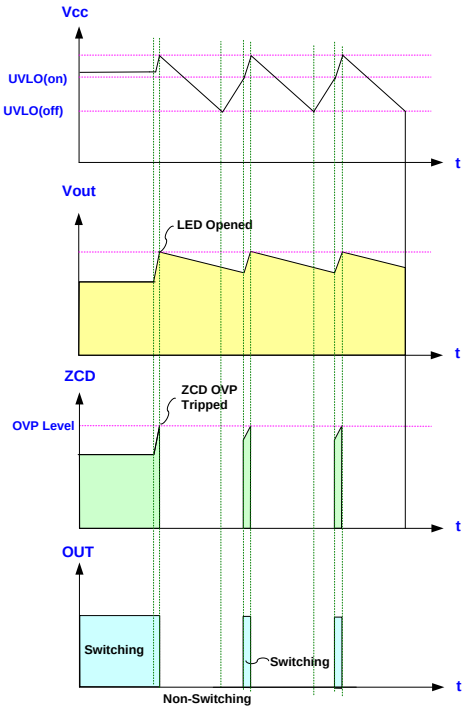


Fig. 17

LED Short Protection (ZCD UVP) – Auto Recovery

To protect the circuit from damage as LED shorts, an auto-recovery type of ZCD UVP protection is implemented for it. Fig. 18 shows the waveforms of the ZCD UVP operation. As LED shorts, the reflected output voltage of aux-winding will cause ZCD voltage decrease. If it's below 0.5V for over the delay time of ZCD UVP, the protection will be activated to turn off the gate until the 4th cycle of Vcc hiccup is tripped. The ZCD UVP delay time is to prevent the false-triggering.

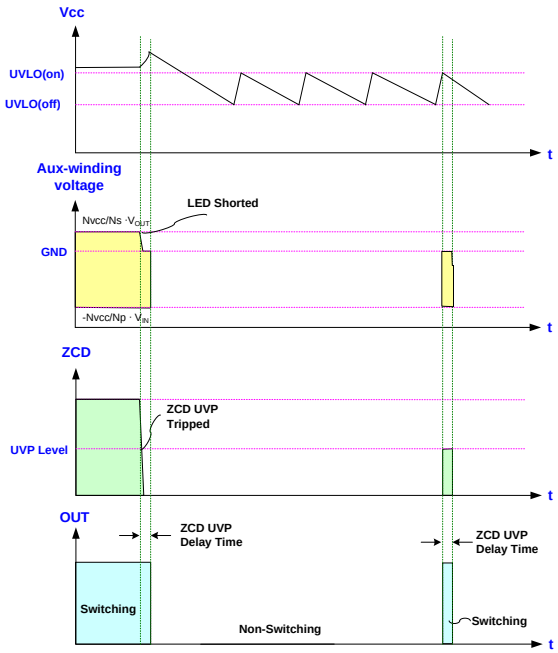


Fig. 18

OVP (Over Voltage Protection) on VCC

The maximum rating of the VCC pin is limited below 28V. To protect VCC from damage due to fault condition, the LD7833 is implemented with OVP function on VCC pin. As soon as the VCC voltage is over OVP threshold (28V), the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(on) arrives. The VCC OVP function of the LD7833 is an auto-recovery protection. The Fig. 19 shows its operation. Upon

removal of the OVP condition will resume the VCC level and the output operation.

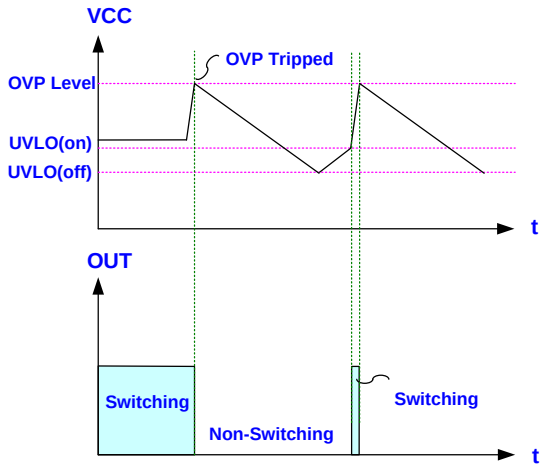


Fig. 19

Output Drive Stage

An output stage of a CMOS buffer with typical 250mA/-500mA driving capability is incorporated to drive a power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage is larger than 13V.

Current Sensing and Leading-edge Blanking

The LD7833 detects the primary MOSFET current over CS pin for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 1V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{Vcs}{Rs} = \frac{0.97}{Rs}$$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike.

Fault Protection

There are several critical protections integrated in the LD7833 to protect the power supply from being damaged. Those damages usually come from open or short condition on the pins of LD7833.

Under the conditions listed below, the gate output will turn off immediately to protect the power circuit ---

1. Comp pin shorts and floats
2. ZCD shorts
3. CS floats

TRIAC Dimming Mode

Phase angle detection by HV pin

The HV pin can detects TRIAC phase by main bulk capacitor and get PD signal in compare with V_{DC1} through phase detector as shown in Fig. 20. The PD signal controls OUT status according to the TRIAC phase in high/ low and determines the internal reference for current control.

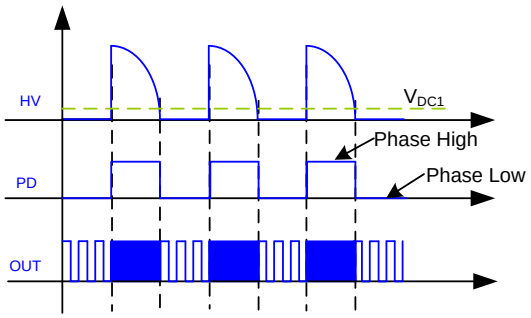


Fig. 20

Programmable Phase Angle Cut-off Function

To prevent shimmering in small conduction angle of TRIAC, the LD7833 provides the function of phase angle cut-off to force the LED load shut off before the shimmer appears.

Fig. 21 shows the operation of the phase angle cut-off function. If HV peak voltage descends to BNO level with TRIAC dimming down, LD7833 will shut the gate off until TRIAC dimming resumes to BNI level.

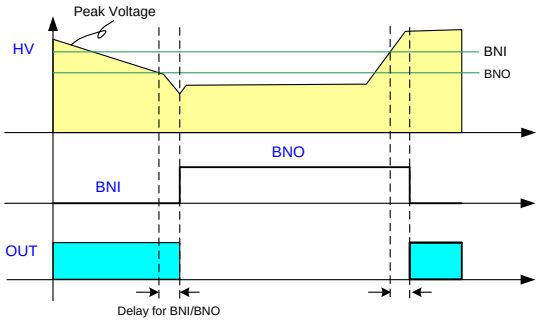
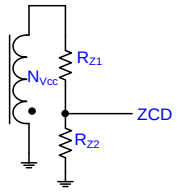


Fig. 21

The phase angle cut-off setting is adjustable with the ZCD resistance, see Fig. 22. The ZCD resistance can be obtained from below equation.



$$R_{ZCD} = \frac{R_{Z1} \cdot R_{Z2}}{R_{Z1} + R_{Z2}}$$

Fig. 22

The following table is a suggestion for phase angle cut-off setting. The cut phase angle corresponds to the threshold of BNI/ BNO.

R_{ZCD}	Input	BNI/BNO	Suggestion	V_{DC2}
55.1k<R_{ZCD}<60.5k	220VAC	200/255	58k	20V
38k<R_{ZCD}<42k		131/200	40k	20V
25.65k<R_{ZCD}<28.35k	220VAC	Disable	27k	
17.1k<R_{ZCD}<18.9k	110VAC	100/128	18k	10V
9.5k<R_{ZCD}<10.5k		66/100	10k	
R_{ZCD}<6.3k	110VAC	Disable	6k	

The following table is a suggestion for phase angle cut-off setting. The cut phase angle corresponds to the threshold of BNI/ BNO. In General, suggest to select BNI/ BNO disable setting.

Damping Circuit

It's necessary to build a Damping circuit in TRIAC dimming application as shown in Fig. 23. A proper selection of capacitance of C_D can provide enough holding current to maintain TRIAC in turn-on mode. R_D is a damper for mitigating the large oscillation of the input current. If the damper is not enough, the induced ringing input current will fall below the holding current threshold to turn off TRIAC immediately as shown in Fig. 24. That's why it causes LED flicker.

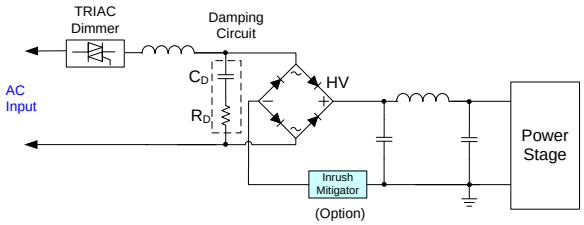


Fig. 23

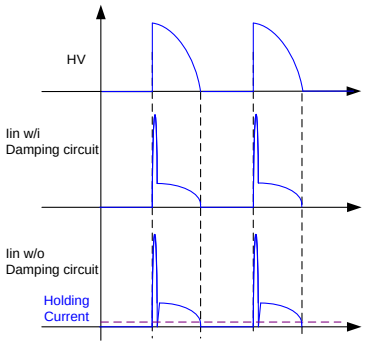
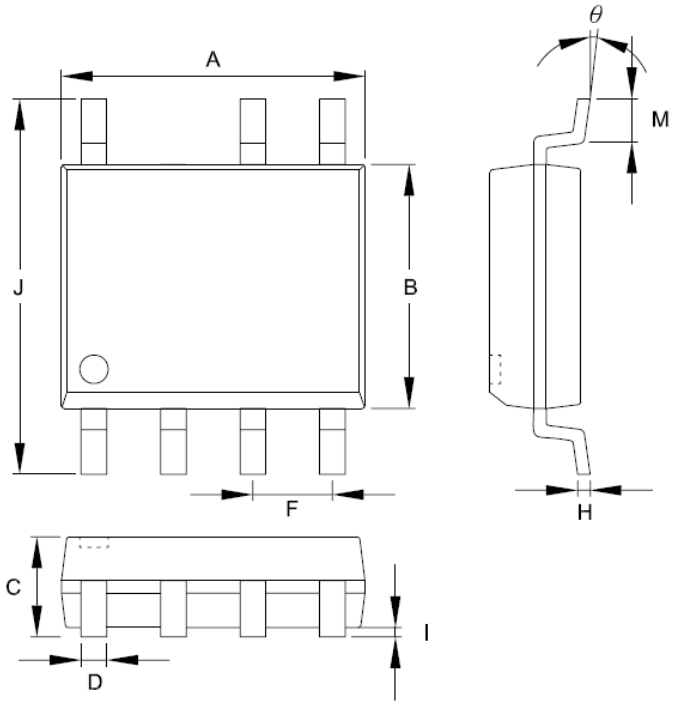


Fig. 24

Package Information

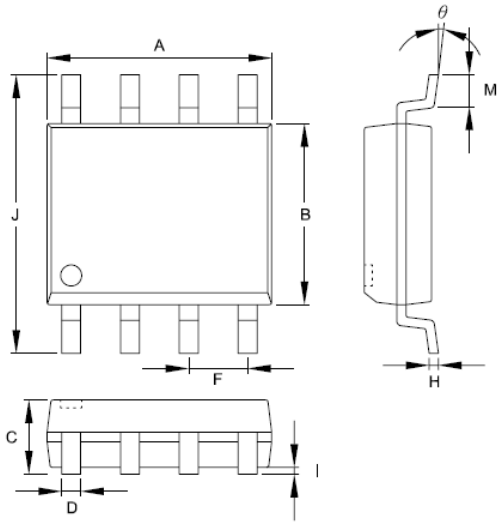
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
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J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	12/23/2016	Original Specification