Non-isolation Buck Solution

High Power Factor LED Controller

REV: 01

General Description

The LD7835 is a floating switch buck solution with Active PFC (APFC) control for LED lighting. It is easy to design with minimum cost and PCB size. The device operates in transition mode (TM) and integrates with complete safety requirement protections.

With power factor correction and TM control, the system is enabled to achieve high PF and high efficiency and to meet most of the international standard.

The LD7835 also features LED open protection (ZCD OVP), LED short protection, over current protection (OCP), and over temperature protection (OTP). It makes the circuit designers easily to meet most of the safety requirements in either normal or abnormal test.

Features

- High Power Factor Controller Integrated
- High Efficiency Transition Mode Operation
- Good Accurate Current Regulation
- Current Ripple Reduction (CRR) Function
- Wide Range of UVLO
- Built in OVP on VCC pin
- LED Open Protection
- LED Short Protection
- OCP (Cycle by cycle current limit)
- OTP (Over Temperature Protection)
- 250mA/-250mA Driving Capability

Applications

- LED Lamp、LED bulb Application

Typical Application

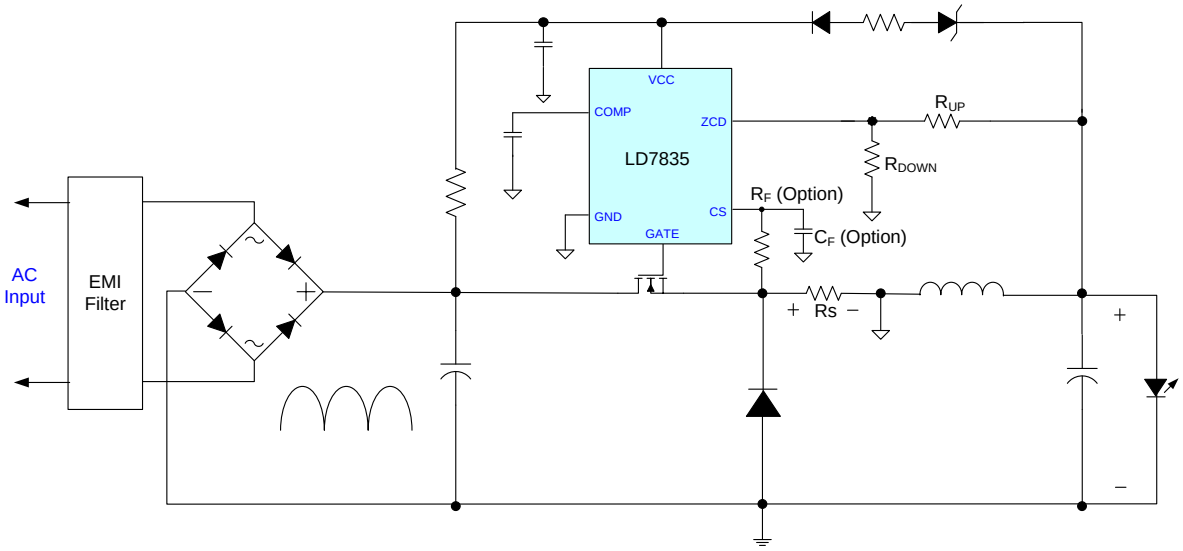
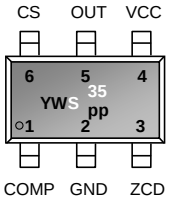


Fig. 1 Application circuit

Pin Configuration

SOT-26 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005…..)
WW, W : Week code
PP : Production code
S35 : LD7835

Ordering Information

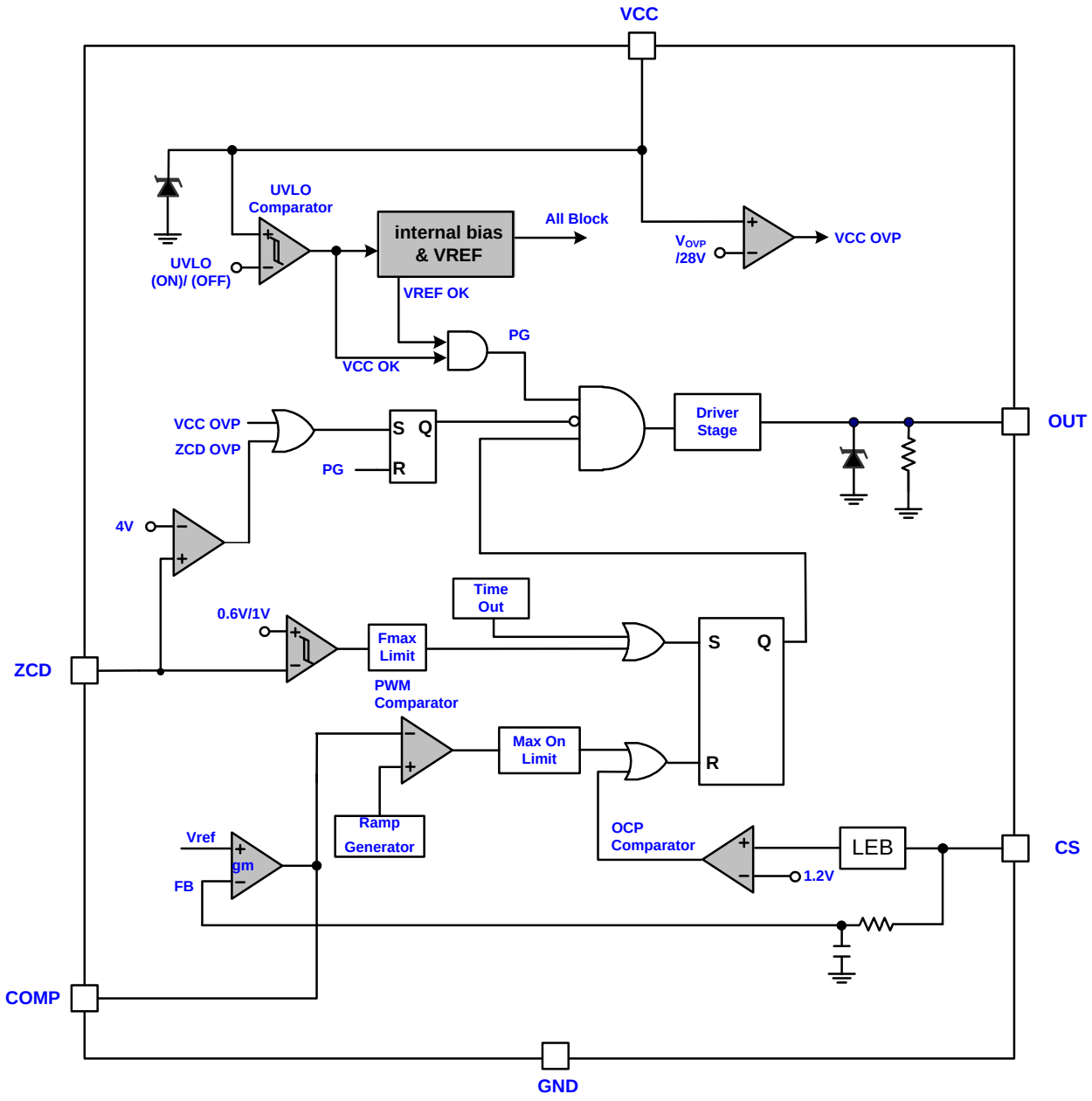
Part number	Package	Top Mark	Shipping
LD7835 GL	SOT-26	YWS/35	3000 /tape & reel

The LD7835 is ROHS compliant/ green packaged.

Pin Descriptions

Pin	NAME	FUNCTION
1	COMP	Compensation pin for internal error amplifier
2	GND	Ground
3	ZCD	Over voltage protection setting, Quasi resonance detector, support programmable maximum on-time.
4	VCC	Power Supply to VCC
5	OUT	Gate Signal Output
6	CS	Connecting a sense resistor to ground, support CRR function setting.

Block Diagram



Absolute Maximum Ratings

VCC	-0.3V ~ 30V
CS	-1V ~ 6V
ZCD	-0.3V ~ 6V
COMP	-0.3V ~ 6V
ZCD Source/ Sink Current	-2mA ~ 1mA
OUT	-0.3V ~ 30V
Operating Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	200°C/W
Power Dissipation (SOT-26, T_J=125°C, T_A=85°C)	200mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
VCC	13	24	V
VCC pin capacitor	4.7	22	μF
COMP	0.8	5	V
COMP pin capacitor	0.47	2.2	μF
Operating Junction Temperature Range	-20	125	°C

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(VCC =14.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	Symbol	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current	VCC=10V	I_{VCC_ST}	-	-	10	μA
Operating Current (with 1nF load on OUT pin)	COMP=3V, ZCD=2V	I_{VCC_14}	-	1	-	mA
	Protection Tripped (OVP, OTP)	I_{VCC_PRO}	-	2	-	mA
UVLO (OFF)		V_{UV_OFF}	7.7	8.2	8.7	V
UVLO (ON)		V_{UV_ON}	15	16	17	V
VCC OVP Threshold		V_{CC_OVP}	27	28	29	V
Compensation(COMP Pin)						
gm(1)		-	-	200	-	μA/V
COMP Pin Open Voltage		V_{CMP}	5	5.5	6	V
Programmable Max-On Time	Level 1, COMP =5V	T_{ON_MAX1}	-	15	-	μs
	Level 2, COMP =5V	T_{ON_MAX2}	-	21	-	μs
	Level 3, COMP =5V	T_{ON_MAX3}	-	29	-	μs
Pre-charge voltage during soft-start(1)		V_{CMP_PRE}	-	0.6	-	V
Current Sensing (CS Pin)						
Reference voltage		V_{ref}	0.194	0.2	0.206	V
OCP Threshold (Cycle by Cycle)		V_{OCP}	1.1	1.2	1.3	V
	During soft-start	V_{OCP_SS}	-	0.45	-	V
Soft-Start Time		T_{SS}	12	16	20	ms
LEB time		T_{LEB}	-	250	-	ns
Zero Current Detector (ZCD Pin)						
Lower Clamp Voltage		V_{ZCD_LC}	-	0	-	V
ZCD OVP Threshold		V_{ZCD_OVP}	3.8	4	4.2	V
ZCD OVP Comparator De-bounce		T_{DEB_OVP}	-	1.6	-	μs
Input Voltage Threshold		V_{ZCD}	-	0.6	-	V
	Hysteresis	V_{ZCD_HYS}	-	0.4	-	V
ZCD Blanking Time		T_{ZCD_BLK}	1.5	2	2.5	μs
Minimum (ON+OFF)-Time, F_{MAX}						
Minimum ON+OFF-Time	$F_{S,\ MAX}$(150kHz)	T_{MIN}	5.34	6.67	8	μs
	During Soft-Start	T_{MIN_SS}	-	11	-	μs

PARAMETER	CONDITIONS	Symbol	MIN	TYP	MAX	UNITS
Gate Drive Output (OUT Pin)						
Output Low Level	VCC=15V, I_{SINK}=20mA	V_{OUT_L}	-	-	0.5	V
Output High Level	VCC=15V, I_{SOURCE}=5mA	V_{OUT_H}	8	-	VCC	V
Output High Clamp Level	VCC=15V	V_{OUT_CL}	12	13	14	V
Rising Time(1)	VCC=15V, CL=1nF	-	-	120	-	ns
Falling Time(1)	VCC=15V, CL=1nF	-	-	30	-	ns
Time out						
Time out Period during Soft start		T_{OUT_SS}	-	80	-	μs
Time out Period after soft start		T_{OUT}	120	160	200	μs
OTP (Over Temp. Protection)						
OTP Trip level(1)		-	-	140	-	°C
OTP Hysteresis(1)		-	-	30	-	°C

Note: (1) Guaranteed by Design.

Typical Performance Characteristics

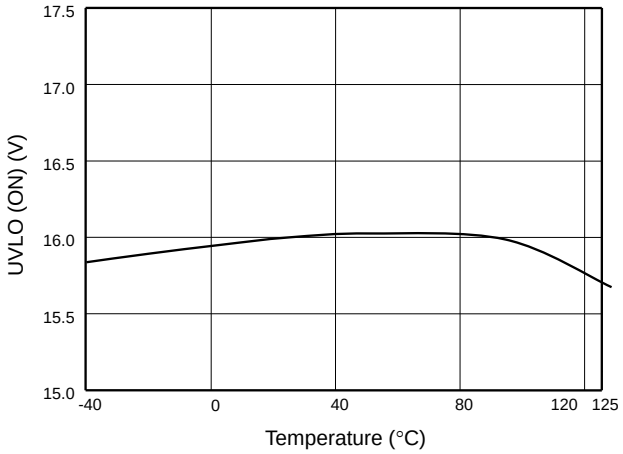


Fig. 2 UVLO (ON) vs. Temperature

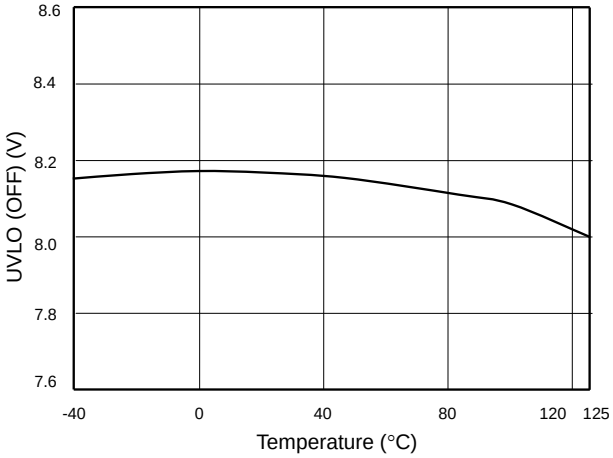


Fig. 3 UVLO (OFF) vs. Temperature

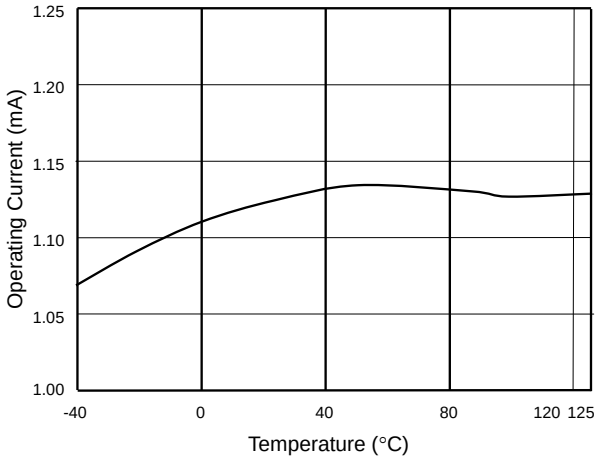


Fig. 4 Operating Current vs. Temperature

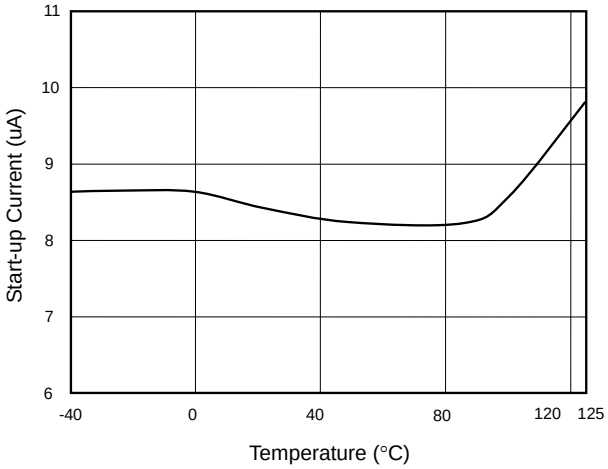


Fig. 5 Start-up Current vs. Temperature

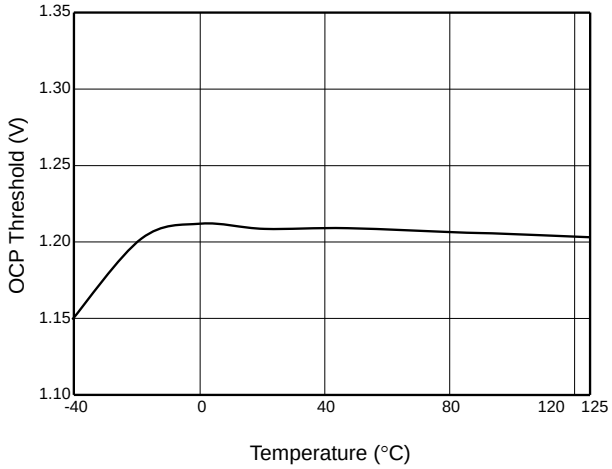


Fig. 6 OCP Threshold vs. Temperature

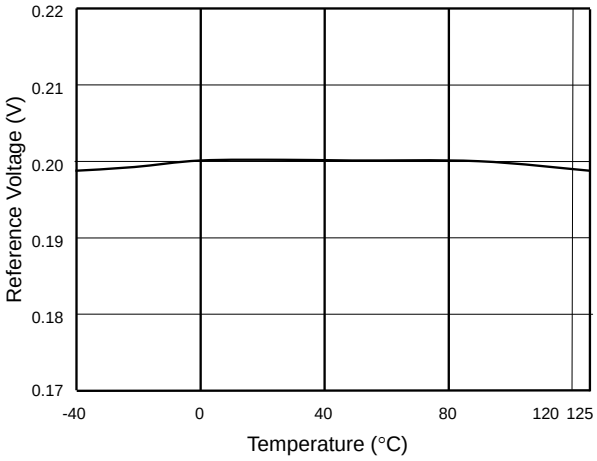


Fig. 7 Reference Voltage vs. Temperature

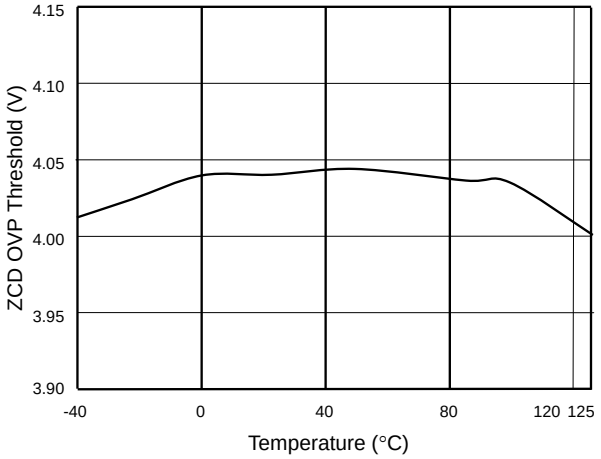


Fig. 8 ZCD OVP Threshold vs. Temperature

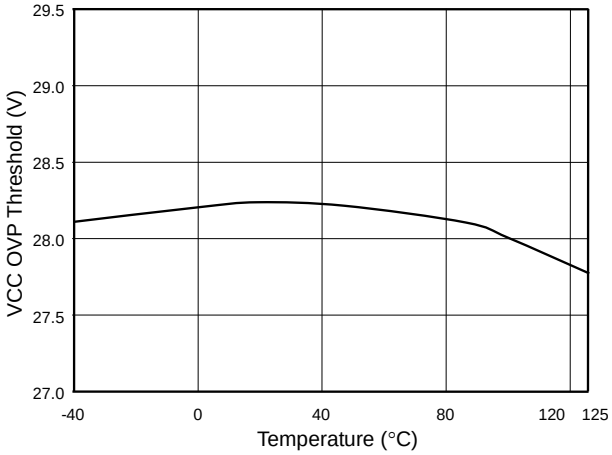


Fig. 9 VCC OVP Threshold vs. Temperature

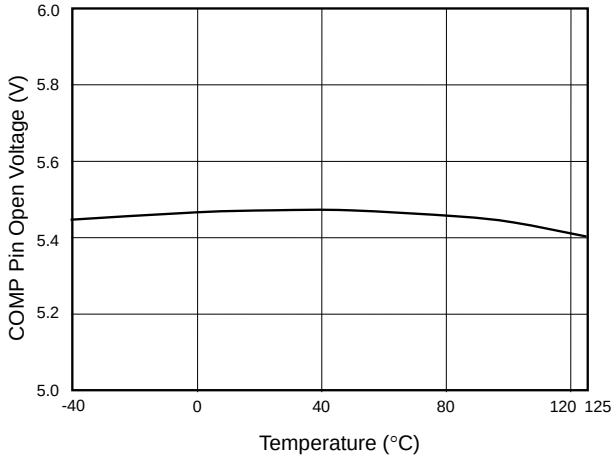


Fig. 10 COMP Pin Open Voltage vs. Temperature

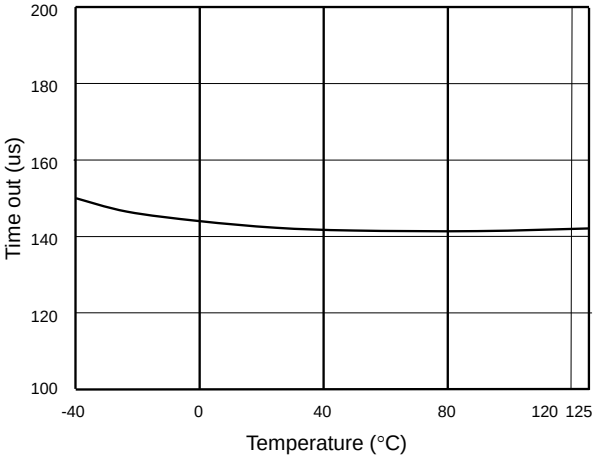


Fig. 11 Time out vs. Temperature

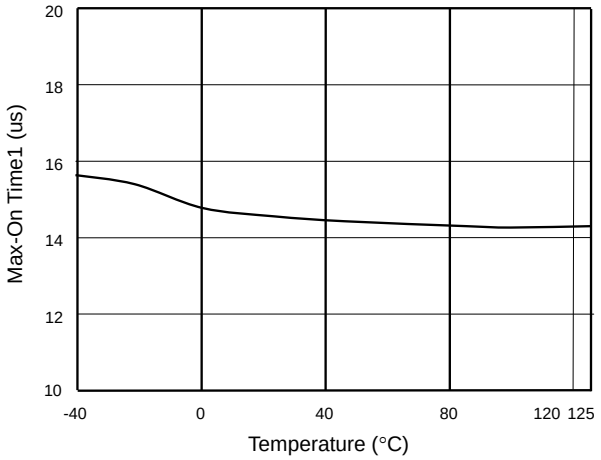


Fig. 12 Max-On Time1(COMP=5V) vs. Temperature

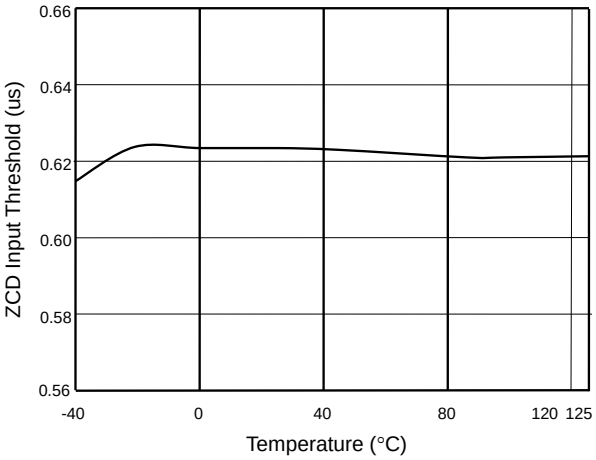


Fig. 13 ZCD Input Threshold vs. Temperature

Application Information

Operation Overview

LD7835 is an LED controller for lighting application. The transition mode (TM) technique meets the requirements for high power factor and high efficiency. It minimizes the external component counts and the PCB size for compact application.

The control mechanism of LD7835 is a voltage-mode operation. The switch turn-on time is fixed while the turn-off time varies in steady state. Therefore, the switch frequency changes in response to the different voltages. The affected frequency reduces EMI noise. LD7835 also features LED open protection, LED short protection, over current protection, and over temperature protection. No extra mains voltage sensing is required as what the traditional current mode PFC controllers behaves for power saving.

Ramp Generator Block, Zero Current Detection (ZCD) and ZCD OVP

Fig. 14 shows typical ramp generator block and ZCD block. The COMP pin voltage and the output of the ramp generator block are compared to determine the MOSFET On-time, as shown in Fig. 15.

The LD7835 features transition mode (TM) operation. The zero current detection block circuit detects the ZCD signal to turn on the MOSFET soon after the voltage across ZCD falls to 0.6V and also the current through the inductor reaches zero. Instead, if there's no signal detected within 160μs, the time-out will generate a signal to turn on MOSFET to ensure the system operate properly.

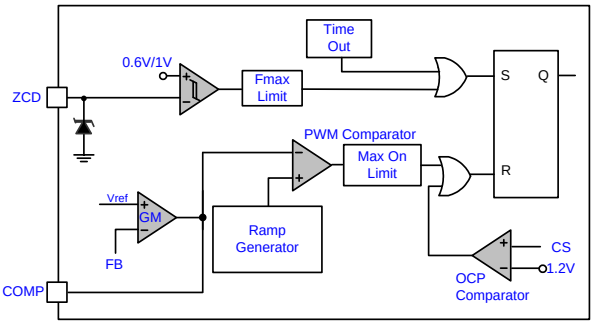


Fig. 14

During the delay time as shown in Fig. 15, the junction capacitor of the MOSFET resonates with the inductor and the drain-source voltage (VDS) decreases accordingly. So, the MOSFET consumes less voltage and the power dissipation will be minimized.

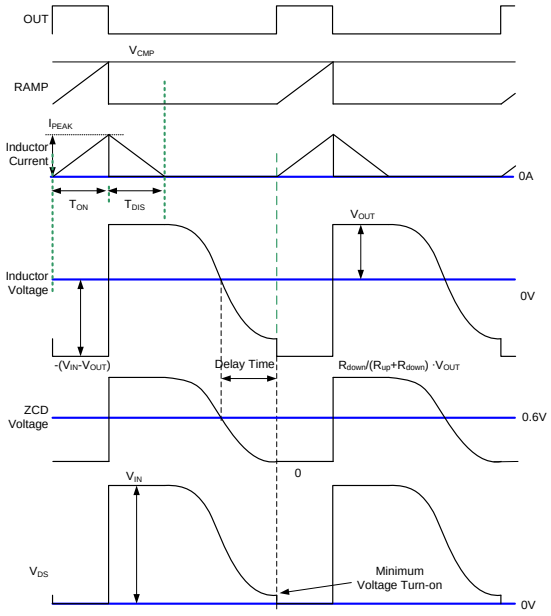


Fig. 15

Fig. 16 illustrates the operation of over voltage protection, where ZCD divider resistors continue to detect the output voltage as the gate switches in off state and return the information to ZCD. If the output voltage increases to trip the threshold, it will signal that there may be some LED(s) open. The LD7835 will

then discharge VCC with a souring current (I_{CC_PRO}) till VCC drops to UVLO (OFF) level. LD7835 will shut down its operation until VCC rises up to next UVLO (ON) level. If the open situation remains still, the system will enter to hiccup mode.

$$V_{ZCD\_OVP} = V_{OVP} \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}}$$

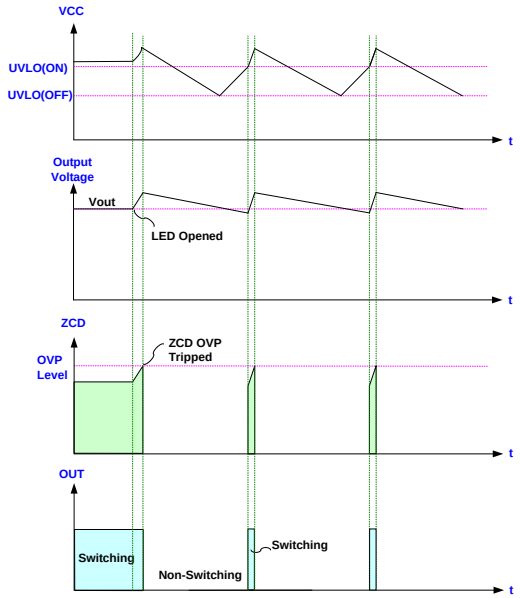
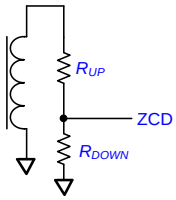


Fig. 16

Programming Maximum ON-time

LD7835 features adjustable maximum ON-time to limit power output in abnormal operation. The selection of maximum ON-time is subject to ZCD resistance as shown in Fig. 17. ZCD resistance can be obtained from below:



$$R_{ZCD} = \frac{R_{UP} \times R_{DOWN}}{R_{UP} + R_{DOWN}}$$

Fig. 17

The following table is a suggestion for maximum ON-time setting.

R_{ZCD} (Ω)	Max. Ton (Typ.)	Suggestion (Ω)
44k<R_{ZCD}	15μs	46k
28k<R_{ZCD}<32k	21μs	30k
R_{ZCD}<20k	29μs	18k

Current Ripple Reduction (C.R.R) Function

LD7835 features current ripple reduction function to minimum the output capacitor. The C.R.R rate is subject to R_F resistance as shown in Fig. 1. The following table is a suggestion for CRR rate setting.

R_F (Ω)	CRR Effective Rate	Suggestion (Ω)
16k<R_F	Heavy	18k
7k<R_F<8k	Light	7.5k
R_F<0.2k	Disable	0

The C.R.R effect is dependent on C.R.R rate, AC line and R_{UP} in fixed output capacitance as shown in the following table for tuning reference.

C.R.R Rate	AC Line	Rup	Current Ripple
Disable	NA	NA	Original
Light	↓	↑	Lightest
Heavy	↑	↓	Heaviest

If C.R.R function is enabled, the output capacitance and the saturation knee point of inductor can be minimize. However, power factor and THD will be slightly lower than disabled condition. It's a trade-off factor between power factor and current ripple.

LED Short Protection

If some LED is in short condition, VCC will drop to UVLO (OFF) level and disable the LD7835. The LD7835 will not resume operation until VCC rises up to next UVLO (ON) level. If the short condition remains still, the system will enter to hiccup mode.

Over Current Protection (OCP)

The LD7835 detects the MOSFET current from the CS pin, which is for the pulse-by-pulse current limit and output current feedback. The maximum voltage threshold of the CS pin is set at 1.2V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK} = \frac{1.2V}{R_S}$$

Over Voltage Protection (VCC OVP)

The maximum rating of the VCC pin is limited below 30V. To prevent VCC from damage due to fault condition, the LD7835 is implemented with OVP function on VCC pin, this value is about 28V. As soon as the VCC voltage is over OVP threshold voltage, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO (ON) arrives. The VCC OVP function of the LD7835 is an auto-recovery protection. The Fig. 18 shows its operation. Upon removal of the OVP condition will resume the VCC level and the output operation

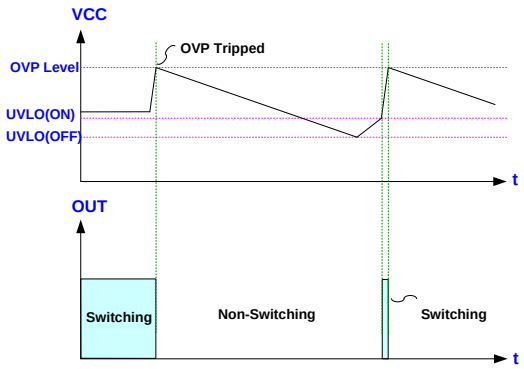


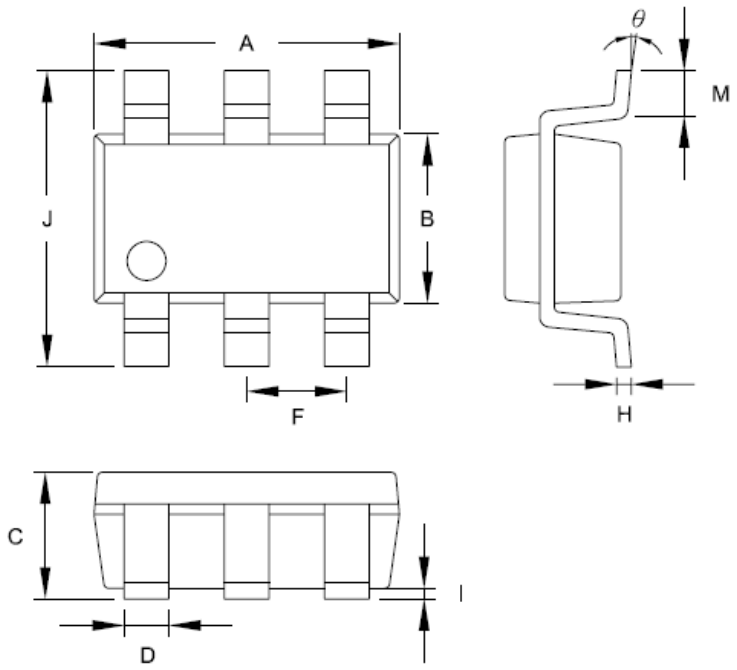
Fig. 18

Output Drive Stage

An output stage of a CMOS buffer, with typical 250mA/-250mA driving capability, is incorporated to drive the power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage rises over 13V.

Package Information

SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	2014/08/28	Original Specification.
01	2015/07/29	Update equation of Fig 17.