High Performance Primary Side Flyback LED Controller with HV Start-up

REV. 00

General Description

The LD7837 is a high performance primary side Flyback or Buck Boost LED Controller with HV start-up special design for LED lighting. This IC operating on transition mode(TM) and integrated with completed safety requirement protections. It minimizes the components counts in a SOP-7 package. Those make it easy design for cost- effective applications.

This chip provides High Current Accuracy at full input voltage range form from 85V to 277V Vac. The constant on time PFC control and THDi compensator could easily achieve PF>0.90 and THDi <10% to meet most of the international standard requirements.

With completed protection built inside this IC, such as over voltage protection (OVP), over current protection (OCP) and short circuit protection (SCP), it enables the circuit to meet most safety requirements in both normal and abnormal test.

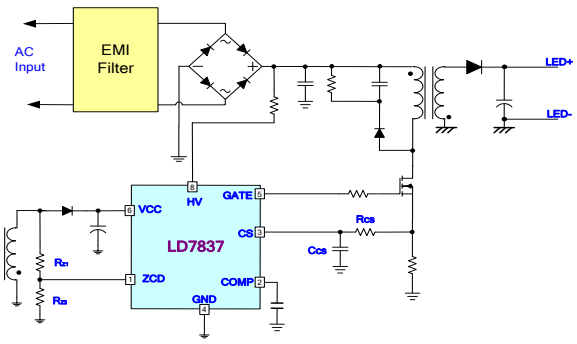
Features

- High voltage 700V startup circuit
- Primary Side PFC controller
- Optimize THDi Over Wide Universal Range
- High LED Current Accuracy
  - Line Regulation ≤ 1%
  - +/-10% output voltage variation Regulation ≤ +/-1%
  - ± 5% Inductance variation ≤ ± 2%
- Power Saving ≤ 0.3W @ No Load V_{AC}=264V
- Output Short Circuit Protection
- CS Short / Open Protection
- 150/-450mA Driving Capability

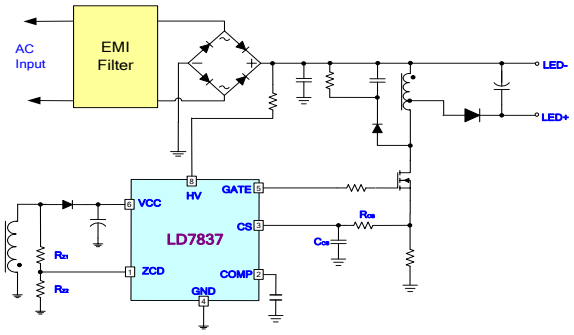
Applications

- LED Power Module
- LED Bulb/Tube lighting

Typical Application



Flyback Topology Design



Buck Boost Topology Design

Pin Configuration

SOP-7

YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package	Top Mark	Shipping
LD7837 GR	SOP-7	LD7837 GR	2500 /tape & reel

The LD7837GR is ROHS compliant/ green packaged.

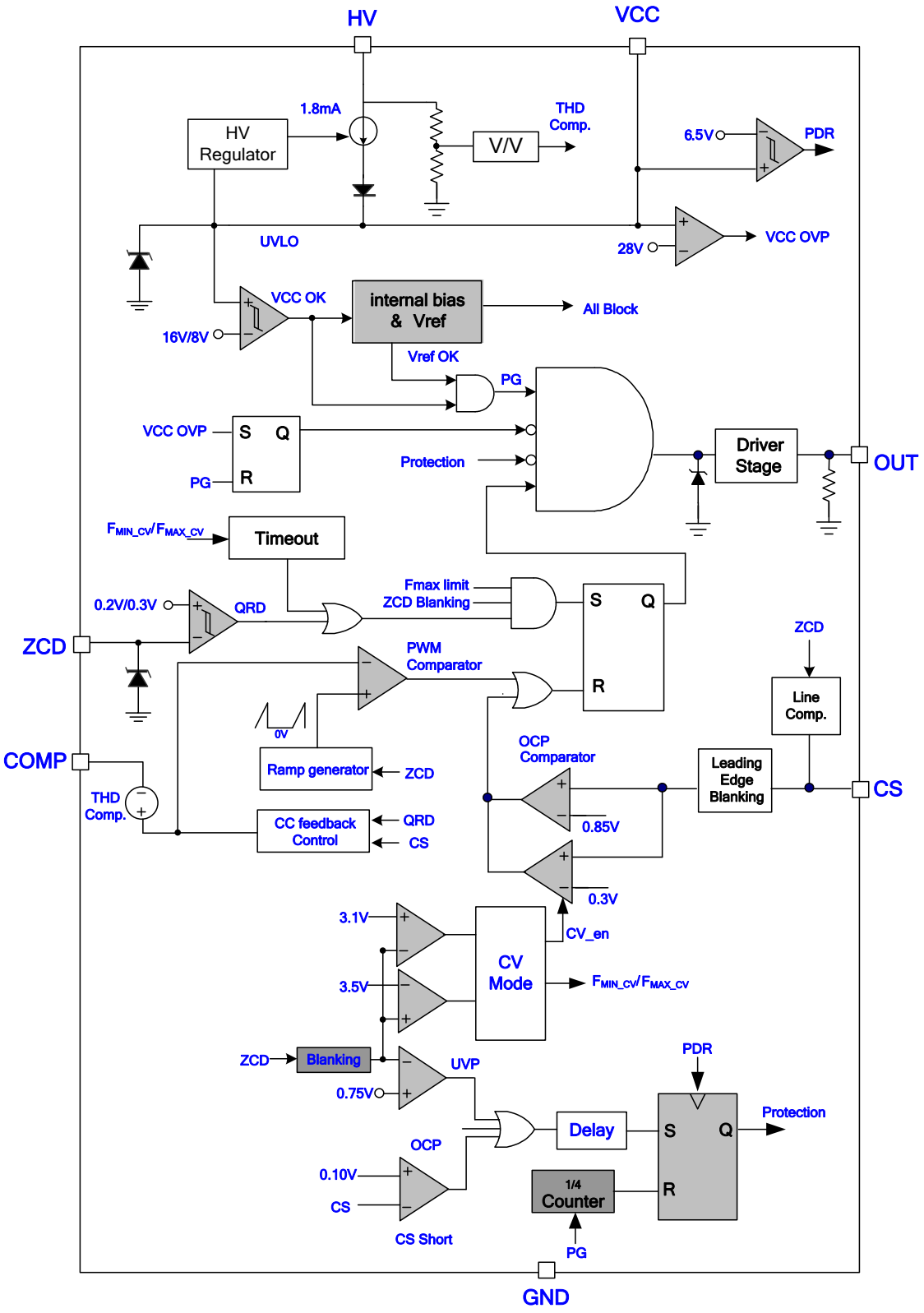
Protection Mode

Part number	VCC_OVP	ZCD_OVP	CS Open/short	OLP/ Output Short	Current Limit-2 Protection
LD7837	Auto recovery	Auto recovery	Auto recovery	Auto recovery	Auto Recovery

Pin Descriptions

Pin	NAME	FUNCTION
1	ZCD	Quasi resonance detector, supports for programmable maximum on-time. This pin receives the auxiliary winding voltage through a resister divider and detects the quasi resonance. It also provides protection for over-voltage output.
2	COMP	Loop compensation pin. Connect a capacitor with it to stabilize the control loop.
3	CS	Current sense pin, connect it to sense the MOSFET current for OCP
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Power source VCC pin
8	HV	Connect this pin to the positive of main bulk cap to provide the startup current for controller.

Block Diagram



Absolute Maximum Ratings

Supply Voltage, VCC	-0.3 ~30V
High voltage pin, HV	-0.3~700V
OUT pin	-0.3 ~VCC +0.3V
COMP, ZCD,CS pin	-0.3 ~6V
ZCD Pin Clamping Current	-1.5mA~100μA
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOP-7, θ_{JA})	160°C/W
Power Dissipation (SOP-7, at Ambient Temperature = 85°C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (Except HV pin)	2.5KV
ESD Voltage Protection, Human Body Model (HV pin)	1 KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply VCC Voltage	9.5	26.5	V
Vcc pin capacitor	4.7	22	μF
HV pin series Resistor	5.1	15	kΩ
CS pin filter capacitor (Ccs)	100	1000	pF
CS pin filter resistor (Rcs)	100	1000	Ω
Operating Junction Temperature	-40	125	°C
Comp pin capacitor for Flyback topology	0.47	2.2	μF
Comp pin capacitor for Buck Boost topology	0.47	1.5	μF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(V_{CC}=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High voltage Supply(HV Pin)						
High-voltage current Source	V_{CC}=12V,HV=180V	I_{HV}	1.5	1.8	2.1	mA
Off-state Leakage current	V_{CC}> V_{UV_ON},HV=500 V_{DC}	I_{HV_OFF}	0		30	μA
Supply Voltage (VCC Pin)						
Startup Current	V_{CC}<UVLO ON	I_{ST}	-	70	90	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V, ZCD=0V	I_{OP_LO}	-	1.05	1.3	mA
	V_{COMP}=3V, ZCD= 2V	I_{OP_HI}	-	1.35	1.8	mA
	V_{CC} OVP	I_{OP_OVP}		0.3	-	mA
	UVP, CS short	I_{OP_UVP}		0.75		mA
UVLO (off)		V_{UV_OFF}	7	8	9	V
UVLO (on)		V_{UV_ON}	15	16	17	V
HV Self Bias (Linear Regulator)		V_{LDO_HVBI}	9	10	11	V
De-Latch Voltage		V_{PDR}	7		8	V
VCC OVP Level		V_{CC_OVP}	27		29	V
CC Integrator (Comp Pin)						
Comp pin clamp Voltage		V_{COMP}	4.3	4.5	4.7	V
Current Sensing (CS Pin)						
Current Limit		V_{OCP}	0.8		0.9	V
Current Limit-2 for Limited Peak Current on MOS	Protection mode is the same as CS pin short circuit (4 times Hiccup)	V_{OCP2}	1.05	1.2	1.35	V
Soft Start Time	*	T_{SS}		8		ms
LEB time	*	T_{LEB}	380		520	ns
CS Input bias current		I_{CS}			1.0	μA
Current Limit-3 for CV Control		V_{OCP3}	0.25	0.29	0.33	V
Ratio of Current Mirror for Line Compensation(K)	I_{ZCD}/I_{CS}=3 at gate on state		-1		+1	%
CS Short Protection		V_{CSSP}	0.05	0.10	0.15	V
CS short Protection Delay Time		T_{CSSP}		40		ms

(V_{CC}=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Zero Current Detector (ZCD Pin)						
Upper Clamp Voltage	I_{DET}=100μA	V_{ZH}	4.4	4.7	4.8	V
Lower Clamp Voltage	$I_{DET=}$-2mA	V_{ZL}	0		-0.3	V
ZCD Voltage Threshold		V_{ZCD}	0.17	0.22	0.27	V
	Hysteresis	ΔV_{ZCD}		0.1		V
ZCD Blanking Time	*	T_{BNK_ZCD}		1.5		μS
UVP Detect Level		V_{UVP_ZCD}	0.65	0.75	0.85	V
UVP Delay Time	*	T_{UVP_ZCD}		48		mS
ZCD OVP Voltage Threshold at CV mode		V_{CV_OVP}	3.0	3.1	3.3	V
CV mode Trigger level at ZCD Voltage		V_{CV_TRI}	3.3	3.5	3.7	V
Minimum Frequency at CV mode	*	F_{MIN_CV}		120		Hz
Maximum Frequency at CV mode	*	F_{MAX_CV}		3.8		kHz
Maximum ON-Time						
Maximum On Time	HV=150V_{DC}	T_{ON_MAX1}	14	15.5	17	μs
	HV=300V_{DC}	T_{ON_MAX2}		6.2		μs
Minimum (ON+OFF)-Time						
Minimum ON+OFF-Time,	$F_{S,MAX}$=300KHz	T_{S_MAX}	2.7	3.33	3.9	μs
	During soft start	T_{S_SS}		10		μs
Gate Drive Output (OUT Pin)						
Output Low Level	I_{SINK}=-20mA	V_{G_LO}	0		0.5	V
Output High Level	I_{SOURCE}=20mA	V_{G_HI}	9.5		15	V
Rising Time	CL=1000pF,*	T_{G_RISE}		250		ns
Falling Time	CL=1000pF,*	T_{G_FALL}		35		ns
Time Out						
Time Out	After Soft Start	T_{OUT1}	120	150	180	μs
	During Soft Start	T_{OUT1_SS}		57.5		μs
Internal OTP (Over Temp. Protection)						
OTP Trip level	*			140		°C
OTP Hysteresis	*			30		°C

Note: (*) Guaranteed by Design.

Typical Performance Characteristics

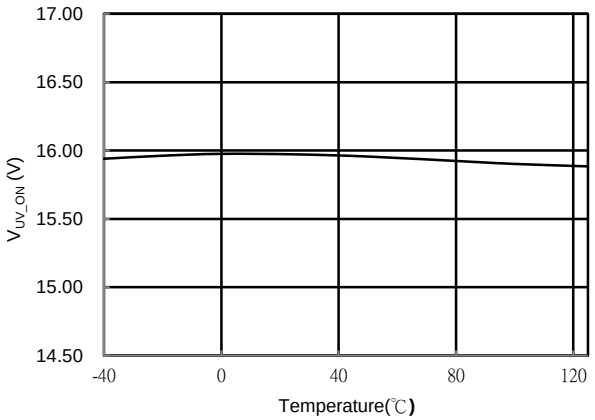


Fig. 1 V_{UV_ON} vs. Temperature

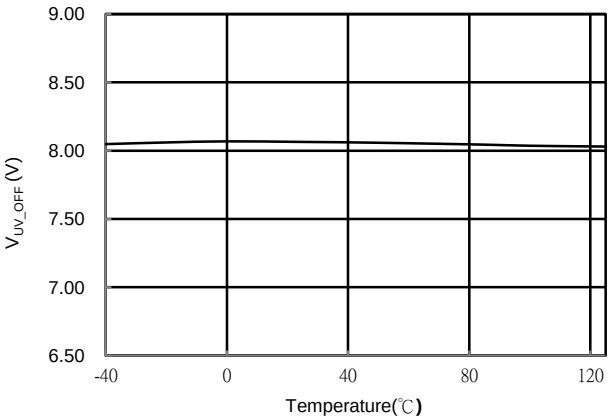


Fig. 2 V_{UV_OFF} vs. Temperature

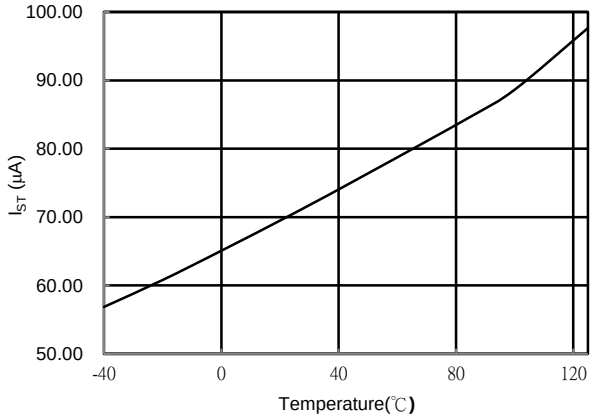


Fig. 3 I_{ST} vs. Temperature

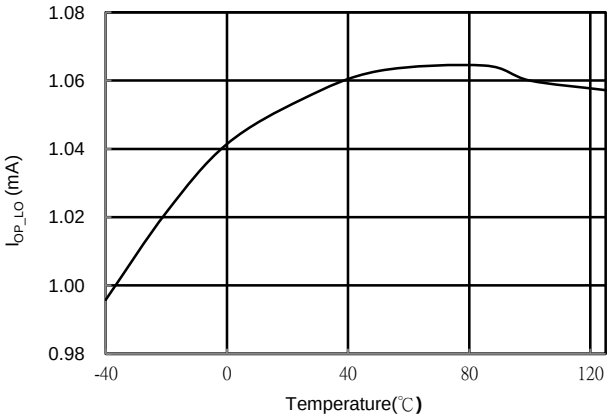


Fig. 4 I_{OP_LO} vs. Temperature

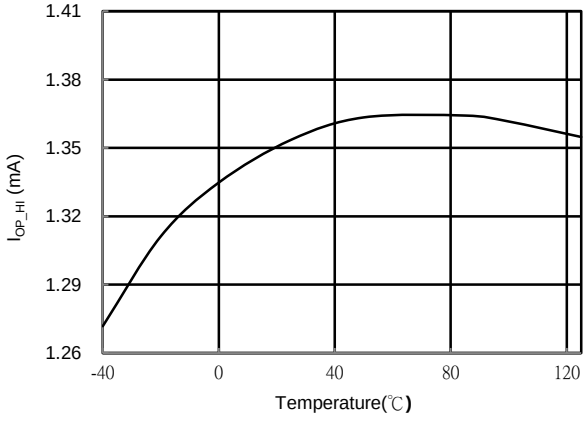


Fig.5 I_{OP_HI}vs. Temperature

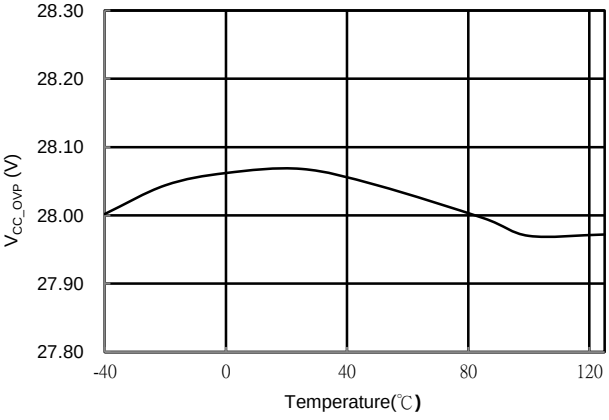


Fig. 6 V_{CC_OVP} vs. Temperature

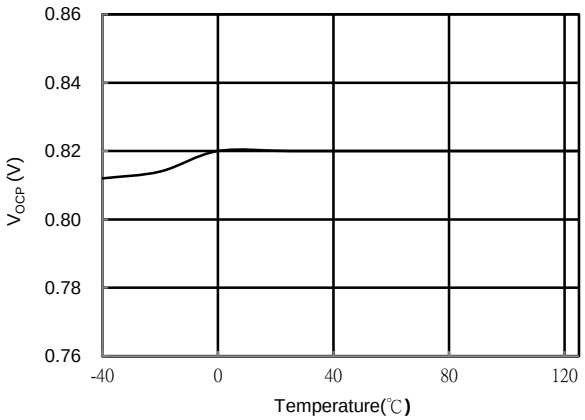


Fig. 7 V_{OCP} vs. Temperature

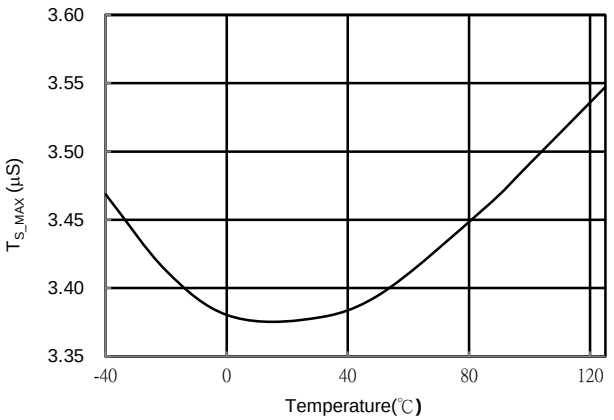


Fig. 8 T_{S_MAX} vs. Temperature

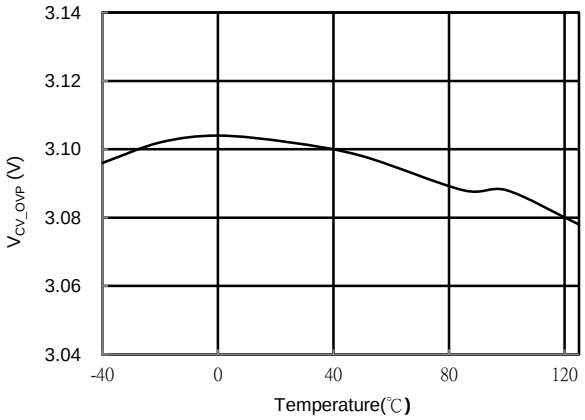


Fig. 9 V_{CV_OVP} vs. Temperature

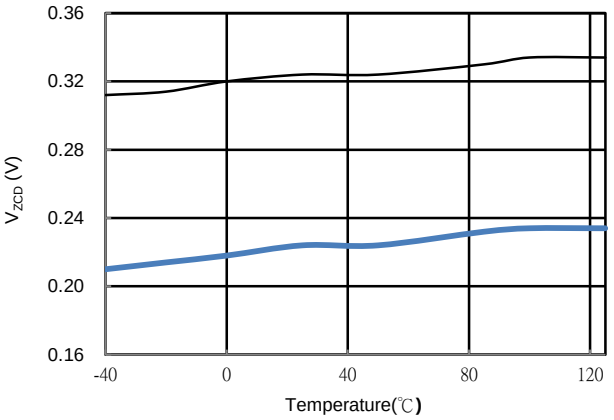


Fig. 10 V_{ZCD} vs. Temperature

Application Information

Operation Overview

The LD7837 is a single-stage Flyback or Buck Boost PFC controller for LED lighting applications. It provides constant current (CC) operation and requires neither photo-coupler nor secondary control circuit. It integrates more functions to reduce the external components counts and the size. Its major features are described as below.

The device operates in the transition mode(TM) and Constant on time in voltage mode control is easily to achieve the high efficiency and high power factor. The internal Current Accuracy and THDi Compensator can meet high performance LED lighting application. And the Constant voltage mode in mode operates for minimum power depletion at no load. The other features output over-voltage protection, output short circuit protection; under voltage lockout and LEB of the current sensing stabilize system operation and protect external components.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes significant power to meet the power saving requirement. In most cases, startup resistors carry large resistance. And, a larger resistor will spend more time to start up.

To achieve optimized topology, as shown in Fig. 11 and Fig. 12, LD7837 is implemented with a high-voltage startup circuit to enhance it. During startup, a high-voltage current source sinks current from the full-bridge rectifier to provide the startup current and charge VCC capacitor C1 at the same time. On condition of VCC below UVLO(ON), the charge current will increases to 1.8mA once V_{CC} rises above UVLO(ON) voltage threshold during start up. Meanwhile, the VCC supply current kept at low level of 70μA that most of the HV current is reserved to charge the Vcc capacitor. By using such configuration, the turn-on delay time will be almost same no matter under low-line or high-line conditions.

The LD7837 will be soon turned on as the VCC's voltage rises over UVLO(ON). It will also drive the high voltage start-up circuit to operate as a regulator and maintain the VCC voltage at UVLO(ON) level. The current consumed is 3mA max. After 50ms of UVLO(ON), the high voltage regulator will be turn on again when VCC less than 9.5V to reduce the power loss. In order to supply sufficient VCC voltage in normal condition, it required auxiliary voltage source to operate. The high voltage regulator will protect the controller from shut off at load transient when VCC voltage drops below UVLO-off. HV regulator will soon be disabled as the IC enter protection mode, as SCP, OVP, OTP, CS short protection…etc.

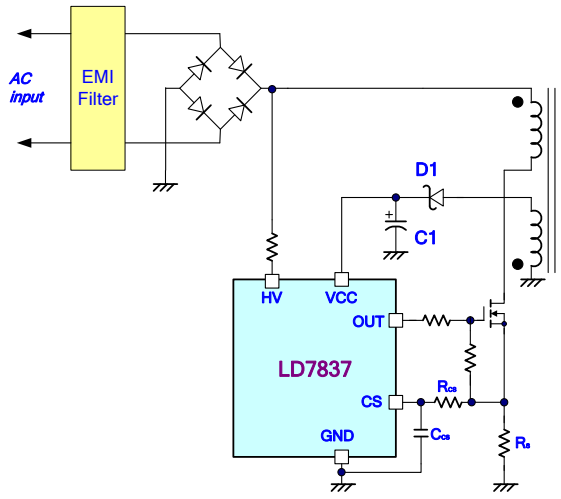


Fig. 11

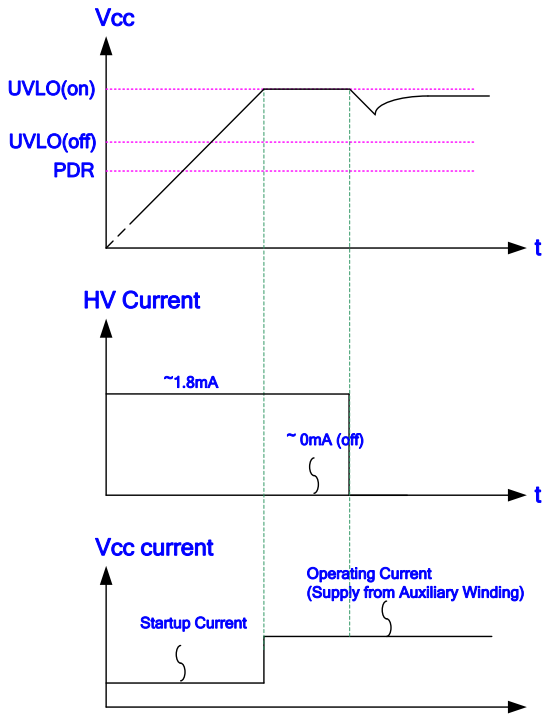


Fig. 12

Ramp Generator Block and Zero Current Detection (ZCD)

Fig. 13 shows typical ramp generator block and ZCD block. The comp pin voltage and the output of the ramp generator block are compared to determine the MOSFET ON-time, as shown in Fig. 14.

The Zero Current Detection block will detect auxiliary winding signal to drive MOSFET as ZCD pin voltage drops to 0.3V. As ZCD pin voltage drop to 0.3V, the current through the transformer is below zero. This feature enables transition-mode operation. The ZCD comparator would not operate if ZCD pin voltage remains at above 0.4V. Once it drops below 0.3V, the zero current detector will act to turn on the MOSFET.

The minimum frequency timer generates a MOSFET turn-on signal if the driver output drops to low level for more than 150μs from the falling edge of the driver output. Fig. 14 shows typical ZCD-related waveforms.

Since ZCD pin carries some capacitance, it produces some delay to the turn-on time caused from Rz1. During delay time, the junction capacitor of the MOSFET resonates with the primary inductor of the transformer and the drain-source voltage (V_{DS}) decreases accordingly. So, the MOSFET consumes less voltage to turn on and it therefore minimizes the power dissipation.

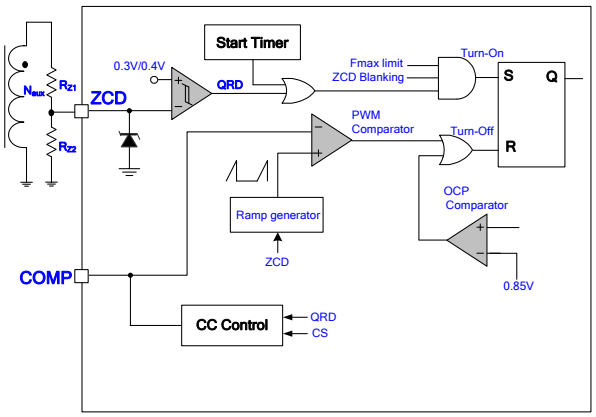


Fig. 13

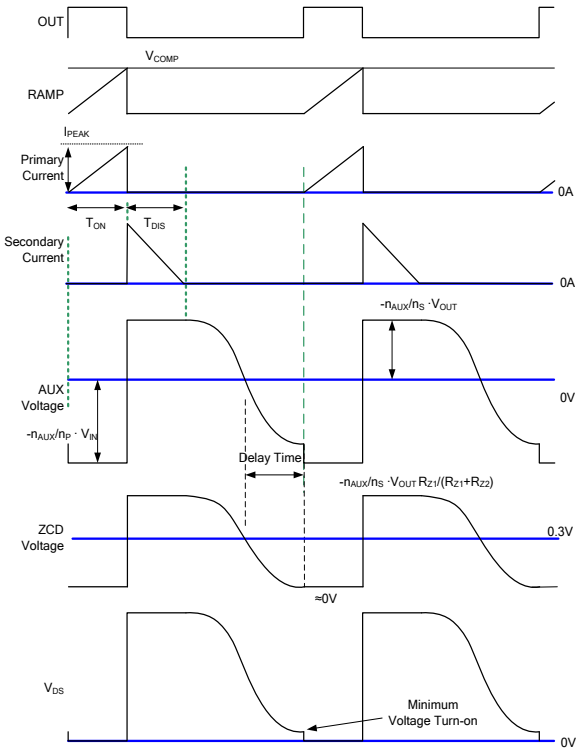


Fig. 14

Output Drive Stage

An output stage of a CMOS buffer, with typical 150mA/-500mA driving capability, is incorporated to drive a power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage is higher than 13V.

Principle of C.C. Operation

Primary side control is applied to eliminate secondary feedback circuit or opto-coupler to reduce the circuit cost. The switching waveforms are shown in Fig.15.

The output current Io can be expressed as:

$$Io = \frac{1}{2}\frac{i_{S,PK} \times T_{DIS}}{T_S}$$
$$= \frac{1}{2}\frac{N_P}{N_S} \times i_{P,PK} \times \frac{T_{DIS}}{Ts}$$
$$= \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS}}{R_S} \times \frac{T_{DIS}}{T_S}$$

The primary peak current $I_{P,PK}$, inductor current discharge time (T_{DIS}) and switching period (T_S) can be detected by the IC. The ratio of V_{CS}*T_{DIS}/T_S will be modulated as a constant. I_O can be induced finally by

$$Io \cong \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS}}{R_S} \times \frac{T_{DIS}}{T_S}$$
$$\sim \frac{1}{2}\frac{N_P}{N_S} \times \frac{0.5}{R_S} \times (1-k)$$
$$\sim \frac{1}{2}\frac{N_P}{N_S} \times \frac{1}{R_S} \times (1/6)$$

Where k = (Ton/Ts) = (1- Tdis/Ts) measured at Vcs =0.5V

So, I_O can be programed by NP/NS and RS easily

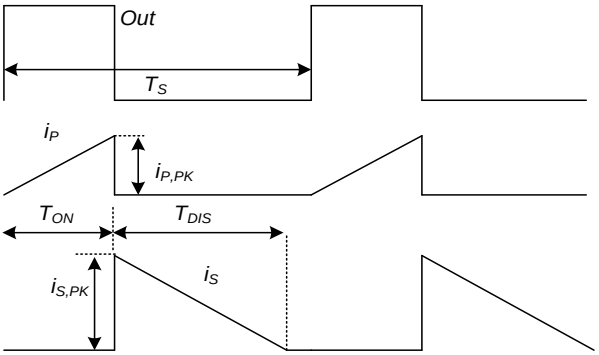


Fig. 15

CS Short Protection (CSSP) – Auto Recovery

In order to prevent the LED driver from damage due to the shorted sense resistor (R_S), CS pin is built in with CS short protection. See Fig. 16 for it. Once the fault occurs, after 1/3 times of max on time (depend on COMP pin level) and the CS voltage will drop to GND, it would enable this protection to avoid seriousness power device damage.

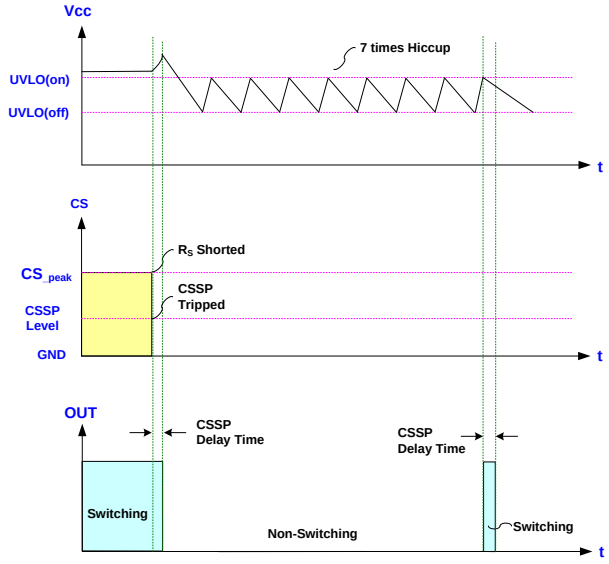


Fig. 16

Output OVP on ZCD

When the LED string open circuit occurs, the reflected output voltage of aux winding will cause ZCD voltage up.

If the ZCD voltage runs up to 3.5V, LD7837 will enforce constant voltage mode and operation at lower frequency to achieve power saving at no load ,as shown in Fig. 17. The LD7837 constant voltage level is 3.1V at ZCD pin. If the ZCD Voltage over the 3.1V, the OUT Pin switching frequency is 125Hz.Otherwise, the switching works at 4KHz. The selection of output OVP level is subject to ZCD divide resistance as the below equation:

$$V_{OVP} \times \frac{N_{VCC}}{N_S} \times \frac{R_{Z2}}{R_{Z1}+R_{Z2}} = 3.1V$$

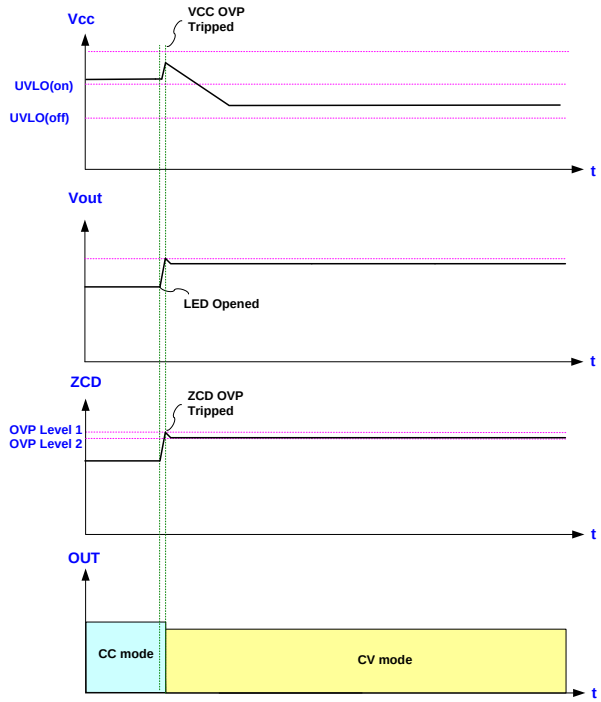


Fig. 17

ZCD under Voltage Protection– Auto Recovery

To protect the circuit from damage due to LED short, an auto-recovery type of ZCD UVP protection is implemented for it. Fig. 18 shows the waveforms of the ZCD UVP operation. In LED short condition, the reflected output voltage of AUX winding will cause ZCD voltage drop. If the ZCD voltage declines below 0.5V for over the delay time of ZCD UVP, the protection will be activated to turn off the gate until the 4th cycle of Vcc hiccup is tripped. The ZCD UVP delay time is to prevent the false-triggering.

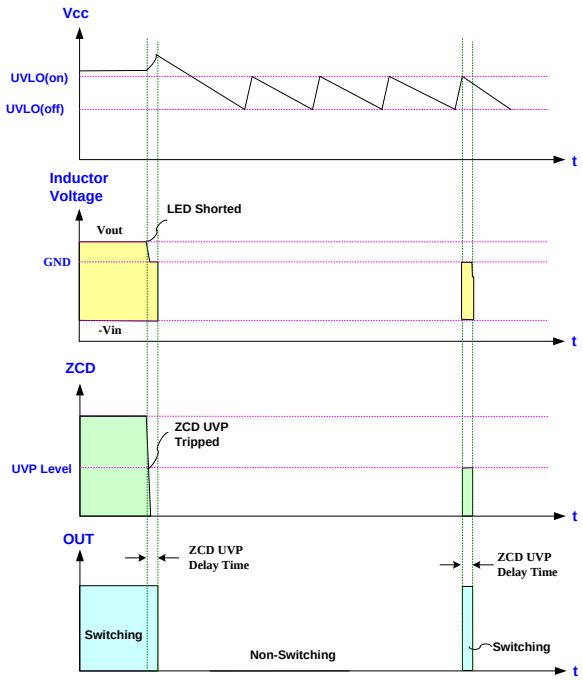


Fig. 18.

Current Sensing and Leading-edge Blanking

The LD7837 detects the primary MOSFET current over CS pin for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.8V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85 - (I_{OCP} \times R_{CS})}{R_S}$$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike.

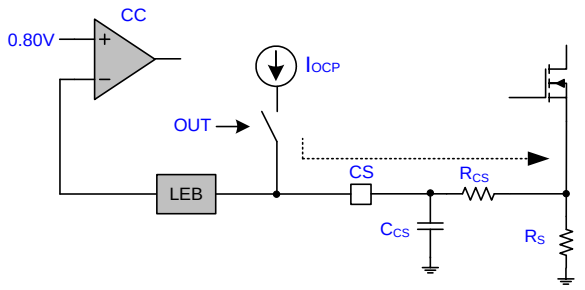
Line Regulation Compensation

In general, the power converter can deliver more current at high input voltage than at low input voltage. So that

cause constant current variation .To compensate this, an offset voltage is added to the CS signal by an internal current source (I_{CS}) and an external resistor (R_{CS}) in series between the sense resistor (Rs) and the CS pin, as shown in Fig. 19. By selecting a proper value of the resistor in series with the CS pin, the amount of compensation can be adjusted. The value of I_{CS} depends on output current of ZCD pin at OUT pin is high. The equation of I_{OCP} is decreased as:

$$I_{OCP} = K \times I_{ZCD}$$

Where I_{ZCD} is about V_{AUX}./ R_{Z1}, and V_{AUX}=Vin X (N_{VCC}/N_P). and Ratio of Current Mirror for Line Compensation , K=1/3



Suggestion design R_{CS}:100Ω~1.0kΩ; C_{CS}:100pF~1000pF

Fig. 19

OVP (Over Voltage Protection) on Vcc

The maximum rating of the VCC pin is limited below 29V. To prevent VCC from the fault condition, the LD7837 is implemented with OVP function on Vcc pin. As soon as the VCC voltage is over OVP threshold voltage (28V), the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(on). The Vcc OVP function of the LD7837 is an auto-recovery protection. The Fig. 20 shows its operation. Upon removal of the OVP condition will resume the Vcc level and the output operation.

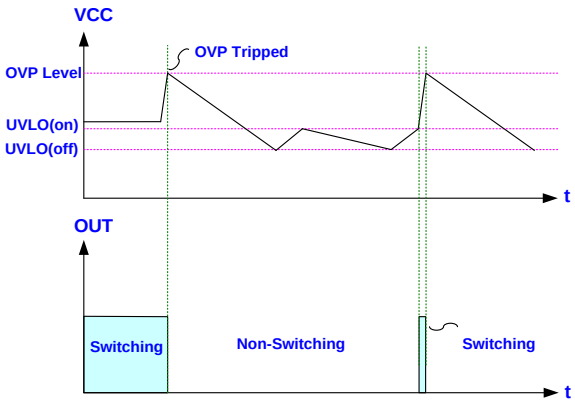
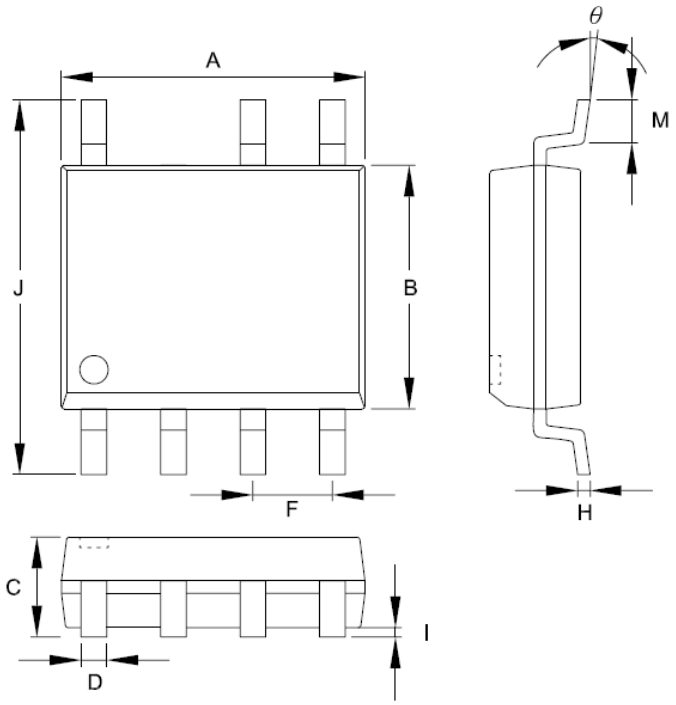


Fig. 20

Package Information

SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	04/06/2017	Original Specification.