High Power Factor Flyback LED Controller with HV Start-up

REV. 00

General Description

The LD7838H is a 700V HV start-up flyback PFC controller, specially designed for LED lighting. This device operates in transition mode(TM) and integrates with completed protections required. It minimizes the components counts in either SOP-7 package. Those make it easy to design with for cost-effective applications.

With HV start-up technology, high power factor and TM control, the start-up time and resistor loss could be minimized efficiently. The circuit can easily achieve PF>0.90 to meet most of the international standard requirements.

With completed protection built inside this IC, such as over voltage protection (OVP), over current protection (OCP), over load protection (OLP), over temperature protection (OTP), and output short circuit protection (OSCP), It enable the circuit to meet most safety requirements in both normal and abnormal test.

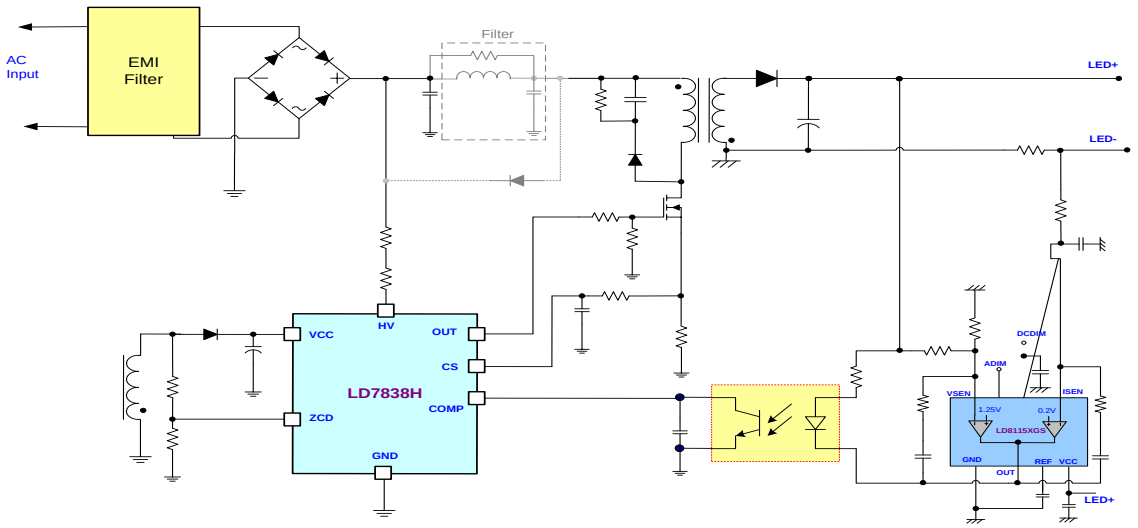
Features

- High voltage (700V) startup circuit for 305VAC
- High Power Factor Flyback PFC controller
- High-efficiency Transition mode operation
- Low Operation Current and Fast start up
- Accurate OLP Compensation for High/ Low Line
- BNI/ BNO Detection Function by HV pin
- Wide UVLO (16.5 Von and 8 Voff) Range
- Cycle by Cycle Current Limiting for Over Current Protection
- OVP (Over Voltage Protection) Function by ZCD and VCC pin
- Internal OTP function

Applications

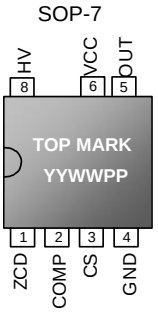
- LED Power Supply
- LED Light Bulb/Tube

Typical Application



Constant current and voltage output application

Pin Configuration



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package	Top Mark	Shipping
LD7838HGR	SOP-7	LD7838H GR	2500 /tape & reel

The LD7838HGR is ROHS compliant/ green packaged.

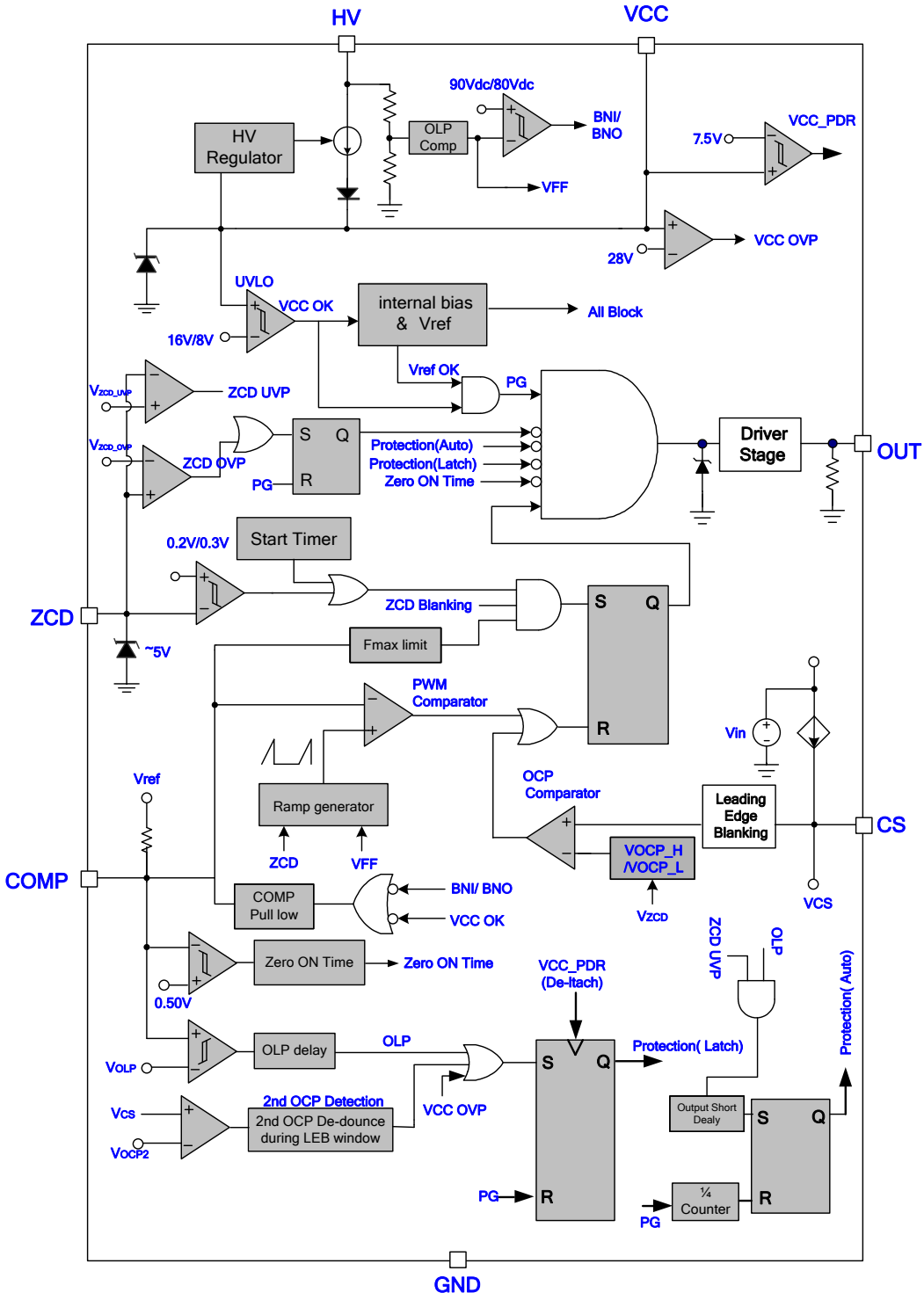
Protection Mode

Part number	BNI/BNO	VCC OVP	ZCD OVP	OLP	Output Short
LD7838H	Yes	Latch	Auto(1st time Hiccup)	Latch	Auto(4th times Hiccup)

Pin Descriptions

Pin	NAME	FUNCTION
1	ZCD	Quasi resonance detector and programmable maximum ON-time.
2	COMP	Feedback pin. Connect a photo-coupler to close the control loop to achieve regulation.
3	CS	Current sense pin, connect it to sense the MOSFET current for OCP.
4	GND	Ground.
5	OUT	Gate drive output to drive the external MOSFET.
6	VCC	Power source VCC pin.
8	HV	Connect this pin to positive terminal of main bulk cap to provide the startup current for controller. When Vcc is UVLO on, the HV loop will open and turn off internal current source to minimize the power loss.

Block Diagram



Absolute Maximum Ratings

Supply Voltage, VCC	-0.3V~30V
High voltage pin, HV	-0.3V~700V
OUT	-0.3V~VCC +0.3V
COMP, ZCD, CS	-0.3V~6V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOP-7, θ_{JA})	160°C/W
Power Dissipation (SOP-7, at Ambient Temperature = 85°C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (Except HV pin)	2.5KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stress above recommended operating conditions may affect device reliability.

Recommended Operating Conditions*Note1

Item	Min.	Max.	Unit
Supply VCC Voltage	10	26	V
VCC pin capacitor	10	47	μF
Operating Junction Temperature	-40	125	°C
Comp pin capacitor	0.22	4.7	μF
CS pin filter capacitance	100	680	pF
CS pin filter resistance	51	300	Ω
HV resistor Value (AC Side) *Note2	2	10.5	KΩ
HV to GND Capacitor Value *Note3	--	330	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
2. This application is based on system operation condition, that's an effect factor of brown in/ out function. Please refer to electrical characteristic information or contract us.
3. This application is based on system operation condition, please refer to detail introduction on application information or contract us.

Electrical Characteristics

(V_{CC}=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High voltage Supply (HV Pin)						
High-Voltage Current Source	VCC<V_{UV_OFF},HV=500 V_{DC}	I_{HV_LO}	-	1.8	-	mA
Off-state Leakage Current	V_{CC}> V_{UV_ON},HV=500 V_{DC}	I_{HV_OFF}	-	-	30	μA
Brown-in Level		V_{HVBI}	-	90	100	V
HV Pin Hysteresis	V_{HVBI} - V_{HVBO}	ΔV_{HV}	-	10	-	V
Supply Voltage (VCC Pin)						
Startup Current	V_{CC}<V_{UV_ON}	I_{ST}	-	75	95	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V, ZCD=0	I_{OP_LO}	-	1	-	mA
	V_{COMP}=3V, ZCD=0	I_{OP_HI}	-	1.5	-	mA
	* OSCP, OLP	I_{OP_LATCH}	-	0.3	-	mA
	ZCD OVP, V_{CC} OVP	I_{OP_PRO}	-	0.3	-	mA
UVLO (OFF)		V_{UV_OFF}	7	8	9	V
UVLO (ON)		V_{UV_ON}	15.5	16.5	17.5	V
HV Self Bias (Linear Regulator)		V_{LDO_LO}	9	10	11	V
De-Latch VCC Voltage	PDR(Power Down Reset)	V_{PDR}	6.8	7.5	8.2	V
VCC OVP Level		V_{CC_OVP}	27	28	29	V
VCC OVP De-bounce Time	*	T_{DEB_OVP}	-	250	-	μs
Voltage Feedback (Comp Pin)						
Short circuit current	V_{COMP}=0	I_{COMP}	0.4	0.5	0.6	mA
Open loop voltage		V_{CMP_OPEN}	5.0	5.4	5.8	V
OLP Trip Level		V_{OLP}	4.45	4.6	4.75	V
Zero ON-time Threshold		V_{CMP_ZOT}	0.46	0.5	0.56	V
OLP Delay Time	*	T_{DEB_OLP}	-	285	-	ms
Output Short Circuit Protection Delay	*; $V_{ZCD} \leq$ 1V and $V_{COMP} \geq V_{LOP}$	T_{DEB_OSCP}	-	140	-	ms

(V_{CC}=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Zero Current Detector (ZCD Pin)						
Upper Clamp Voltage	I_{DET}=100μA	V_{ZH}	-	4.7	-	V
Lower Clamp Voltage	$I_{DET=}$-1mA	V_{ZL}	0	-	-0.3	V
Input Voltage Threshold		V_{ZCD}	0.15	0.2	0.25	V
	Hysteresis	VH_{ZCD}	-	0.1	-	V
Input bias current	V_{ZCD}=1V~4V, OUT=Low	I_{ZCD_BIAS}	0.0	-	1.0	μA
ZCD OVP Threshold		V_{ZCD_OVP}	3.3	3.5	3.7	V
ZCD OVP De-bounce	*	T_{DEB_OVP}	-	250	-	μs
ZCD UVP Threshold	VCS = V_{OCP_L}, after V_{CC} = V_{UV_ON}	V_{ZCD_UVP}	0.7	0.78	0.9	V
Minimum (ON+OFF)-Time						
Minimum (ON+OFF)-Time	Fmax(350kHz)	T_{F_MAX}	-	2.85	-	μs
Gate Drive Output (OUT Pin)						
Output Low Level	V_{CC}=15V, I_{SINK}=20mA	V_{G_LO}	0	-	0.5	V
Output High Level	V_{CC}=15V, I_{SOURCE}=20mA	V_{G_HI}	10	-	14	V
Rising Time	*; V_{CC} =15V, CL=1000pF	T_{G_RISE}	-	250	-	ns
Falling Time	*; V_{CC} =15V, CL=1000pF.	T_{G_FALL}	-	50	-	ns
Current Sensing (CS Pin)						
Soft Start Time	*		-	10	-	ms
Current Limit	When ZCD pin voltage > 0.8V during gate off status	V_{OCP_H}	0.8	0.85	0.9	V
	*; When ZCD pin voltage ≦ 0.8V during gate off status. It's a Reduce Ratio (k) of V_{OCP_H}	k	0.45	0.5	0.55	
Leading edge blanking time	*		-	375	-	ns
Current Limit-2	During LEB time window	V_{OCP2}	0.63	0.73	0.83	V
Counter Time of Current Limit-2	*	T_{DEB_DSP}	-	7	-	Times
OCP Compensation Current	I_{OCP} per $V_{IN,AC}$ on HV pin	I_{OCP}	170	200	220	μA/V
Internal OTP (Over Temp. Protection)						
OTP Trip level	*		-	140	-	°C
OTP Hysteresis	*		-	30	-	°C

*: Guaranteed by design.

Typical Performance Characteristics

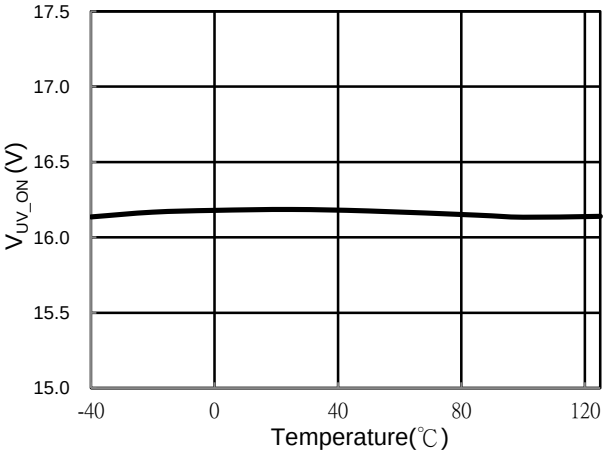


Fig.1 V_{UV_ON} VS. Temperature

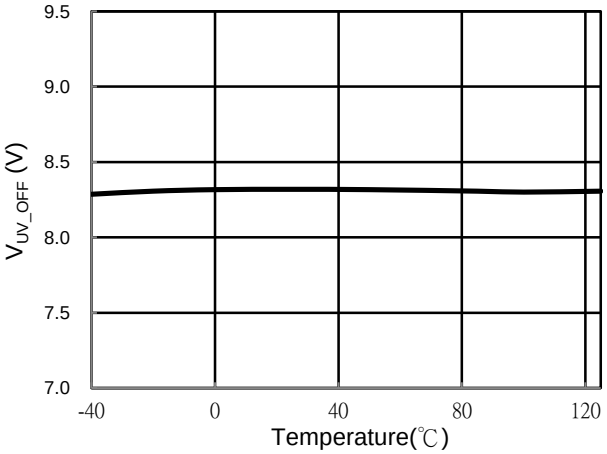


Fig.2 V_{UV_OFF} VS. Temperature

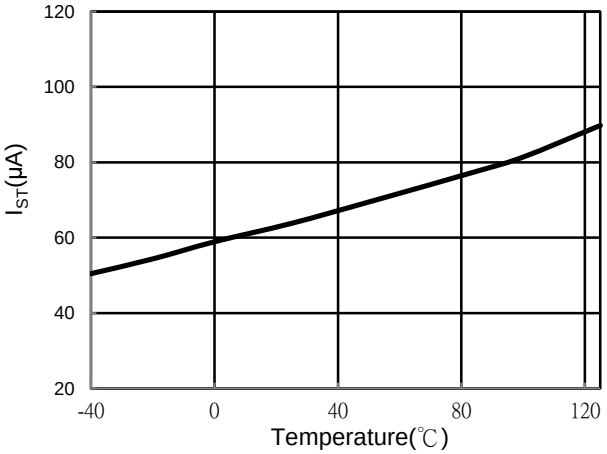


Fig.3 I_{ST} VS. Temperature

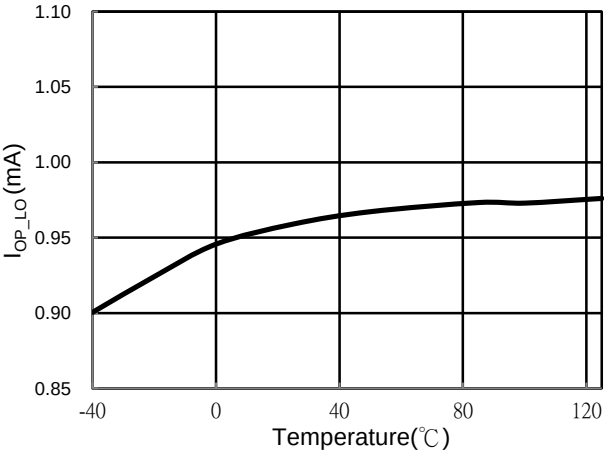


Fig.4 I_{OP_LO} VS. Temperature

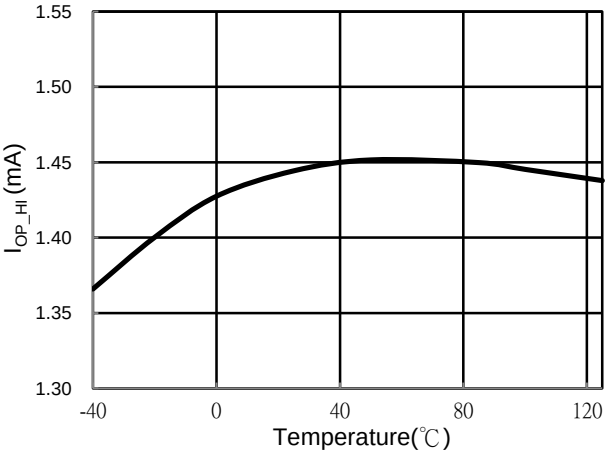


Fig.5 I_{OP_HI} VS. Temperature

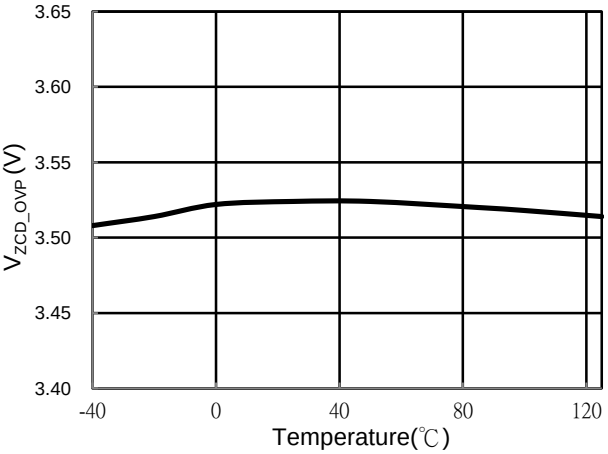


Fig.6 V_{ZCD_OVP} VS. Temperature

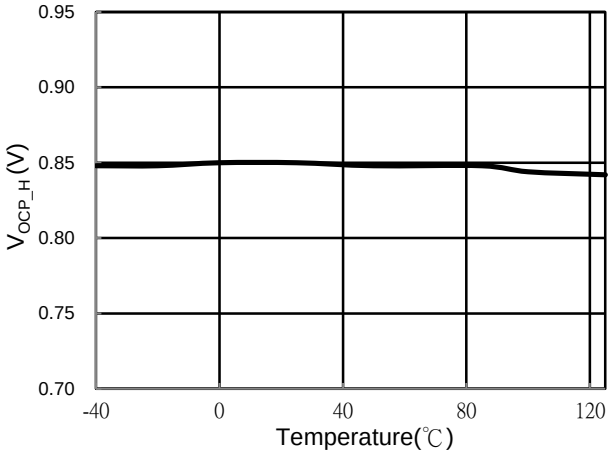


Fig.7 V_{OCP_H} VS. Temperature

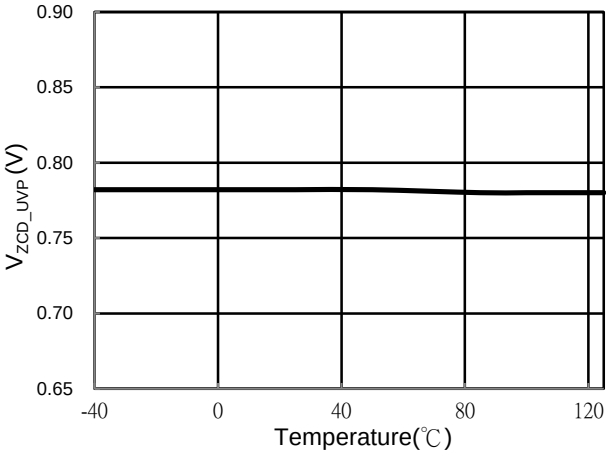


Fig.8 V_{ZCD_UVP} VS. Temperature

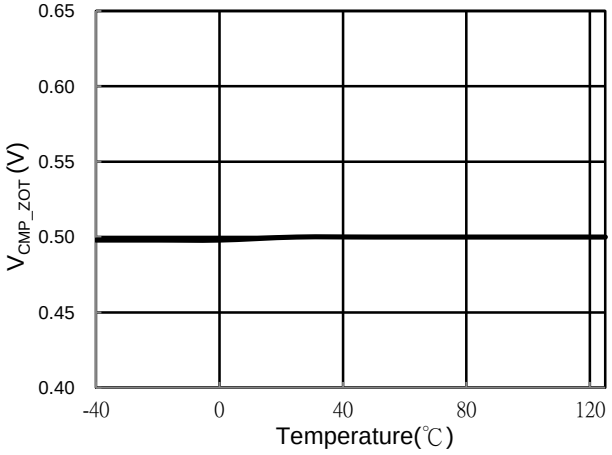


Fig.9 V_{CMP_ZOT} VS. Temperature

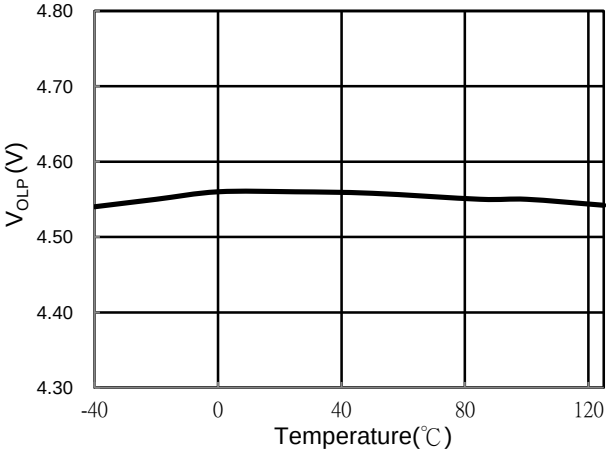


Fig.10 V_{OLP} VS. Temperature

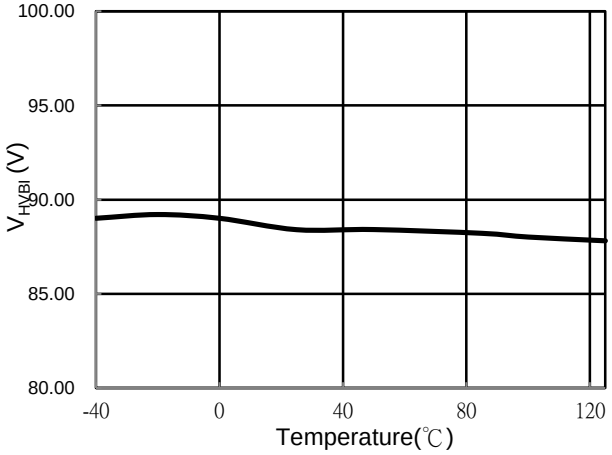


Fig.11 V_{HVBI} VS. Temperature

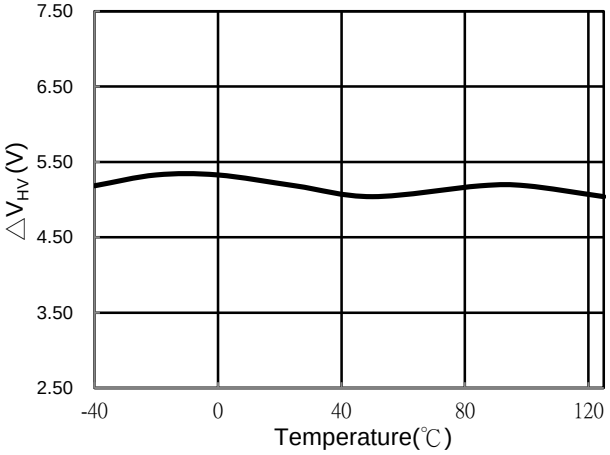


Fig.12 $\triangle V_{HV}$ VS. Temperature

Application Information

Operation Overview

The LD7838H is an excellent single-stage flyback PFC controller for LED lighting applications. It integrates more functions to reduce the external components counts and the size. Its major features are described as below.

The LD7838H is a transition mode(TM) and voltage-mode PFC controller. The turn-on time of the switch is fixed while the turn-off time is varied in steady state. Therefore, the switching frequency varies in accordance with the input voltage or output power variation. The LD7838H provides complete protections as over load protection, over voltage protection, over current protection, under voltage lockout and LEB of the current sensing. Also, the LD7838H requires no mains voltage sensing unlike what the other traditional current mode PFC controllers behave for power saving.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes significant power to meet the power saving requirement. In most cases, startup resistors carry large resistance. A larger resistor will spend more time to start up.

To achieve optimized topology, as shown in Fig. 13, LD7838H is implemented with a high-voltage startup circuit to enhance it. During startup, a high-voltage current source sinks current from the full-bridge rectifier to provide the startup current and charge Vcc capacitor C1 at the same time. On condition of VCC below UVLO(ON), the charge current will increases to 1.8mA once V_{CC} rises above UVLO(ON) voltage threshold during start up. Meanwhile, it consumes only 75μA for V_{CC} supply current, that most of the HV current is reserved to charge the V_{CC} capacitor. In using such configuration, the turn-on delay time will be almost no difference either in low-line or high-line conditions.

Once the V_{CC} voltage rises higher than UVLO(ON) to power on the LD7838H and further to deliver the gate drive signal, the high-voltage current source will be disabled and the supply current is provided from the auxiliary winding of the transformer. Therefore, it would eliminate the power loss on the startup circuit and perform highly power saving.

An UVLO comparator is embedded to detect the voltage on the Vcc pin to ensure the supply voltage enough to power on the LD7838H PWM controller and in addition to drive the power MOSFET. As shown in Fig. 14, a hysteresis is provided to prevent the shutdown from the voltage dip during startup.

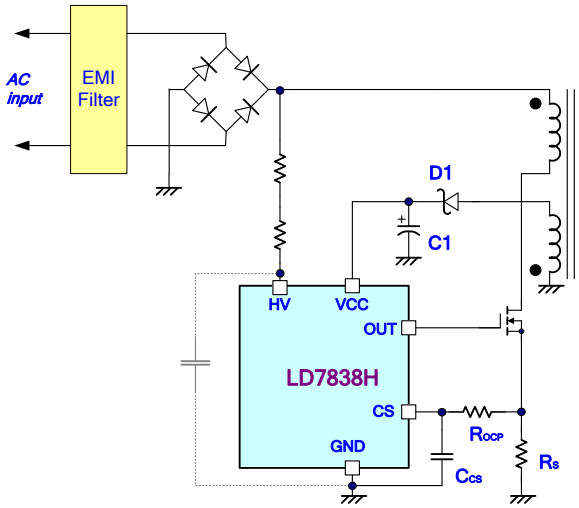


Fig. 13

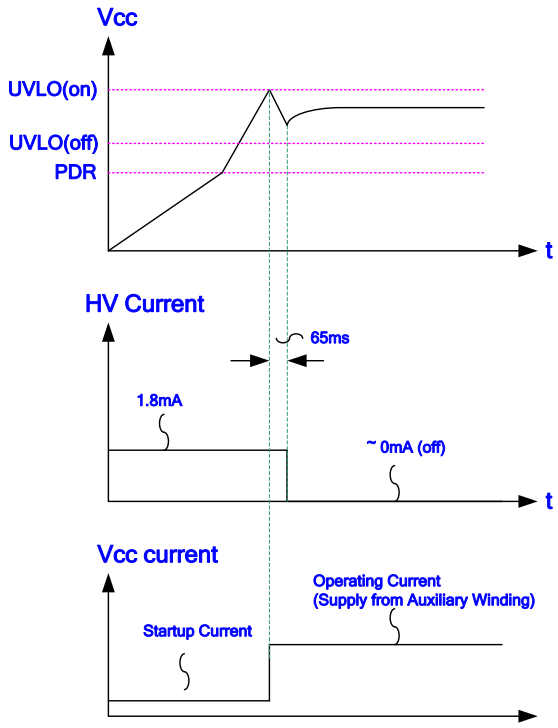


Fig. 14

Ramp Generator Block and Zero Current Detection (ZCD)

Fig. 15 shows typical ramp generator block and ZCD block. The comp pin voltage and the output of the ramp generator block are compared to determine the MOSFET on-time.

A greater comp voltage produces more on-time. Using an external resistor connected to ZCD pin to set the desired slope of the internal ramp, the user may program the maximum on-time. Alternatively, the on-time will also achieve its maximum when COMP pin voltage trip OLP trigger point.

The maximum on-time should be set according to the condition of the transformer, lowest AC line voltage, and maximum output power. A choice of optimum resistor value would result in best performance.

It shuts down the drive output if COMP pin voltage falls below zero on-time threshold. This optimizes the efficiency in power saving in most conditions.

The zero current detection block will detect auxiliary winding signal to drive MOSFET as ZCD pin voltage drops to 0.1V. As ZCD pin voltage drop to 0.1V, the current through the transformer is below zero. This feature enables transition-mode operation. The ZCD comparator would not operate if ZCD pin voltage remains at above 0.2V. Once it drops below 0.1V, the zero current detector will act to turn on the MOSFET.

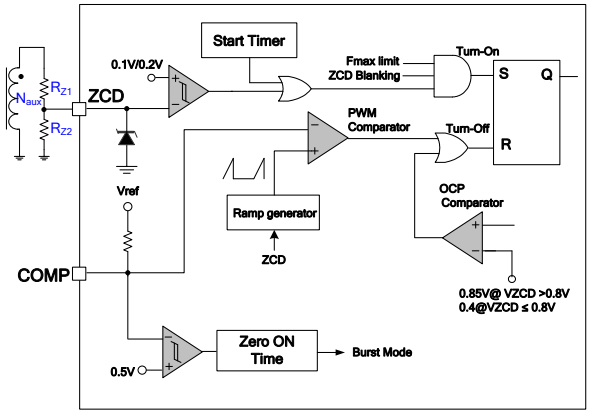


Fig. 15

Fig. 16 shows typical ZCD-related waveforms. Since ZCD pin carries some capacitance, it produces some delay to the turn-on time caused from R_{Z1}. During delay time, the junction capacitor of the MOSFET resonates with the primary inductor of the transformer and the drain-source voltage (V_{DS}) decreases accordingly. So, the MOSFET consumes less voltage to turn on and it therefore minimizes the power dissipation.

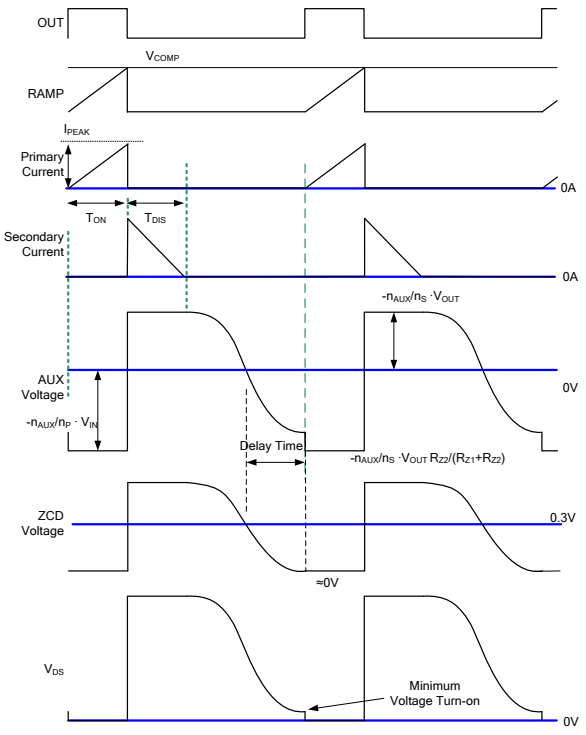
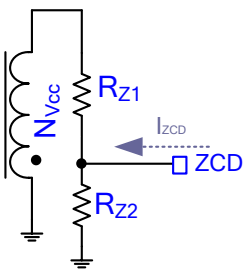


Fig. 16

Programming Maximum On-Time

LD7838H provides adjustable maximum on-time to limit power output in abnormal operation. The selection of maximum on-time is subject to ZCD resistance as shown in Fig. 17. ZCD resistance can be obtained from below, but order to avoid ZCD pin over rating, I_{ZCD} must be set less than 3mA.



$$R_{ZCD} = \frac{R_{Z1} \cdot R_{Z2}}{R_{Z1} + R_{Z2}} \quad \text{and} \quad I_{ZCD} = \frac{V_{in,peak}}{R_{Z1}} \times \left(\frac{N_{VCC}}{N_P}\right)$$

Fig. 17

The following table is a suggestion for maximum ON-time setting.

R_{ZCD}	Max. Ton (Typ.)	Suggestion
44.65k ≦ R_{ZCD}	25μs	47kΩ
25.65k ≦ R_{ZCD} ≦ 28.35k	20μs	27kΩ
13.3k ≦ R_{ZCD} ≦ 14.7k	16μs	14kΩ
R_{ZCD} ≦ 6.3k	10μs	6kΩ

Output OVP on ZCD - Auto

When the LED string open circuit occurs, the reflected output voltage of aux winding will cause ZCD voltage up. If the ZCD voltage runs up to 3.5V after gate-off has 1.5μs delay, LD7838H will enforce the gate off until the 1st cycle of Vcc hiccup is tripped, the selection of output over voltage (V_{OVP})trigger level is subject to ZCD divide resistance as the below equation:

$$V_{OVP} \times \frac{N_{VCC}}{N_S} \times \frac{R_{Z2}}{R_{Z1}+R_{Z2}} = 3.5V$$

Output Drive Stage

With typical 125mA/-500mA driving capability, an output stage of a CMOS buffer is incorporated to drive a power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage is higher than 13V.

Current Sensing and Leading-Edge Blanking

The LD7838H detects the primary MOSFET current from the CS pin, which is for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V when ZCD voltage is higher than ZCD UVP Threshold (V_{ZCD_UVP}); but if ZCD voltage level is under V_{ZCD_UVP}, the maximum voltage threshold of the current sensing pin is approached to ~0.4V. From

above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{V_{CS}}{R_S} = \frac{V_{OCP\_H} - \Delta V_{OCP}}{R_S} = \frac{0.85 - \Delta V_{OCP}}{R_S}$$

Where $\Delta V_{OCP} \approx (I_{CS} \times R_{OCP})$ and $I_{CS} = V_{IN,AC} \times I_{OCP}$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the different rated power application, if the total pulse width of the turn-on spikes is less than and the negative spike on the CS pin doesn't exceed -0.3V, it could eliminated the R-C filter.

However, the total pulse width of the turn-on spike is determined by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

Adjustable OCP Compensation

In general, the power converter can deliver more current dependent on input voltage real value on HV pin. To compensate this, an offset voltage is added to the CS signal by an internal current source (I_{OCP}) and an external resistor (R_{OCP}) in series between the sense resistor (R_S) and CS pin, as shown in Fig. 18.

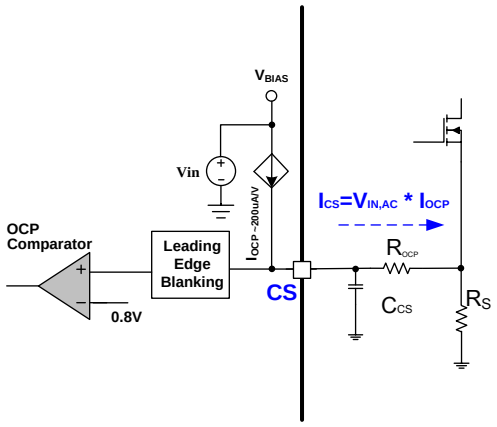


Fig. 18

By selecting a proper value of the resistor in series with the CS pin, the amount of compensation can be adjusted.

Output Short Circuit Protection (OSCP) - Auto

To protect the circuit from damage due to output short condition, a smart OSCP function is implemented in the LD7838H for it. This function is an auto recovery type protection. Under such fault condition, the feedback system will pull auxiliary wire voltage on ZCD (V_{ZCD}) pin to lower than ZCD UVP threshold (V_{ZCD_UVP}) then force the voltage loop toward saturation and thus pull up the voltage of COMP pin (V_{COMP}). When the V_{ZCD} is lower than V_{ZCD_UVP} and trips the OLP threshold of 4.6V and stays for over output short circuit protection delay time (~140ms), LD7838H will enforce the gate off until the 4th cycles of V_{CC} hiccup is tripped, as shown in Fig. 19.

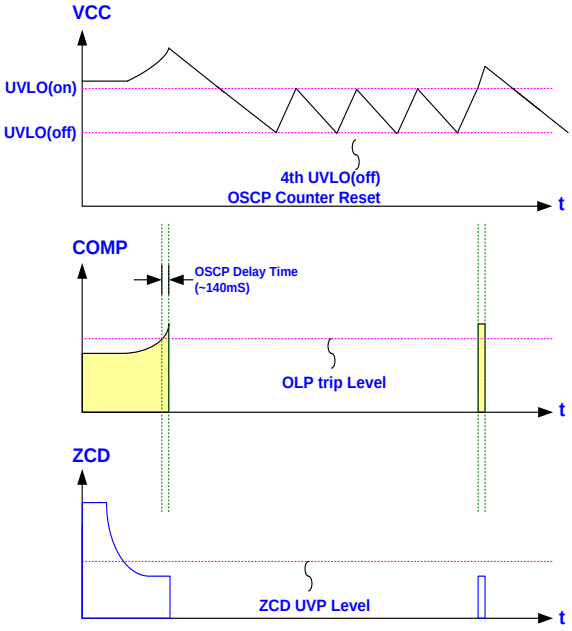


Fig.19

Over Load Protection (OLP) - Latch

To protect the circuit from damage due to overload condition, a simple OLP function is implemented in the

LD7838H which is a latch type protection. Under such fault condition, the feedback system will force the voltage loop toward saturation and thus pull up the voltage of COMP pin (V_{COMP}). If the V_{COMP} trips the OLP threshold of 4.6V and ZCD voltage is higher than ZCD UVP threshold (V_{ZCD_UVP}) and lower than ZCD OVP threshold (V_{ZCD_OVP}) then stays for over load protection delay time(~285ms), the protection will be activated to turn off the gate output and to shut down the switching of power circuit then latch itself. The OLP delay time is to prevent the false-trigger during the power-on and turn-off transient. Whenever OLP is activated, this latch mode will be released if the V_{CC} is pull low under de-latch voltage point (V_{PDR}) then the output recovers switching again.

OVP (Over Voltage Protection) on V_{CC} Pin-Latch

The maximum rating of the V_{CC} pin is limited below 30V. To prevent V_{CC} from the fault condition, the LD7838H is implemented with OVP function on V_{CC} pin. As soon as the V_{CC} pin voltage is over OVP threshold voltage, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(ON). The over voltage of V_{CC} pin protect function of LD7838H is a latch type protection. This latch mode will be released if the V_{CC} is under de-latch voltage point (V_{PDR}), then the output recovers switching again, as shown in Fig. 20.

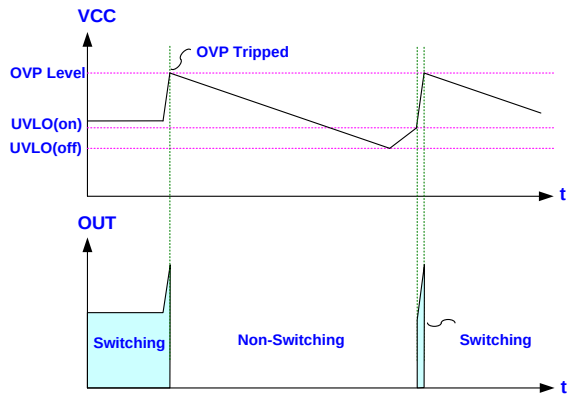
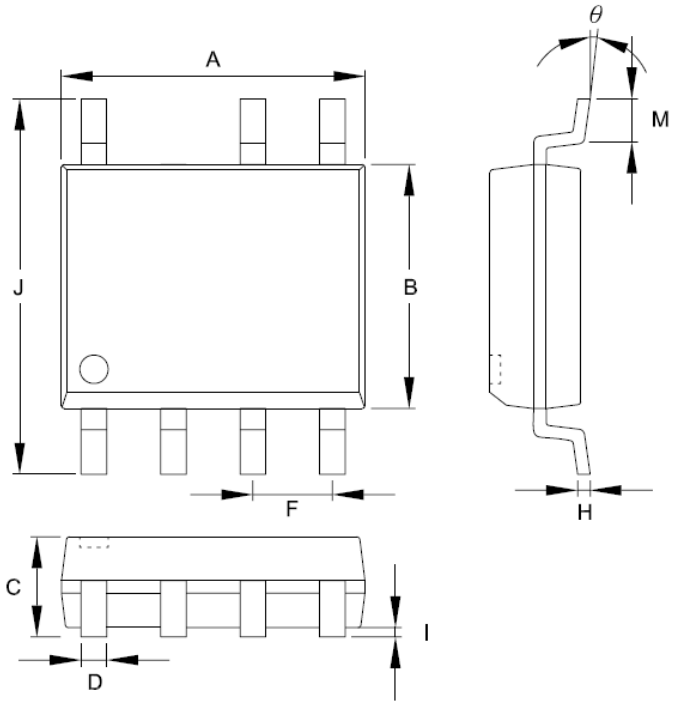


Fig.20

Package Information

SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	12/28/2017	Original Specification