Synchronous Rectification Driver with Green Mode Function

REV. 00

General Description

LD8523/P is a secondary side synchronous rectification (SR) driver IC. It combines a low voltage drop N-channel MOSFET to improve efficiency and reduce heat from secondary-side rectifier.

LD8523/P is suited for flyback low side and high side synchronous rectification in CCM, DCM and QR mode. For forward freewheeling rectification application, LD8523/P can be applied in CCM and DCM operation.

In light load condition, LD8523/P will enter green mode to reduce operation current by stopping SR MOSFET driving function.

Load regulation improve function is an innovative design in LD8523/P. With this unique function, switch power supply can achieve minimum load regulation easily.

Features

- Suited for low side flyback synchronous rectification in CCM, DCM and QR(valley lock) mode
- Suited for forward freewheeling rectification in CCM and DCM
- LD8523P is suitable for primary side with peak load function
- VCC range from 3V to 7.5V
- Programmable turn-off level
- Fast turn-off total delay of 30ns
- 220μA Ultra low green mode operation current
- Cable loss compensation Improve function
- Gate source/sink capability: 0.5A/-3A

Applications

- Switching AC/DC adaptor and battery charger
- Open frame switching power supply

Typical Application

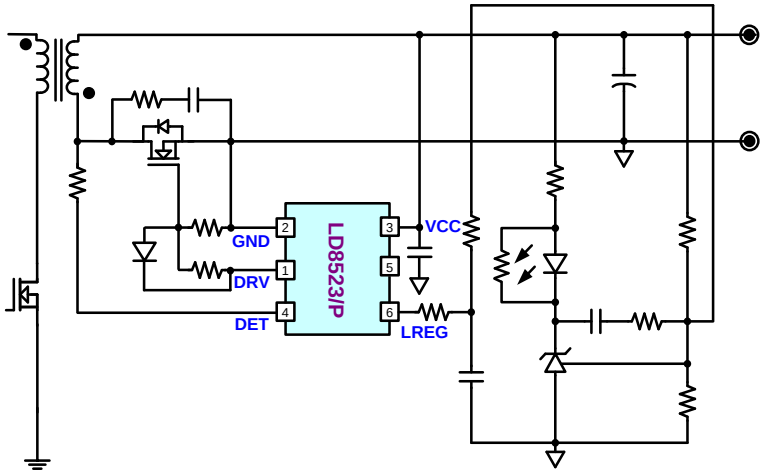
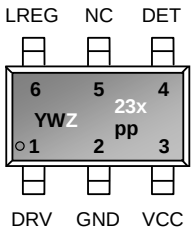


Fig. 1 Flyback Low Side Synchronous Rectification

Pin Configuration

SOT-26 (TOP VIEW)



Y : Year code
W : Week code
PP : Production code
Z23x : LD8523 or LD8523P

Ordering Information

Part number	Package		Top Mark	Shipping
LD8523 GL	SOT-26	Green Package	YWZ/23	3000 /tape & reel
LD8523P GL	SOT-26	Green Package	YWZ/23P	3000 /tape & reel

The LD8523/P is ROHS compliant/ green packaged

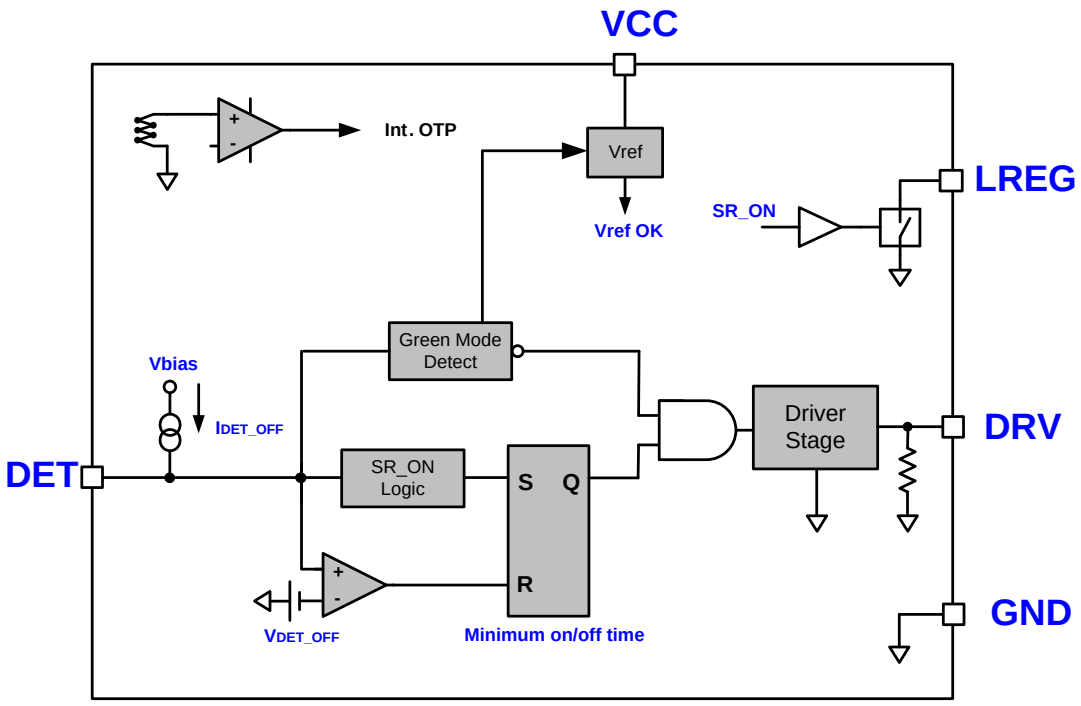
Protection Mode

Part number	Int. OTP
LD8523	Auto-Restart
LD8523P	Auto-Restart

Pin Descriptions

PIN (SOT-26)	NAME	FUNCTION
1	DRV	Driving pin, connector to GATE pin of MOSFET directly or through a resistor
2	GND	Ground pin
3	VCC	Supply voltage pin
4	DET	Synchronous rectification detection
5	NC	No connect
6	LREG	Cable loss compensation pin

Block Diagram



Absolute Maximum Ratings

DET	-0.7V ~ 80V
VCC	-0.3V ~ 7.5V
DRV	-0.3V~VCC+0.3V
LREG	-0.3V ~ 6V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOT-26)	200°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	200mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except of DET Pin)	2.5KV
ESD Voltage Protection, Human Body Model (DET Pin)	1KV
ESD Voltage Protection, Machine Model	250V

Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item		Min.	Max.	Unit
Operating Junction Temperature		-40	125	°C
Supply Voltage VCC		3	5.5	V
Power MOS Gate Threshold Voltage		1.5	4	V
Operating Frequency	LD8523		65	KHz
	LD8523P		130	KHz
VCC capacitor		0.1		μF
MOSFET Ciss (1)		1000	5500	pF
Turn-Off Rgate (1)		0	5	Ω
RDET			200	Ω

Notes:

1. When MOSFET Ciss is the maximum value, turn-off Rgate must be the minimum value. On the contrary, when MOSFET Ciss is the minimum, turn-off Rgate must be the maximum.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=5V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
UVLO (on)		V_{CC_ON}	2.8	3	3.2	V
UVLO (off)		V_{CC_OFF}		2.8		V
UVLO Hysteresis		V_{CC_HYS}		0.2		V
Operating Current	Vcc=5V, DET=65kHz, 4.7nF on GATE pin	I_{VCC_OP1}		6.5	8.5	mA
	Green mode	I_{VCC_OP2}		220	250	µA
Detection Reference (DET Pin)						
Turn-on voltage		V_{DET_ON}	-400	-300	-200	mV
Turn-off voltage	(3)	V_{DET_OFF}	10	20	30	mV
Turn-off compensation current		I_{DET_OFF}	180	200	220	µA
Ring Reject Threshold		V_{DET_R}		1.6		V
Ring Reject Threshold Hysteresis	VDET_L: -0.3v	V_{DET_RHY}		1.9		V
Ring Reject Window		T_{DET_WD}	60	80	100	ns
Leakage current	V_{DET}=80V	I_{DET_LK}			1	µA
Drive (DRV Pin)						
Total Turn-on delay time	(2)	T_{D_ON}		80	120	ns
Total Turn-off delay time	(2)	T_{D_OFF}		30	35	ns
Pseudo dead time	LD8523	T_{PDT}		5		µs
	LD8523P			3.6		µs
Output High Voltage	VCC=5V, Io=10mA	V_{DRV_H}	2.6			V
Output Low Voltage	VCC=5V, Io=-10mA	V_{DRV_L}			0.5	V
Turn-off propagation delay		T_p		15		ns
Turn-on Rising time	(2), drive voltage from 20%(1V) to 80%(4V)	T_r		100		ns
Turn-off Falling time	(2), drive voltage from 80%(4V) to 20%(1V)	T_f		13		ns

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Drive (DRV Pin)						
Minimum On Time	LD8523	T_{MIN_ON}	1.2	1.5	1.8	µs
	LD8523P		0.7	1	1.3	µs
Minimum Off Time	LD8523	T_{MIN_OFF}	1.2	1.5	1.8	µs
	LD8523P		0.7	1	1.3	µs
Green mode operation						
DET pin >0V Time to Enter Green Mode		T_{DET_IGM}		1.2		ms
DET pin >0V Time to Exit Green Mode		T_{DET_OGM}		1.1		ms
Number of Switch Cycle to Enter Green Mode	(DET pin >0V Time) >t	P_{DET_IGM}		1		times
Number of Switch Cycle to Leave Green Mode	(DET pin >0V Time) >t	P_{DET_OGM}		16		times
On Chip OTP (Over Temperature) Auto-Recovery						
OTP Level	(1)	T_{OTP}		140		°C
OTP Hysteresis	(1)	T_{OTP_HYS}		30		°C

Notes:

1. Guaranteed by design.
2. Load capacitance=4.7nF.
3. For avoiding SR too late to turn off in CCM, R_{DET} must be adjusted from 200R down to appropriate value.

Typical Performance Characteristics

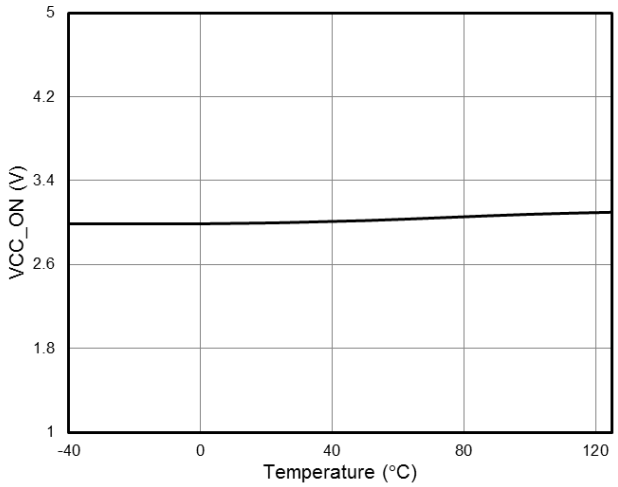


Fig. 2 UVLO ON vs. Temperature

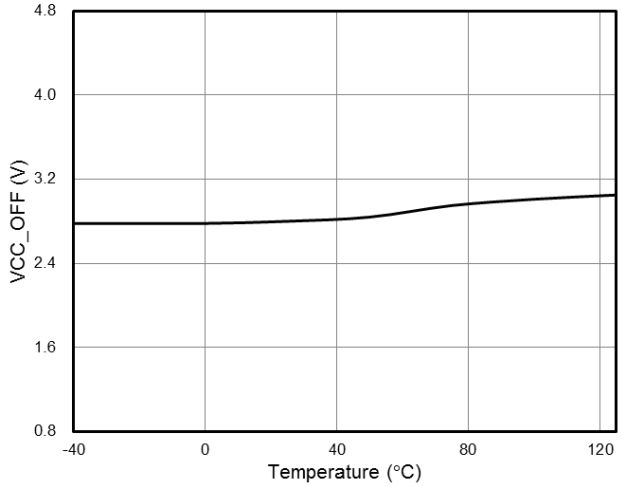


Fig. 3 UVLO OFF vs. Temperature

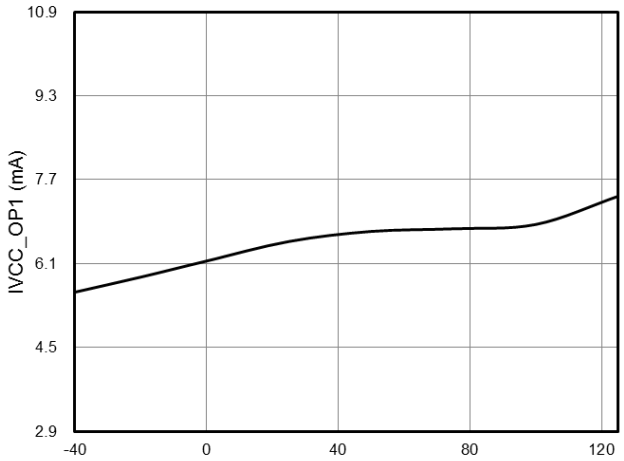


Fig. 4 Operation Current vs. Temperature

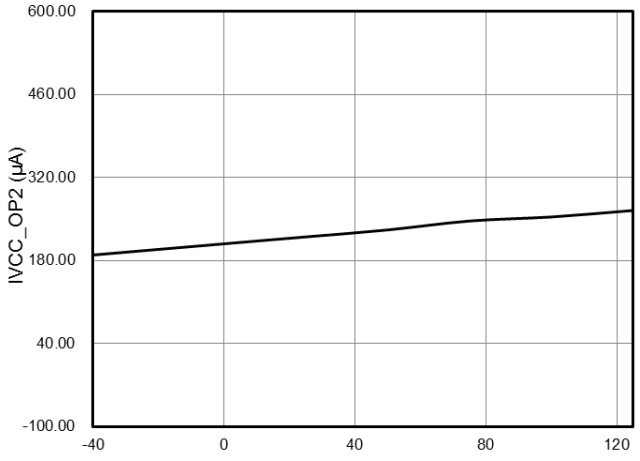


Fig. 5 Green Mode Current vs. Temperature

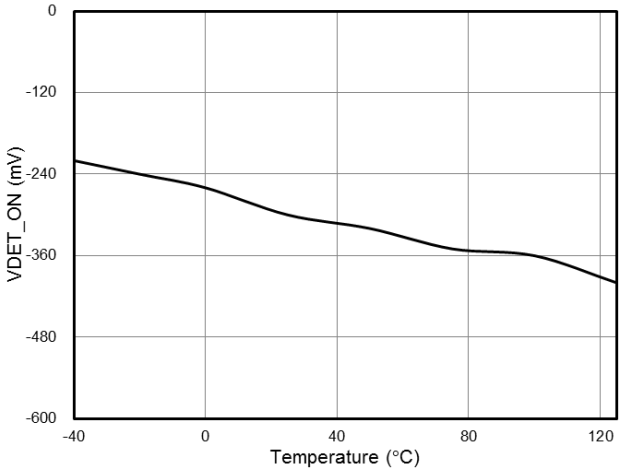


Fig. 6 Turn On Voltage vs. Temperature

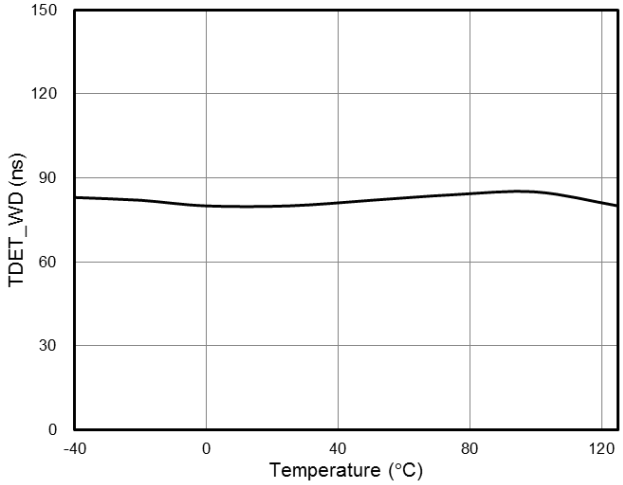


Fig. 7 Ring Reject Window vs. Temperature

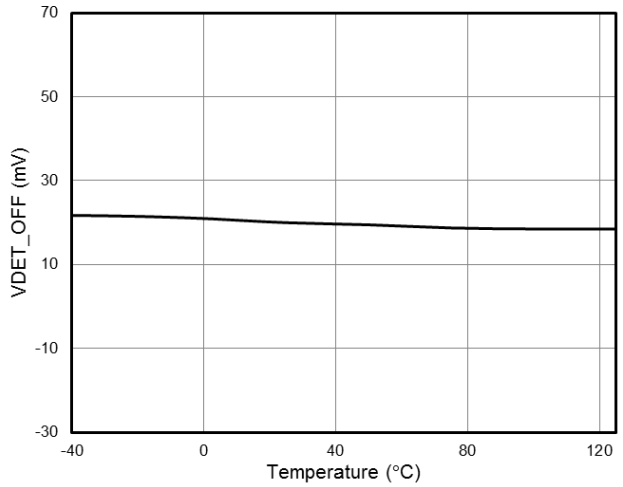


Fig. 8 Turn Off Voltage vs. Temperature

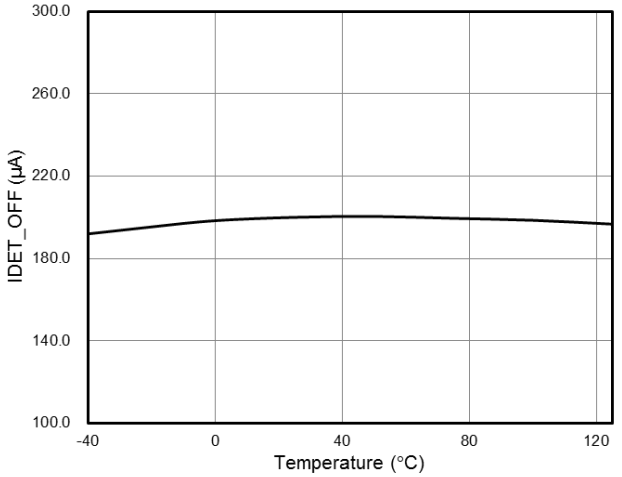


Fig. 9 Turn Ooff Compensation Current vs. Temperature

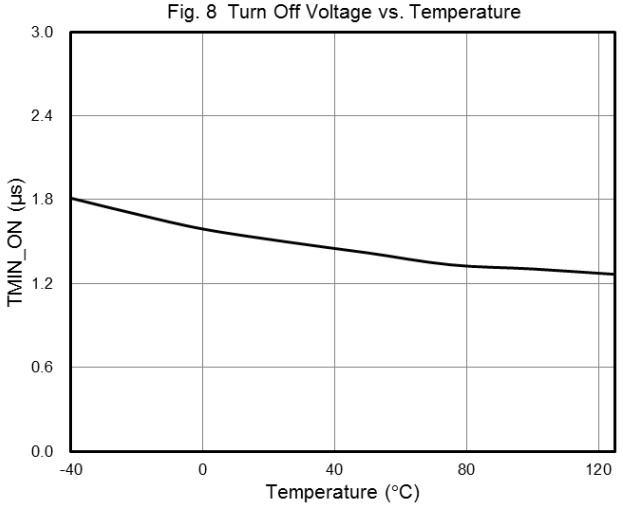


Fig. 10 Minimum On Time for LD8523 vs. Temperature

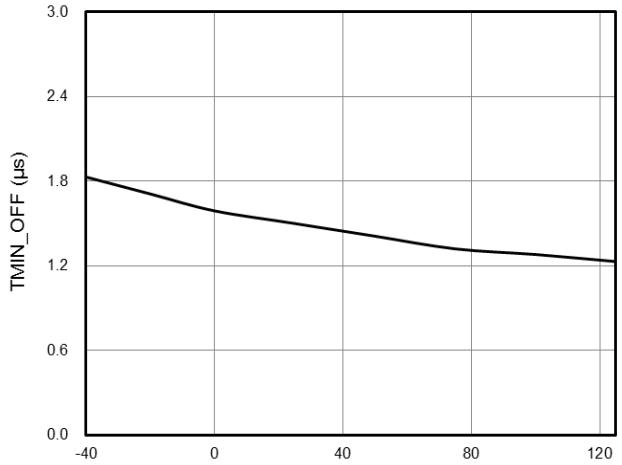


Fig. 11 Minimum Off Time for LD8523 vs. Temperature

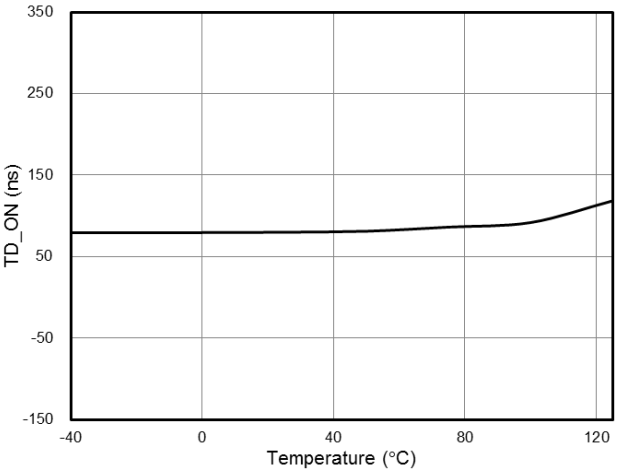


Fig. 12 Total Turn-On Delay Time vs. Temperature

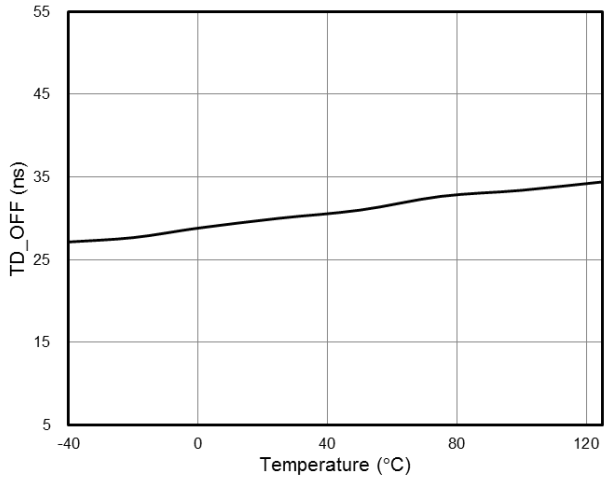


Fig. 13 Total Turn-Off Delay Time vs. Temperature

Application Information

Operation Overview

The LD8523/P is a secondary side synchronous rectification driver IC for CCM and DCM operation. The LD8523/P not only has excellent dead time control function for safety in load transient, but also only needs very few operation current in green mode. In addition, LREG pin provides a possibility to improve cable loss; it is useful for power supply with high output current.

Under Voltage Lockout (UVLO) and Enable Function

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It will assure the supply voltage enough to turn on the LD8523/P controllers and further to drive the synchronous rectifier. As shown in Fig. 14, the UVLO(ON) and UVLO(OFF) are respective 3.0V and 2.8V.

To enable synchronous rectifier, the following conditions must be met:

1. VCC > UVLO(ON)
2. Exit green mode
3. DET > V_{DET_ON}

With these restrictions, synchronous rectifier always operates in stable condition. Therefore, some unstable transient, which are like turn-on, turn-off, output short, surge, ESD…etc., will not make synchronous rectifier unsafe when it works.

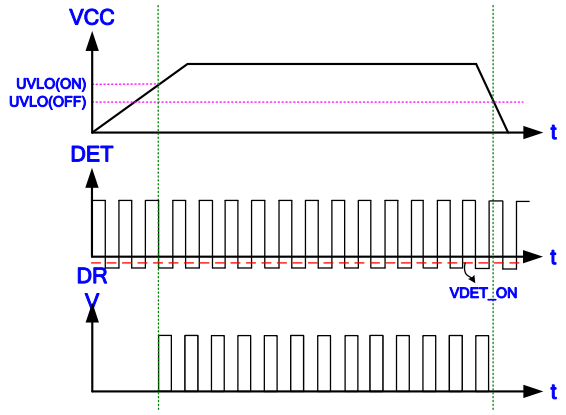


Fig. 14

Green Mode Operation

For improving the efficiency in light load conditions, LD8523/P stops SR MOSFET driving function to reduce operation current, as shown in Fig. 15.

DET pin detects system behavior. Then, the internal logic circuit determines when DRV pin turn on and turn off, what dynamic dead time is at system in load transient, when LD8523/P enter/leave green mode.

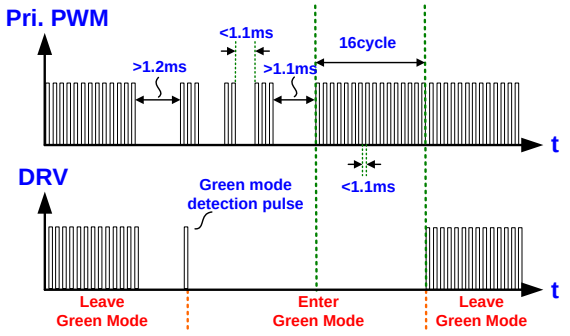


Fig. 15

Turn-on Phase

After a negative voltage (−300 mV typical) is sensed on the DET pin, the driver output voltage is made high and the external MOSFET is switched on. After switch-on of the SR MOSFET, the input signal on the DET pin is blanked for 1.5μs (typical). This will eliminate false switch-off due to high frequency ringing at the start of the secondary stroke.

Turn-off Phase

The DET pin has detection gate on time to do prediction gate pre-drop method (Ton x 0.5 = Tpredict), gate driver voltage decreases to adjust the Vds to typical (4V).

As soon as the DET voltage is above VDET_OFF, the driver output is pulled to ground. For avoiding SR too late to turn off in CCM, the following condition must be met, as shown in Fig. 16.

$$V_{DET\_OFF} - I_{DET\_OFF} \times R_{DET} + X = -10mV$$

Where I_{DET_OFF} = 200μA, V_{DET_OFF} = +20mV, X= thermal effect and parasitic inductance from trace & electronic components. Hence R_{DET} must be from 200Ω down to find the appropriate turn-off time.

Gate driver behaviors of DCM & CCM are separately shown as Fig. 17.

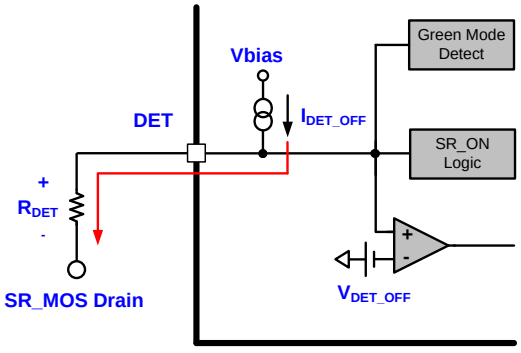


Fig. 16

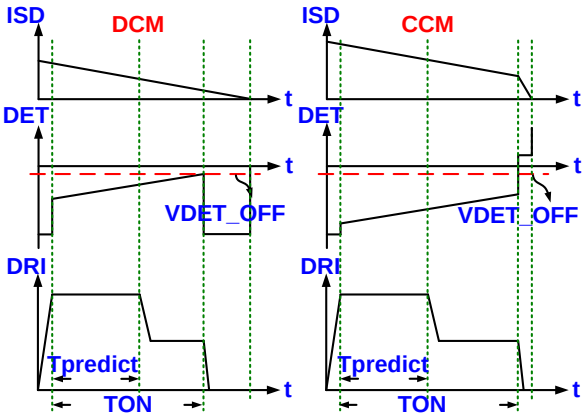


Fig. 17

LREG Pin Behavior

In some higher output current system, series voltage drop on output cable would cause worse load regulation. There is a signal level switch inside LREG pin, the switch turn on by DET signal. Generally, LREG internal switch has low impedance when secondary-side current existence, as shown in Fig. 18.

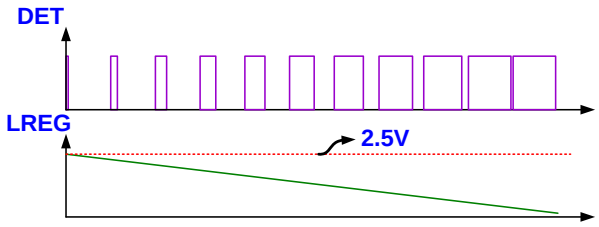


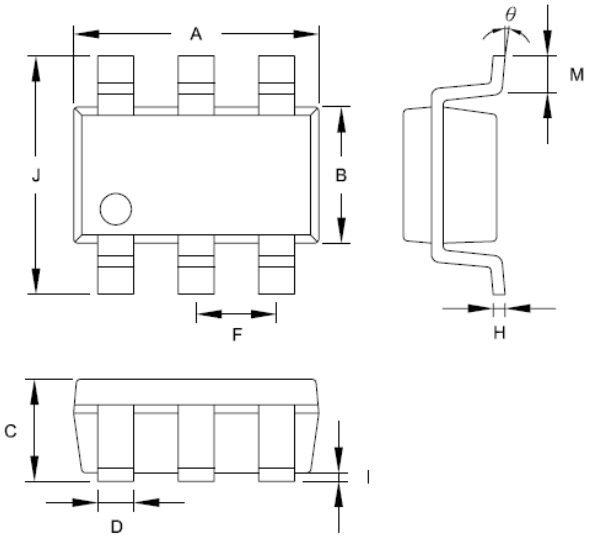
Fig. 18

On-Chip OTP - Auto Recovery

An internal OTP circuit is embedded inside the LD8523/P to provide the worst-case protection for this controller. When the chip temperature rises higher than the trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window.

Package Information

SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	11/24/2017	Original Specification