LD8526S

01/03/2020

Synchronous Rectification Driver

REV. 00

General Description

LD8526S is a secondary side synchronous rectification (SR) driver IC. It is suited for flyback low side and high side synchronous rectification in CCM, DCM and QR mode. For forward freewheeling rectification application, LD8526S can be applied in CCM and DCM operation.

LD8526S can generate its own supply voltage through high side rectification applications to charge battery.

Features

- Suited for low side and high side flyback synchronous rectification in CCM, DCM and QR(valley lock) mode
- Suited for forward freewheeling rectification in CCM and DCM
- Self-supplying for operation with low output voltage and/or high–side rectification without an auxiliary winding.
- Suited for PSR with peak load function (max. frequency 130kHz)
- Programmable turn-off level
- Fast turn-off total delay of 30ns
- Gate source/sink capability: 0.5A/-3A

Applications

- Switching AC/DC adaptor and battery charger
- Open frame switching power supply

Typical Application

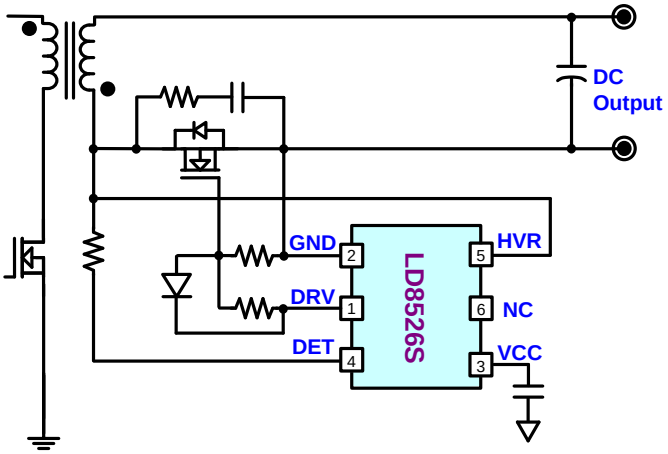


Fig. 1 Flyback Low Side Synchronous Rectification

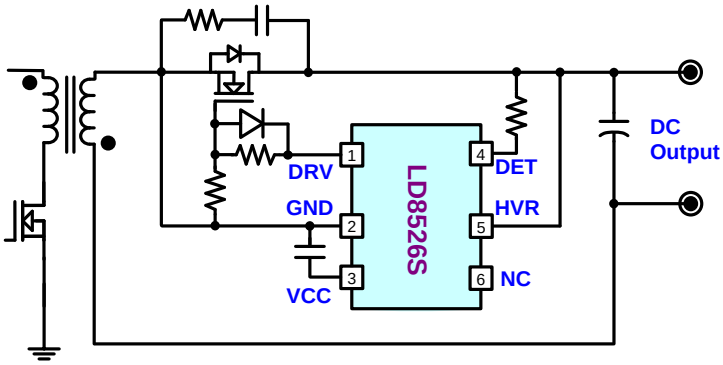
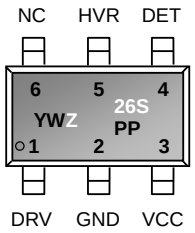


Fig. 2 Flyback High Side Synchronous Rectification

Pin Configuration

SOT-26 (TOP VIEW)



Y : Year code (D: 2004, E: 2005…..)
W : Week code
PP : Production code
Z26S : LD8526S

Ordering Information

Part number	Package		Top Mark	Shipping
LD8526S GL	SOT-26	Green Package	YWZ/26S/PP	3000 / tape & reel

The LD8526S is ROHS compliant/ green packaged.

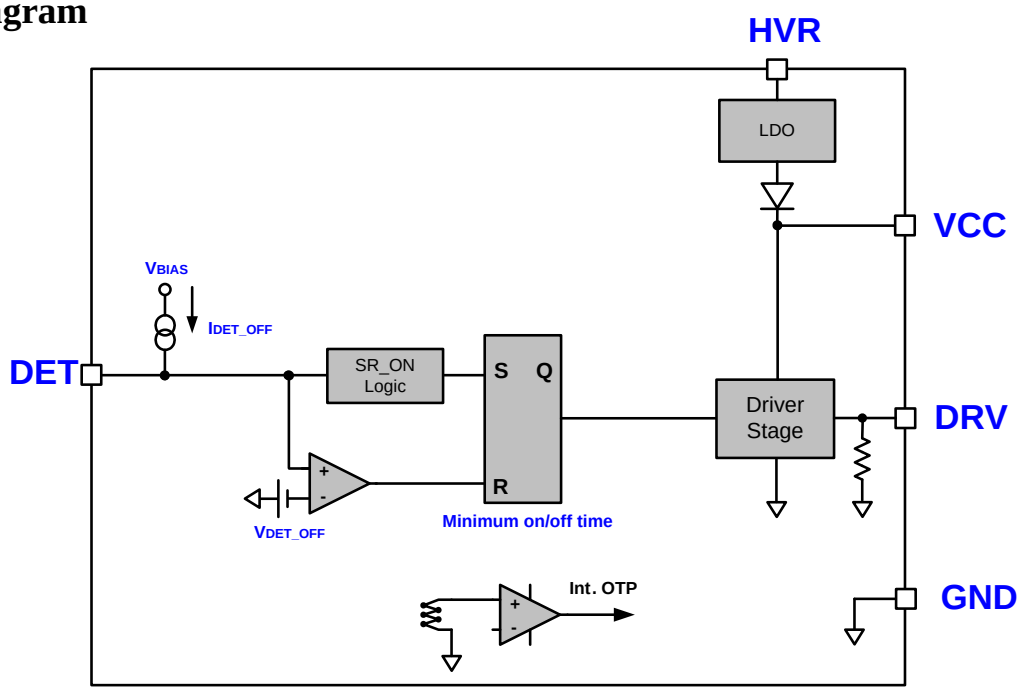
Protection Mode

Part number	Int. OTP
LD8526S	Auto-Restart

Pin Description

PIN (SOT-26)	NAME	FUNCTION
1	DRV	Driving pin, connector to GATE pin of MOSFET directly or through a resistor
2	GND	Ground pin
3	VCC	Supply voltage pin
4	DET	Synchronous rectification detection
5	HVR	HV linear regulator input
6	NC	No connect

Block Diagram



Absolute Maximum Ratings

DET	-1V ~ 200V
HVR	-1V ~ 200V
VCC	-0.3V ~ 7V
DRV	-0.3V~VCC+0.3V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOT-26)	200°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	200mW
Lead temperature (Soldering, 10sec)	260°C

Caution:

Stresses beyond the ratings specified in "absolute maximum ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply Voltage VCC	3	6	V
Power MOS Gate Threshold Voltage	1.5	4	V
Operating Frequency		130	KHz
VCC capacitor	2.2		μF
MOSFET Ciss (1)	1000	5500	pF
Turn-Off Rgate (1)	0	5	Ω
RDET		600	Ω

Notes:

1. When MOSFET Ciss is the maximum value, turn-off R_{GATE} must be the minimum value. On the contrary, when MOSFET Ciss is the minimum, turn-off R_{GATE} must be the maximum.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, HVR=30V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
HVR (HVR pin)						
HVR charge current	HVR=30V, VCC=3.5V	I_{CHG_HVR1}	20	35	50	mA
	HVR=12V, VCC=3.5V	I_{CHG_HVR2}	10	20	30	mA
Leakage current	V_{HVR}=200V	I_{HVR_LK}			50	µA
Supply Voltage (VCC Pin)						
UVLO (on)		V_{CC_ON}	2.8	3	3.2	V
UVLO (off)		V_{CC_OFF}		2.8		V
UVLO Hysteresis		V_{CC_HYS}		0.2		V
VCC Operating Voltage	HVR=30V	V_{VCC_H1}	4.5	5.8	6.8	V
Operating Current	Vcc=5V, DET=65kHz, 4.7nF on GATE pin	I_{VCC_OP1}		2.2	3	mA
	UVLO_OFF mode VCC=2.5V	I_{VCC_OFF}		350		µA
Detection Reference (DET Pin)						
Turn-on voltage		V_{DET_ON}	-400	-300	-150	mV
Turn-off voltage	(3)	V_{DET_OFF}	10	20	30	mV
Turn-off compensation current		I_{DET_OFF}	85	100	115	µA
Leakage current	V_{DET}=200V	I_{DET_LK}			1	µA

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Drive (DRV Pin)						
Total Turn-on delay time	(2)	T_{D_ON}		65		ns
Total Turn-off delay time	(2)	T_{D_OFF}		25		ns
Output High Voltage	Io=+10mA	V_{DRV_H}	4.4	4.7		V
Output Low Voltage	Io=-10mA	V_{DRV_L}			0.5	V
Turn-off propagation delay		T_P		15		ns
Turn-on Rising time	(2), drive voltage from 20%(1V) to 80%(4V)	T_r		75	150	ns
Turn-off Falling time	(2), drive voltage from 80%(4V) to 20%(1V)	T_f		13	30	ns
Minimum On Time		T_{MIN_ON}	0.7	1	1.3	μs
Minimum Off Time		T_{MIN_OFF}	0.7	1	1.3	μs
On Chip OTP (Over Temperature) Auto-Recovery						
OTP Level	(1)	T_{OTP}		150		°C
OTP Hysteresis	(1)	T_{OTP_HYS}		30		°C

Notes:

1. Guaranteed by design.
2. Load capacitance=4.7nF.
3. For avoiding SR being too late to turn off in CCM, R_{DET} must be adjusted from 600R down to appropriate value.

Typical Performance Characteristics

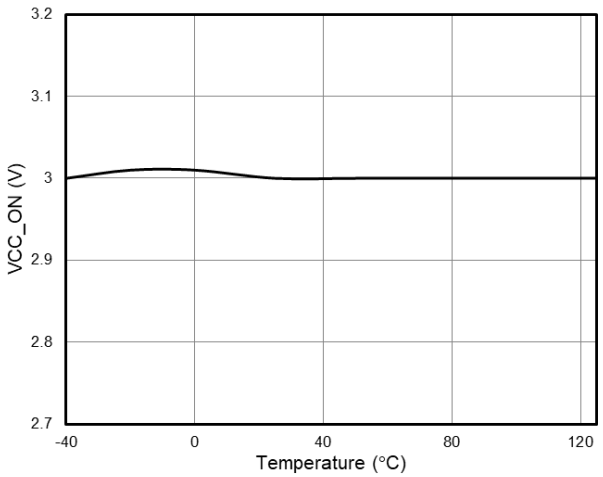


Fig. 3 UVLO ON vs. Temperature

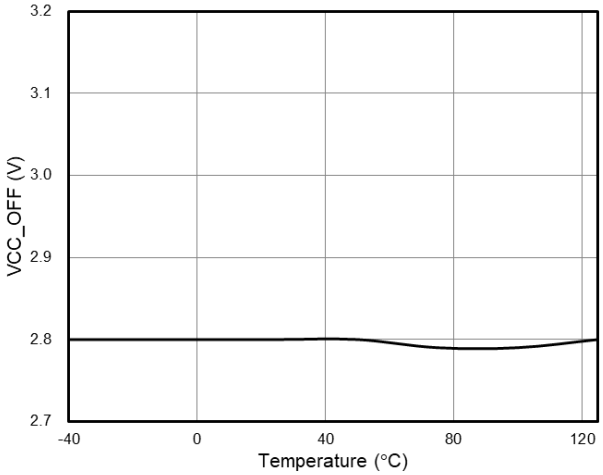


Fig. 4 UVLO OFF vs. Temperature

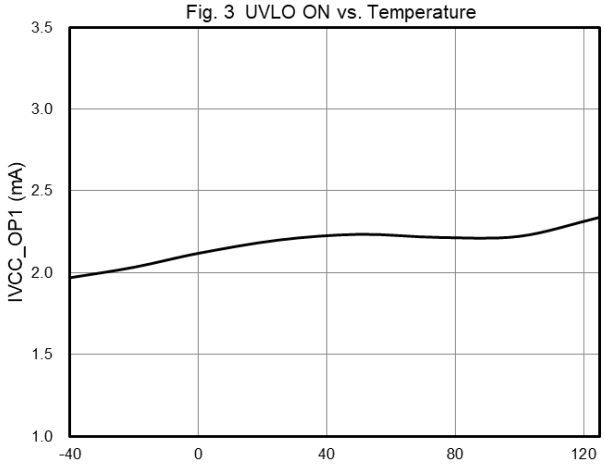


Fig. 5 Operation Current vs. Temperature

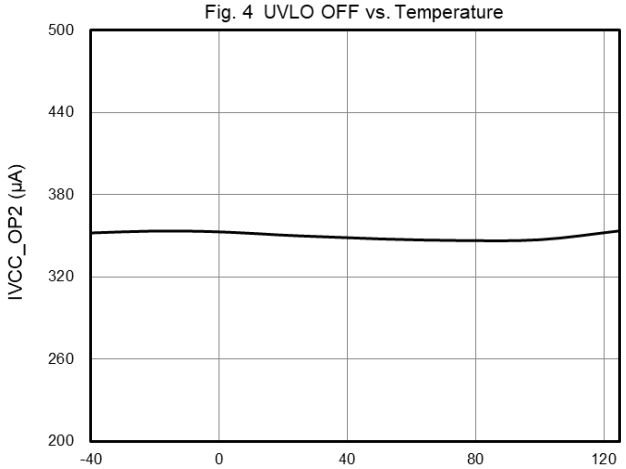


Fig. 6 Green Mode Current vs. Temperature

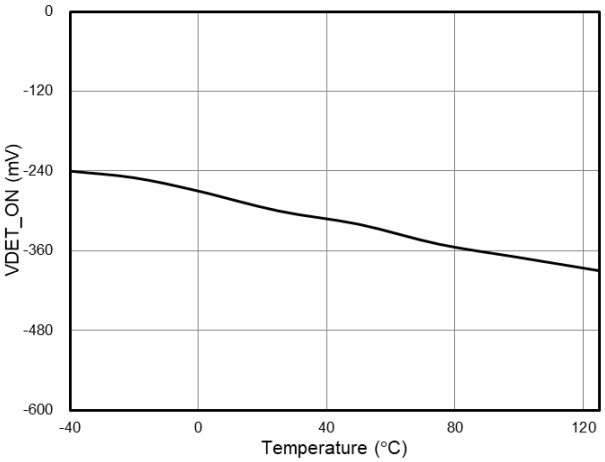


Fig. 7 Turn On Voltage vs. Temperature

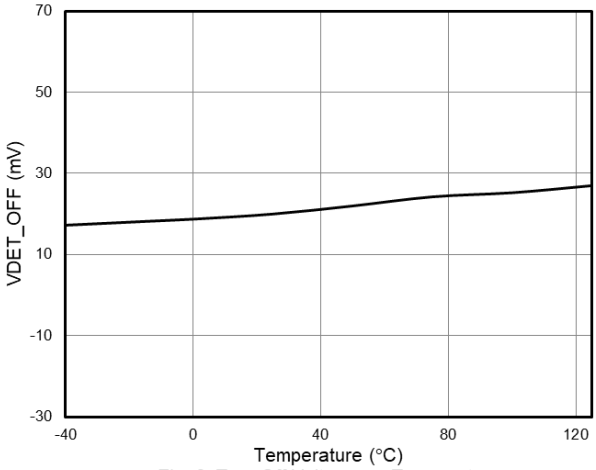


Fig. 8 Turn Off Voltage vs. Temperature

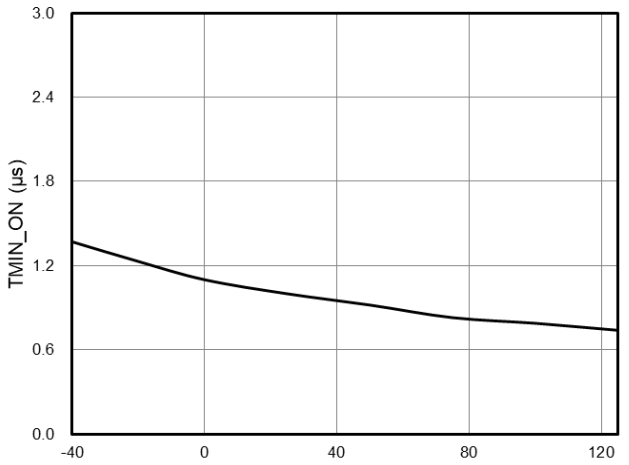


Fig. 9 Minimum On Time vs. Temperature

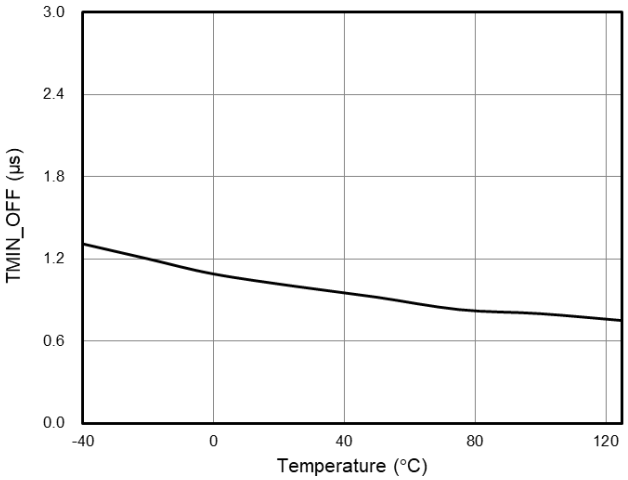


Fig. 10 Minimum Off Time vs. Temperature

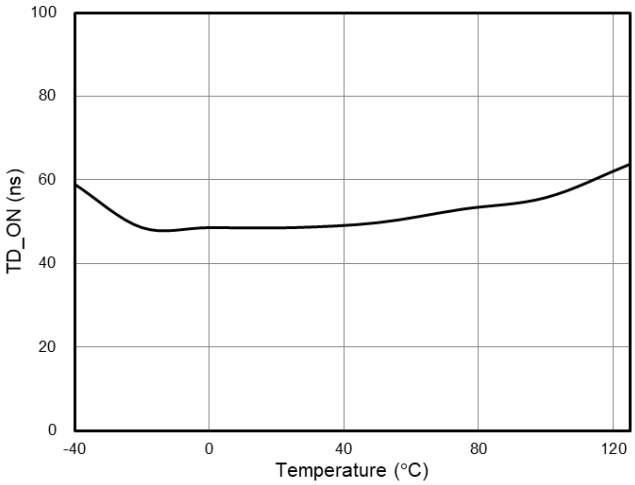


Fig. 11 Total Turn-On Delay Time vs. Temperature

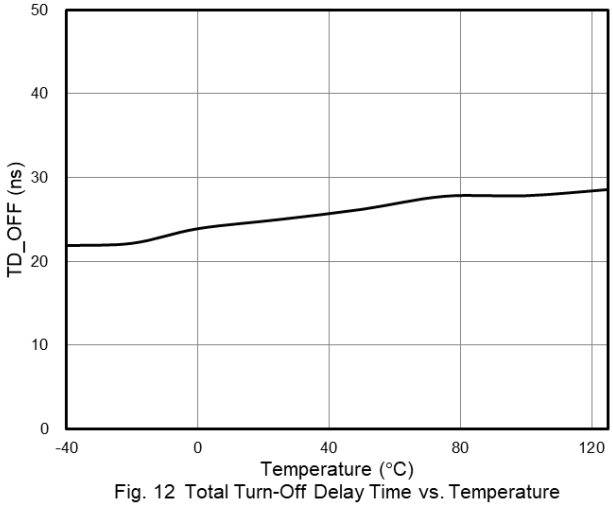


Fig. 12 Total Turn-Off Delay Time vs. Temperature

Application Information

Operation Overview

The LD8526S is a secondary side synchronous rectification driver IC for CCM and DCM operation, and has excellent dead time control function for safety in load transient. In addition, LD8526S can generate its own supply voltage through low output voltage or high side rectification applications to charge battery. Hence, LD8526S is suitable for PD application.

LDO Charge Function

LD8526S with a LDO (low drop-out regulator) provides VCC power, and charged by HVR. The LDO charging current can be controlled by connecting a resistor between HVR & MOS drain for the chip temperature optimization. Besides, a capacitor must exist from VCC to GND to store the energy.

Under Voltage Lockout (UVLO) and Enable Function

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It will assure the supply voltage enough to turn on the LD8526S controllers and further to drive the synchronous rectifier. As shown in Fig. 13, the UVLO(ON) and UVLO(OFF) are 3V and 2.8V respectively.

To enable synchronous rectifier, the following conditions must be met:

1. VCC > UVLO(ON)
2. DET > V_{DET_ON}

With these restrictions, synchronous rectifier always operates in stable condition. Therefore, some unstable transient, which are like turn-on, turn-off, output short, surge, ESD…etc., will not make synchronous rectifier unsafe when it works.

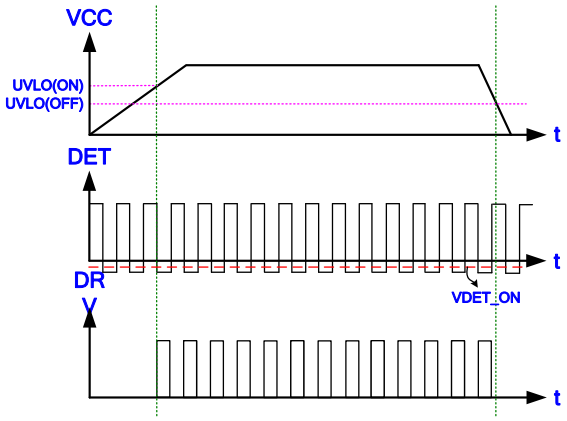


Fig. 13

Turn-on Phase

After a negative voltage (-300 mV typical) is sensed on the DET pin, the driver output voltage (DRV, see Block Diagram) is made high and the internal MOSFET is switched on. After switch-on of the SR MOSFET, the input signal on the DET pin is blanked for 1μs (typical). This will eliminate false switch-off due to high frequency ringing at the start of the secondary stroke.

Turn-off Phase

As soon as the DET voltage is above VDET_OFF, the driver output is pulled to ground. For avoiding SR being too late to turn off in CCM, the following condition must be met, as shown in Fig. 14.

$$V_{DET\_OFF} - I_{DET\_OFF} \times R_{DET} + X = -10mV$$

Where I_{DET_OFF} = 100μA, V_{DET_OFF} = +20mV, X= thermal effect and parasitic inductance from trace & electronic components. Hence R_{DET} must be from 600Ω down to find the appropriate turn-off time.

The behavior of DRV in DCM & CCM are shown separately in Fig. 15.

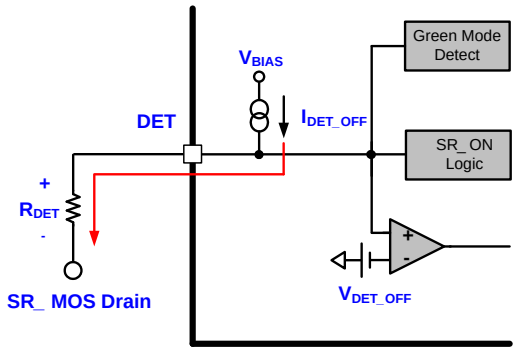


Fig. 14

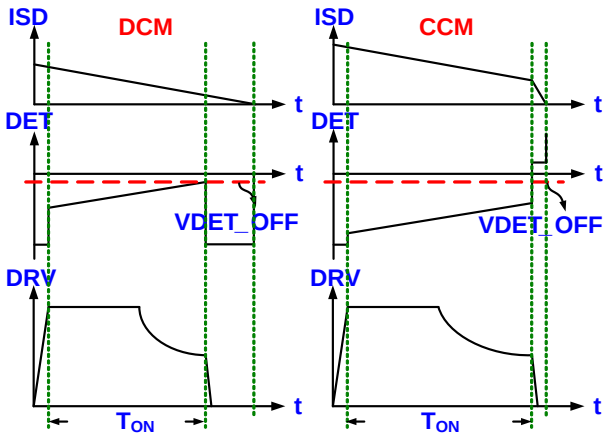


Fig. 15

On-Chip OTP - Auto Recovery

An internal OTP circuit is embedded inside the LD8526S to provide the worst-case protection for this controller. When the chip temperature rises and it's higher than the trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window.

Recommended Layout Guide

In order for the system to work properly, layout must pay attention to the following points:

1. Keep the DET and GND loops as small as possible.

2. The power loop needs to be separated from the DET detection loop.

3. Place VCC capacitor as close to IC as possible.

4. Keep the GND of IC and the source pin of MOS as short as possible.

5. To let MOS be turned OFF in time, keep 5nH~20nH inductance of PCB trace as shown in Fig.16 & Fig. 17 in red lines. The suggested trace configurations are listed below:

a. 3.5mm*18mm*2oz

b. 4mm*20mm*2oz

c. 3.5mm*9mm*1oz

d. 4mm*10mm*1oz

e. 6mm*15mm*1oz

In high side application, DET detection point needs to be close to the output capacitor, and in low side application, DET detection point needs to be close to the transformer.

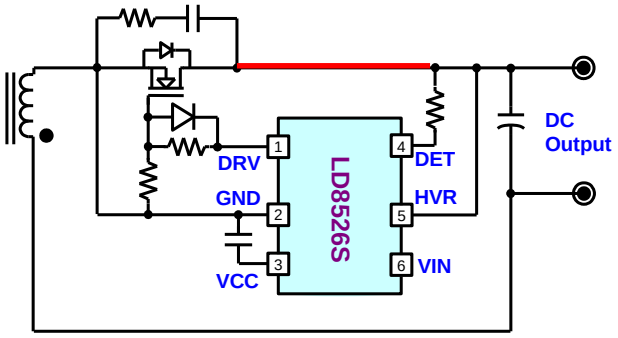


Fig. 16

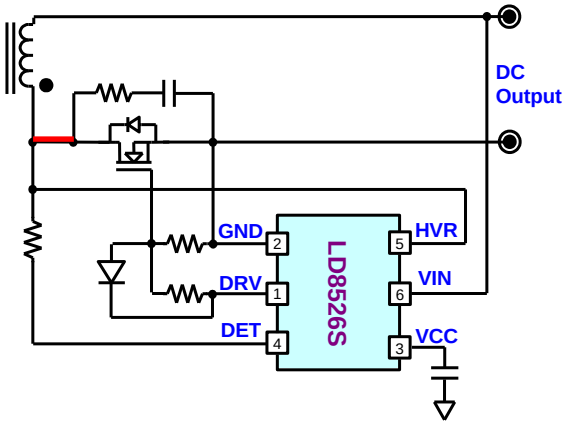
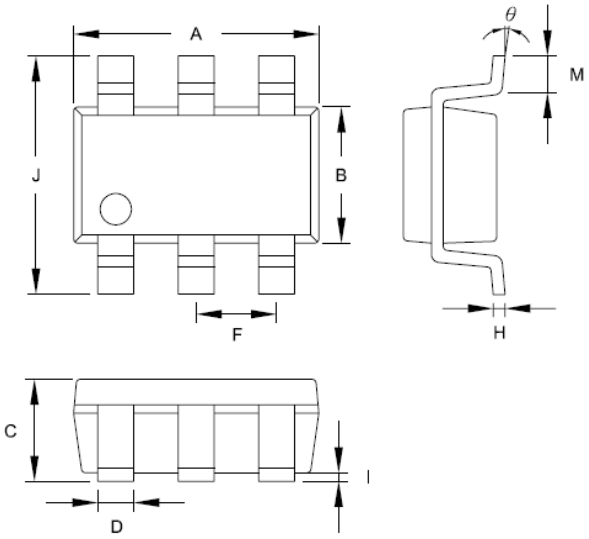


Fig. 17

Package Information

SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Revision History

REV.	Date	Change Notice
00	01/03/2020	Original Specification

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice.

Customers should verify the datasheets are current and complete before placing order.