Synchronous Rectification Driver with Green Mode Function

REV. 00

General Description

LD8926AA1 is a secondary side synchronous rectification (SR) IC with drive element and MOSFET. It is suited for flyback low side and high side synchronous rectification in CCM, DCM and QR mode. In light load condition, LD8926AA1 will enter green mode to reduce operation current by stopping SR MOSFET driving function.

LD8926AA1 can generate its own supply voltage through low output voltage or high side rectification applications to charge battery.

To reduce assembly process, layout area, and production cost, SR MOSFET and LD8926AA1 control core are packaged in SOP-8.

Features

- Suited for low side and high side flyback synchronous rectification in CCM, DCM and QR(valley lock) mode
- Suited for forward freewheeling rectification in CCM and DCM
- Self-supplying for operation with low output voltage and/or high–side rectification without an auxiliary winding
- Suited for primary side with peak load function (max. frequency 130kHz)
- Suited for PD application,
- VCC range from 3V to 6V
- Programmable turn-off level
- Fast turn-off total delay of 30ns
- 200μA ultra-low green mode operation current

Applications

- Switching AC/DC adaptor and battery charger
- Open frame switching power supply

Typical Application

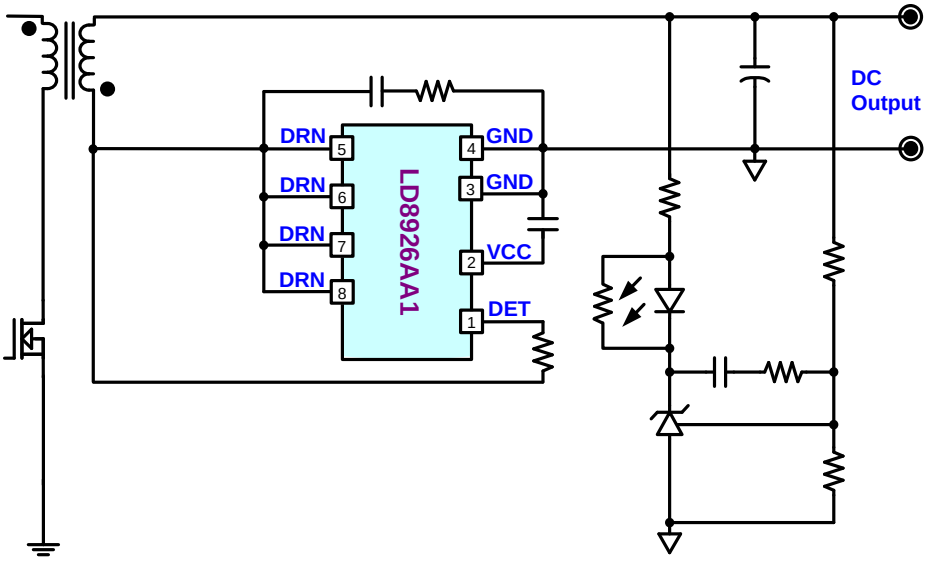


Fig. 1 Flyback Low Side Synchronous Rectification

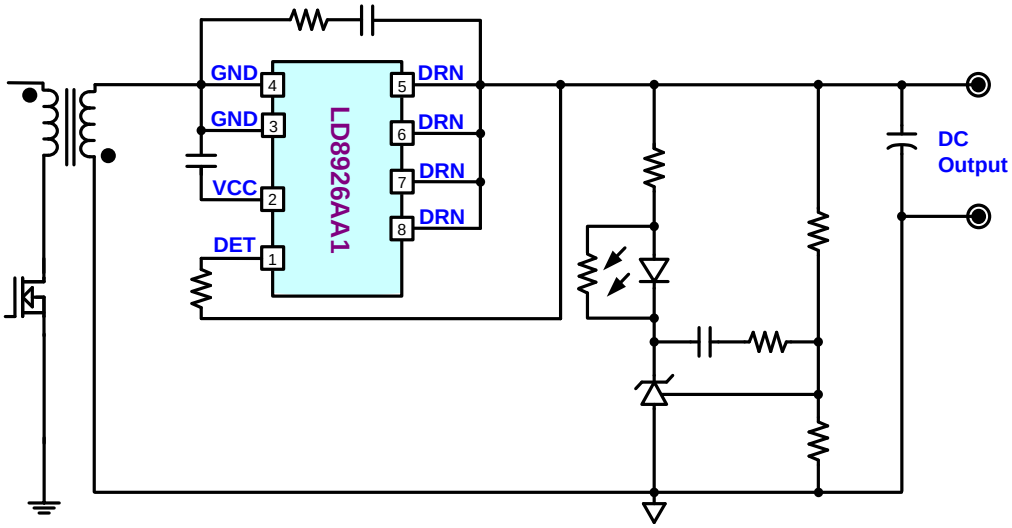


Fig. 2 Flyback High Side Synchronous Rectification

Pin Configuration

SOP-8 (TOP VIEW)

GS: SOP-8
YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package		Top Mark	Shipping
LD8926AA1 GS	SOP-8	Green Package	LD8926AA1	2500 / tape & reel

The LD8926AA1 is ROHS compliant/ green packaged.

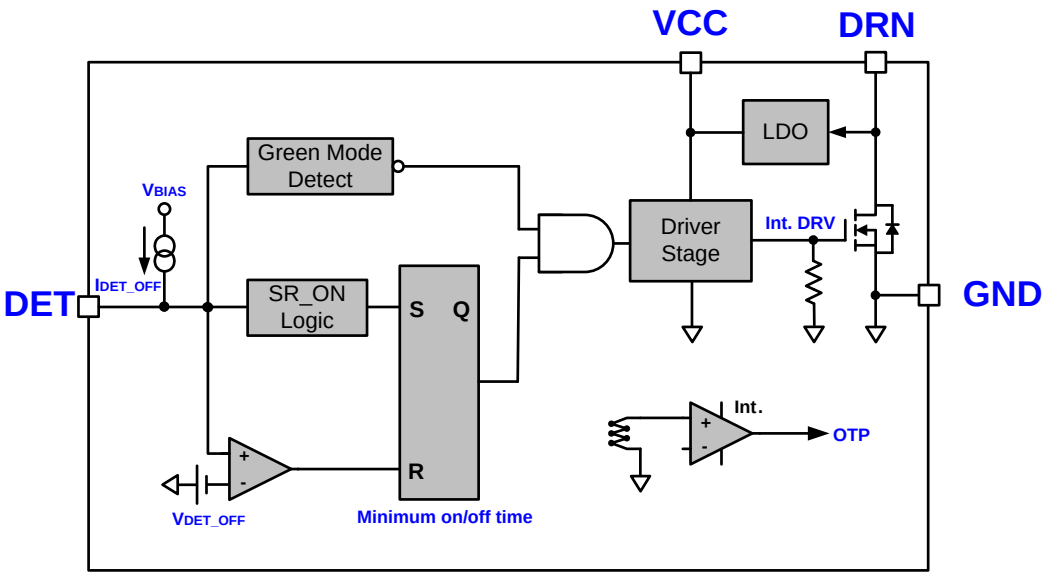
Protection Mode

Part number	Int. OTP
LD8926AA1	Auto-Restart

Pin Description

PIN	NAME	FUNCTION
1	DET	Synchronous rectification detection
2	VCC	Supply voltage pin
3~4	GND	Ground pin
5~8	DRN	MOS Drain Pin

Block Diagram



Absolute Maximum Ratings

DET	-1V ~ 200V
DRN	-0.3V ~ 100V
VCC	-0.3V ~ 7V
DRN Continuous Current (at T_C=25°C/100°C)	25A / 15A
DRN Peak Current @ T=100us (at T_C=25°C/100°C)	45A / 25A
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8, θ_{JA})	106°C/W
Package Thermal Resistance (SOP-8, θ_{JC})	20°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	377mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (VCC)	2.5KV
ESD Voltage Protection, Human Body Model (DET)	1KV
ESD Voltage Protection, Human Body Model (DRN)	2.5KV
ESD Voltage Protection, Machine Model	250V

*Note1: The value of θ_{JA} is measured with the device mounted on 1 inch^2 FR-4 board with 2oz. Copper, in a still air environment (Forced heat conduction K=3W/mK) with T_A =25°C. The value in any given application depends on the user's specific board design.

Caution:

Stresses beyond the ratings specified in “absolute maximum ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply Voltage VCC	3	6	V
Operating Frequency		130	KHz
VCC capacitor	2.2		μF
RDET		600	Ω

Notes:

1. When MOSFET Ciss is the maximum value, turn-off R_{GATE} must be the minimum value. On the contrary, when MOSFET Ciss is the minimum, turn-off R_{GATE} must be the maximum.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=5V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
MOSFET drain (DRN Pin)						
Drain-Source Breakdown Voltage	I_{DS}=500μA	BV_{DS}	100	110		V
Drain to Source On Resistance	I_{DS}=6A; V_{GS}=4.5V	R_{DS_ON}		12	16	mΩ
Supply Voltage (VCC Pin)						
VCC UVLO (on)		V_{CC_ON}	2.8	3	3.2	V
VCC UVLO (off)		V_{CC_OFF}		2.8		V
UVLO Hysteresis		V_{CC_HYS}		0.2		V
Operating Current	VCC=5V, DET=65kHz	I_{VCC_OP1}		2	2.9	mA
	Green mode	I_{VCC_OP2}		200	250	μA
Operating Current	UVLO_OFF mode(option) VCC=2.5v	I_{VCC_OFF}		25		μA
Detection Reference (DET Pin)						
Turn-on voltage		V_{DET_ON}	-400	-300	-150	mV
Turn-off voltage	(2)	V_{DET_OFF}	10	20	30	mV
Turn-off Compensation Current		I_{DET_OFF}	85	100	115	μA
Ring Reject Threshold		V_{DET_R}	1.3	1.6	1.8	V
Ring Reject Threshold Hysteresis		V_{DET_RHY}		1.1		V
Ring Reject Window		T_{DET_WD}	50	70	100	ns
Leakage Current	V_{DET}=200V	I_{DET_LK}			10	μA
Max. Operating Limit	(1)	F_{SW_MAX}	150	180	230	kHz
On Chip OTP (Over Temperature) Auto-Recovery						
OTP Level	(1)	T_{OTP}		150		°C
OTP Hysteresis	(1)	T_{OTP_HYS}		30		°C

Notes:

1. Guaranteed by design.
2. For avoiding SR being too late to turn off in CCM, R_{DET} must be adjusted from 600R down to appropriate value.

Typical Performance Characteristics

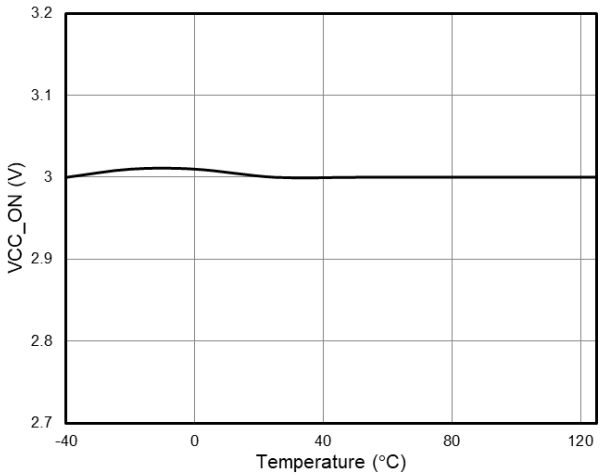


Fig. 3 UVLO ON vs. Temperature

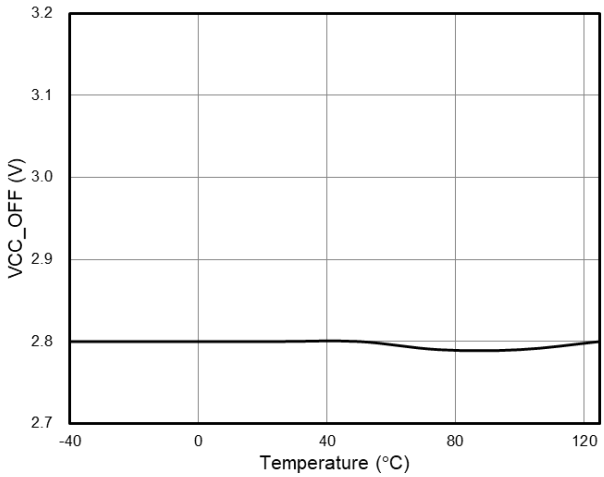


Fig. 4 UVLO OFF vs. Temperature

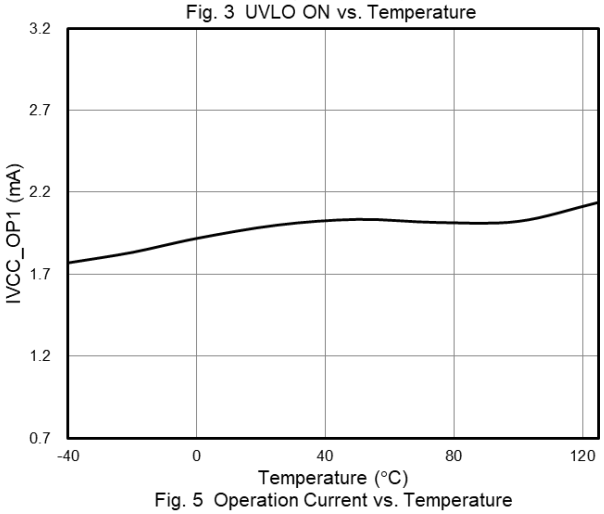


Fig. 5 Operation Current vs. Temperature

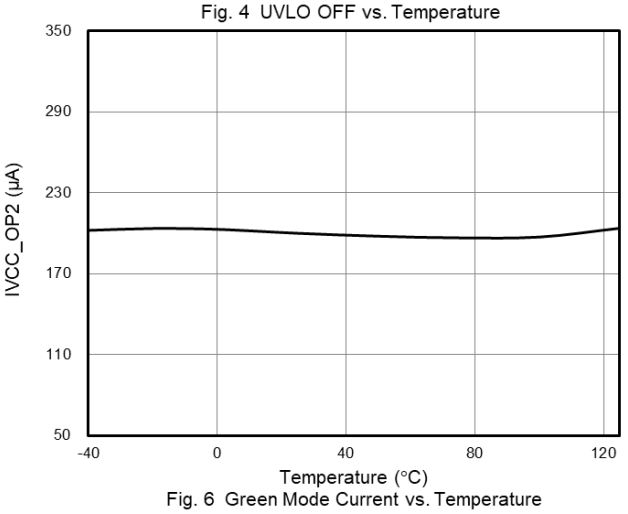


Fig. 6 Green Mode Current vs. Temperature

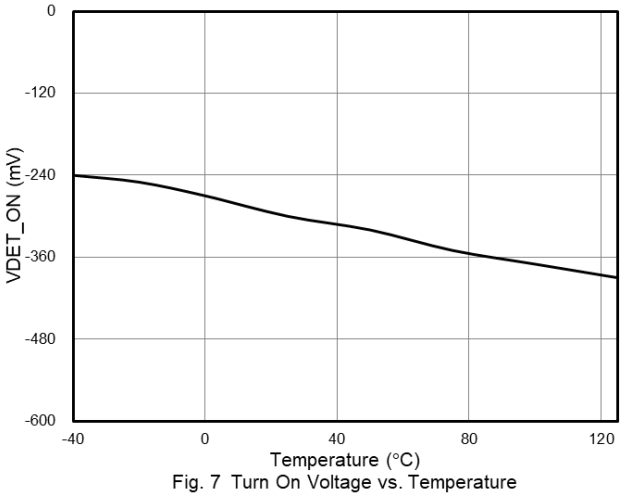


Fig. 7 Turn On Voltage vs. Temperature

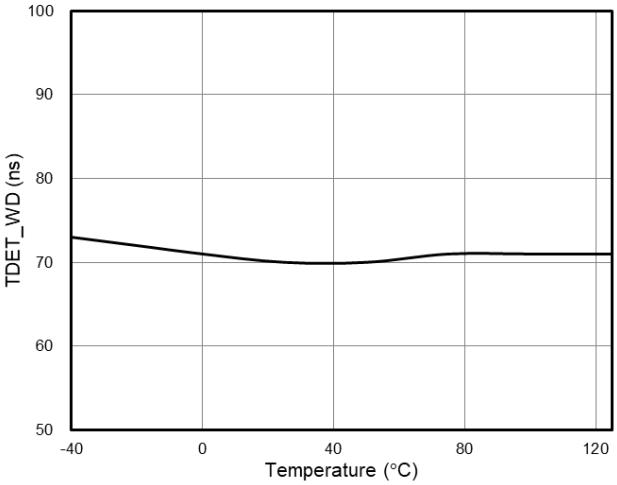


Fig. 8 Ring Reject Window vs. Temperature

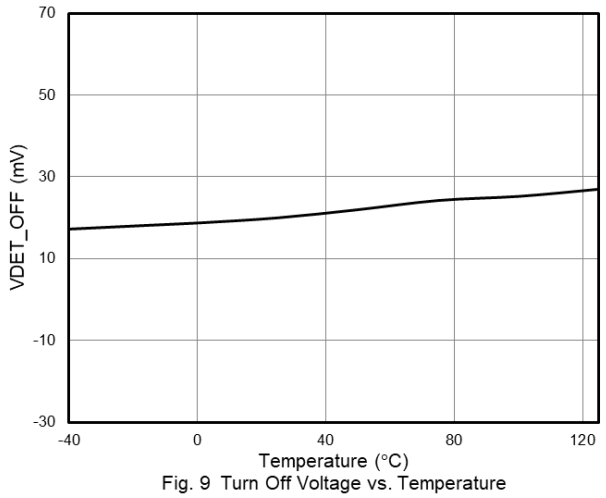


Fig. 9 Turn Off Voltage vs. Temperature

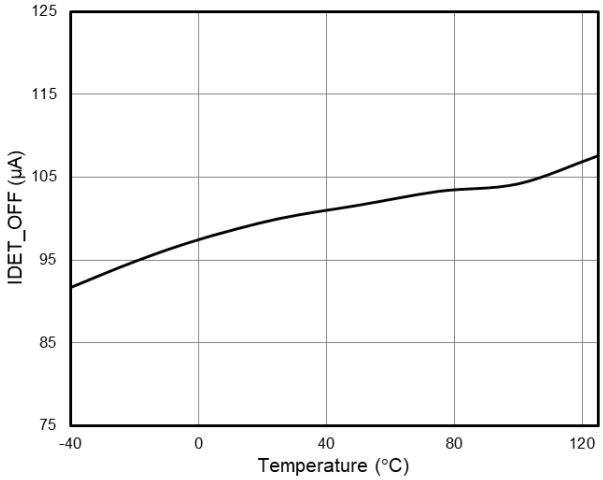


Fig. 10 Turn Ooff Compensation Current vs. Temperature

Application Information

Operation Overview

The LD8926AA1 is a secondary side synchronous rectification driver IC for CCM and DCM operation. The LD8926AA1 not only has excellent dead time control function for safety in load transient, but also only needs very low operation current in green mode. In addition, LD8926AA1 can generate its own supply voltage through low output voltage or high side rectification applications to charge battery. Hence, LD8926AA1 is suitable for PD application.

To reduce assembly process, layout area, and production cost, SR MOSFET and LD8926AA1 control core are packaged in SOP-8.

LDO Charge Function

No matter LD8926AA1 is applied in high side or low side, there is a LDO (low drop-out regulator) used to provide VCC power, and a capacitor must exist from VCC to GND to store the energy.

Under Voltage Lockout (UVLO) and Enable Function

An UVLO comparator is implemented to detect the voltage on the VCC pin. It will assure the supply voltage enough to turn on the LD8926AA1 controllers and further to drive the synchronous rectifier. As shown in Fig. 11, the UVLO(ON) and UVLO(OFF) are 3V and 2.8V respectively.

To enable synchronous rectifier, the following conditions must be met:

1. VCC > UVLO(ON)
2. Exit green mode
3. DET > V_{DET_ON}

With these restrictions, synchronous rectifier always operates in stable condition. Therefore, some unstable transient, which are like turn-on, turn-off, output short, surge, ESD…etc., will not make synchronous rectifier unsafe when it works.

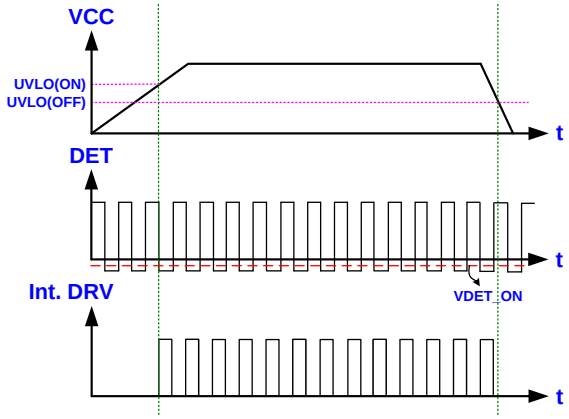


Fig. 11

Green Mode Operation

For improving the efficiency in light load conditions, LD8926AA1 stops SR MOSFET driving function to reduce operation current, as shown in Fig. 12.

DET pin detects system behavior, and the internal logic circuit sets Int. DRV to high or low. Hence, LD8926AA1 can enter/exit green mode normally, even under dynamic load.

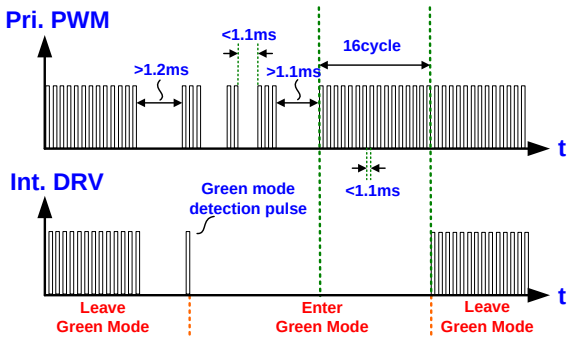


Fig. 12

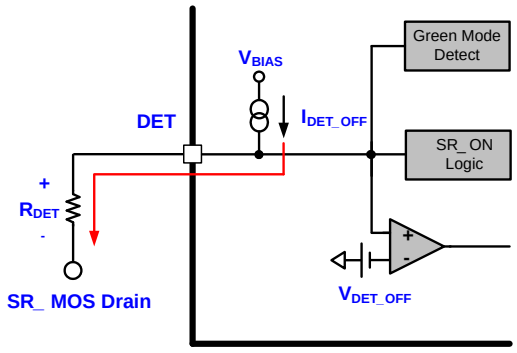


Fig. 13

Turn-on Phase

After a negative voltage (-300 mV typical) is sensed on the DET pin, the driver output voltage (Int. DRV, see Block Diagram) is made high and the internal MOSFET is switched on. After switch-on of the SR MOSFET, the input signal on the DET pin is blanked for 1.5μs (typical). This will eliminate false switch-off due to high frequency ringing at the start of the secondary stroke.

Turn-off Phase

The DET pin has detection gate on time to do prediction gate pre-drop method (T_{ON} x 0.5 = $T_{PREDICT}$), and adjusting V_{DS} decreases gate driver voltage to 4V (typical).

As soon as the DET voltage is above VDET_OFF, the driver output is pulled to ground. For avoiding SR being too late to turn off in CCM, the following condition must be met, as shown in Fig. 13.

$$V_{DET\_OFF} - I_{DET\_OFF} \times R_{DET} + X = -10mV$$

Where I_{DET_OFF} = 100μA, V_{DET_OFF} = +20mV, X= thermal effect and parasitic inductance from trace & electronic components. Hence R_{DET} must be from 600Ω down to find the appropriate turn-off time.

The behavior of Int. DRV in DCM & CCM are shown separately in Fig. 14.

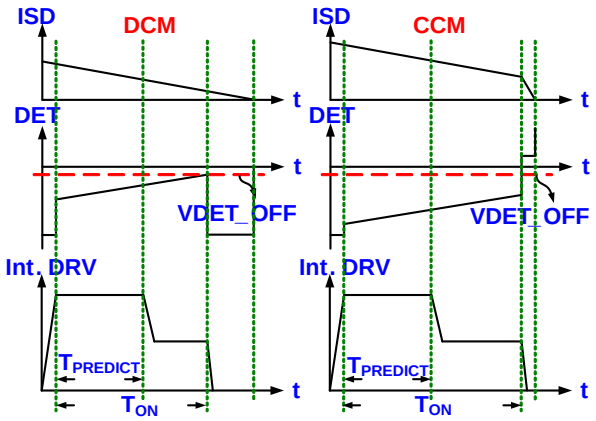


Fig. 14

On-Chip OTP - Auto Recovery

An internal OTP circuit is embedded inside the LD8926AA1 to provide the worst-case protection for this controller. When the chip temperature rises and is higher than the OTP trip level, the output will be disabled until the chip is cooled down below the hysteresis window.

Recommended Layout Guide

In order for the system to work properly, layout must pay attention to the following points:

1. Keep the DET and GND loops as small as possible.

2. The power loop needs to be separated from the DET detection loop.

3. Place VCC capacitor as close to IC as possible.

4. Keep the GND of IC and the source pin of MOS as short as possible.

5. To let MOS be turned OFF in time, keep 5nH~20nH inductance of PCB trace as shown in Fig.15 & Fig. 16 in red lines. The suggested trace configurations are listed below:

a. 3.5mm*18mm*2oz

b. 4mm*20mm*2oz

c. 3.5mm*9mm*1oz

d. 4mm*10mm*1oz

e. 6mm*15mm*1oz

In high side application, DET detection point needs to be close to the output capacitor, and in low side application, DET detection point needs to be close to the transformer.

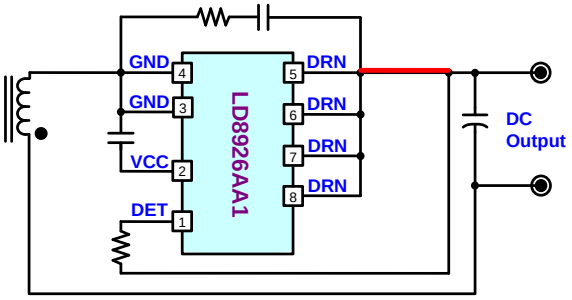


Fig. 15

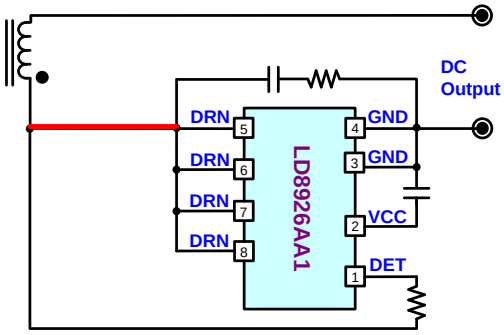
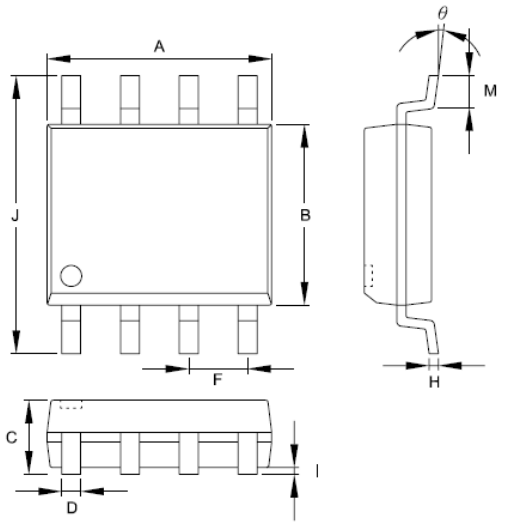


Fig. 16

Package Information

SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

REV.	Date	Change Notice
00	06/14/2019	Original Specification