Green-Mode PWM Controller with Frequency Swapping with protections and MOSFET Integrated

REV. 00

General Description

The LD9704R is built-in with several functions, protection and EMI-improved solution within a 680V MOSFET in a DIP-6 package. It takes less components counts or circuit space, especially ideal for those total solutions of low cost.

The implemented functions include low startup current, green-mode power-saving operation and internal slope compensation. It also features more protections like OLP (Over Load Protection) and OVP (Over Voltage Protection) to prevent circuit damage occurred under abnormal conditions.

Furthermore, the Frequency Swapping function can reduce the noise level and thus help the power circuit designers to easily deal with the EMI filter design by spending minimum amount of component cost and developing time.

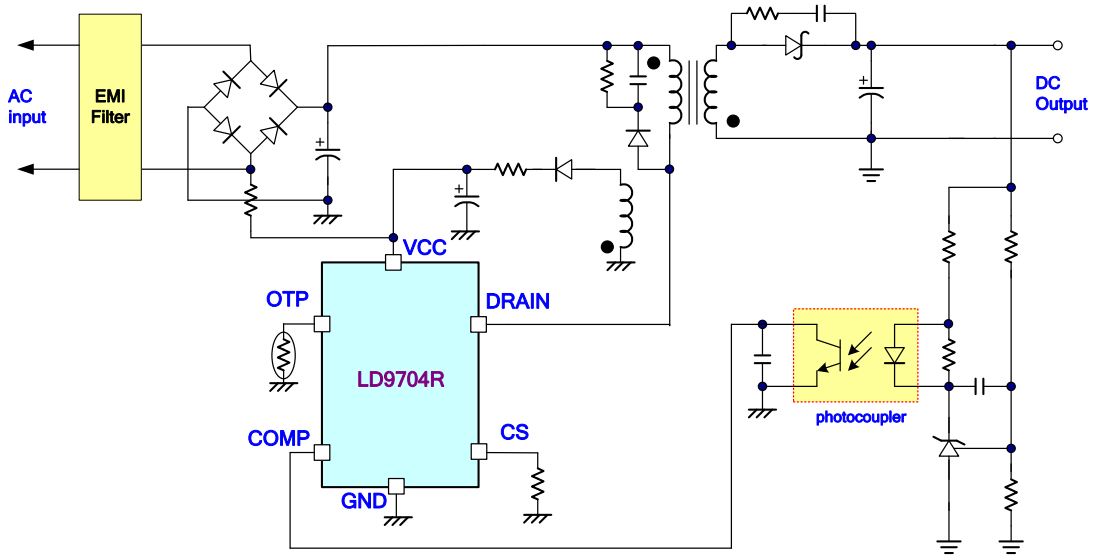
Features

- Built-in 680V Power MOSFET
- Fixed Switching Frequency at 130KHz
- Very Low Startup Current (<3μA)
- Current Mode Control
- Green Mode Control
- UVLO (Under Voltage Lockout)
- Internal Frequency Swapping, Slope Compensation
- OVP (Over Voltage Protection) on VCC Pin
- Built in OCP(Over Current Protection) Compensation
- OTP (Over Temperature Protection) through a NTC
- OLP (Over Load Protection)

Applications

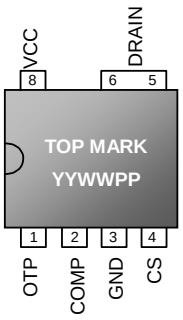
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

Typical Application



Pin Configuration

DIP-6 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package	Top Mark	Shipping
LD9704RGP7	DIP-6	LD9704RGP7	3600 /tube /Carton

The LD9704R is ROHS compliant / Green Packaged

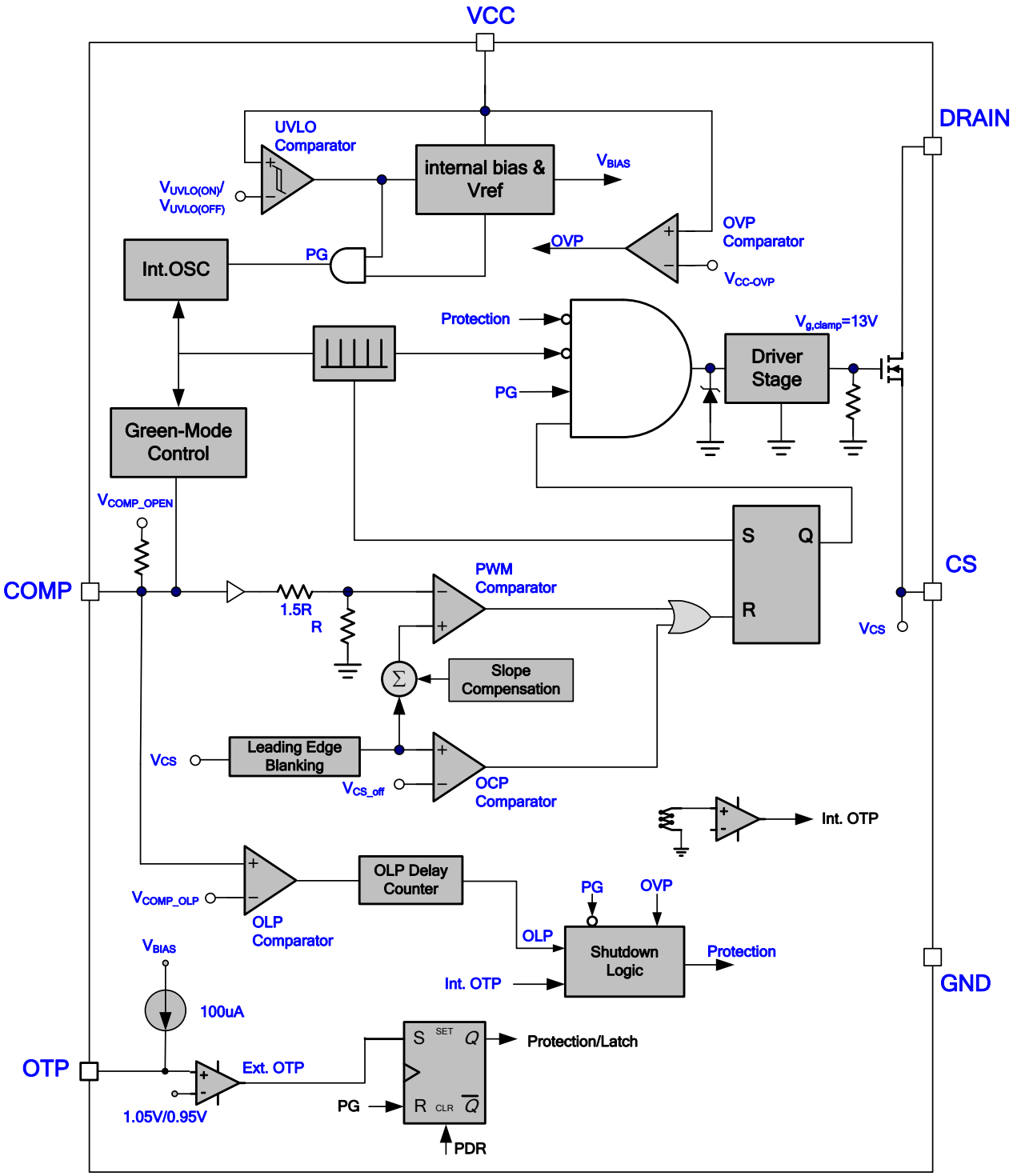
Protection Mode

Switching Freq.	OLP	VCC OVP	OTP Pin	Output Short
130kHz	Auto recovery	Auto recovery	Latch	Auto-restart by OLP

Pin Descriptions

DIP-6	NAME	FUNCTION
1	OTP	Pull this pin below 0.95V to shut down the controller into latch mode until the AC resumes power-on. Connecting this pin to ground with NTC will achieve OTP protection. Let this pin float or connect a 100kΩ resistor to disable the latch protection.
2	COMP	Voltage feedback pin. Connect a photo-coupler to close the control loop and achieve the regulation.
3	GND	Ground
4	CS	Source terminal of the internal power MOSFET and Current sense pin
5,6	DRAIN	Drain terminal of the internal power MOSFET
7	NC	NC
8	VCC	Supply voltage pin

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V ~ 30V
COMP, CS, OTP	-0.3V ~ 6V
DRAIN	-0.3V ~ 680V
Avalanche Energy (L=10mH, IAS=3A) on absolute maximum rating)	45mJ
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (DIP-6/7, θ_{JA})	80°C/W
Package Thermal Resistance (DIP-6/7, θ_{Jc})	30°C/W
Power Dissipation (DIP-6/7, at Ambient Temperature = 25°C)	1250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (DRAIN pin is exclusive)	2.5 KV
ESD Voltage Protection, Machine Model (DRAIN pin is exclusive)	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.5	26.5	V
VCC Capacitor	4.7	10	μF
Start-up resistor Value (AC Side, Half Wave)	750K	2.4M	Ω
COMP Pin Capacitor	1	10	nF
Current Sense Impedance	0.52	-	Ω
Snubber Capacitor between Drain and CS pin	-	100	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF ~ 0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. It's also essential to connect a capacitor to COMP to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYM.	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current	VCC < UVLO(ON)	I_{CC_ST}		1.5	3	μA
Operating Current (with 1nF load on DRAIN pin)	V_{COMP}=3V	I_{CC_OP1}		2.5	3.5	mA
	V_{COMP}=0V	I_{CC_OP2}		0.35	0.5	mA
	OLP/OVP Tripped / Auto	I_{CC_OPA}		600		μA
	*; OTP Pin Tripped / Latch, VCC=7V	I_{CC_OPL1}		430	500	μA
	OTP Pin Tripped / Latch VCC=5V	I_{CC_OPL2}		40	60	μA
Latch-Off Release Voltage		V_{CC_PDR}	3.6	4.5	5.2	V
UVLO(OFF)	OUT OFF	V_{CC_OFF}	7.0	7.5	8.0	V
UVLO(ON)		V_{CC_ON}	15	16	17	V
VCC OVP Level		V_{CC_OVP}		28.5		V
VCC OVP De-bounce time*		T_{D_VCCOVP}		8		cycle
Voltage Feedback (Comp Pin)						
Short Circuit Current	V_{COMP}=0V	I_{COMP}		0.125		mA
Open Loop Voltage	COMP pin open	V_{COMP_OPEN}	2.75	3	3.25	V
Normal Mode Threshold	*; COMP pin	V_N		1.2		V
Green Mode Threshold	*; COMP pin	V_G		1		V
Zero Duty Threshold VCOMP		V_{ZDC}		0.6		V
Zero Duty Hysteresis		V_{ZDCH}		100		mV
Current Sensing (CS pin)						
Maximum Input Voltage, V_{S_OFF}	*;Duty=50%	$V_{CS\_50\%}$		0.60		V
Maximum Input Voltage, V_{S_OFF}	Duty=25%	$V_{CS\_25\%}$		0.50		V
Min. on Time	*	T_{LEB}		400		ns
Internal Limited Vcs level	*; When V_{CS}>$V_{cs,limit}$, gate off immediately	V_{CS_LIMIT}		1.2		V
Internal Slope Compensation*	*; 0% to D_{MAX}. (Linearly increase)	V_{SLP_L}		300		mV
Input impedance	*	Z_{CS}	1			MΩ
Delay to Output	*	T_{PD}		100		ns
Soft Start Duration	*	T_{SS}		7		ms

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYM.	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency						
Frequency, FREQ		F_{SW}	120	130	140	kHz
Green Mode Frequency, FREQG		F_{SW_GREEN}		28		kHz
Frequency Swapping	V_{COMP}>2.575V	F_{SW_MOD}		± 6		%
Temp. Stability*	*	F_{SW_TS}	0	5		%
Voltage Stability*	*; (VCC=11V-25V)	F_{SW_VS}	0	1		%
Max. Duty		MXD		80		%
OLP (Over Load Protection)						
OLP Trip Level		V_{COMP_OLP}		2.6		V
OLP Delay Time at start-up*	OLP + Soft start	T_{D_OLPSS}		71.5		ms
OTP Pin Latch Protection (OTP Pin)						
OTP Pin Source Current		I_{OTP}	90	100	110	μA
OTP Turn-On Trip Level		V_{OTP_ON}	1.0	1.05	1.1	V
OTP Turn-Off Trip Level		V_{OTP_OFF}	0.9	0.95	1.0	V
OTP Turn-Off Trip Resistance	*; V_{OTP_OFF}/I_{OTP}	R_{OTP}		9.5		kΩ
OTP pin de-bounce time	V_{COMP} > 3V	T_{D_OTP}		500		μs
Internal OTP Protection						
OTP Level	*	T_{UP_OTP}		140		℃
OTP Hysteresis	*	T_{INOTP_HYS}		15		℃

Electrical Characteristics for MOSFET

(T_A = +25°C)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage						
Breakdown Voltage BV_{DSS}	Vcc=0V,COMP=0V, I_D=250μA	BV_{DSS}	680			V
Drain Current						
Continuous Drain Current	*; Vcc=15V,COMP=2V	I_D			3	A
Drain on Resistance						
D to S pin On-Resistance	I_D=1.5A;V_{CC}=15V;	R_{DSON}		2.4	2.8	Ω

*: Guaranteed by design.

Typical Performance Characteristics

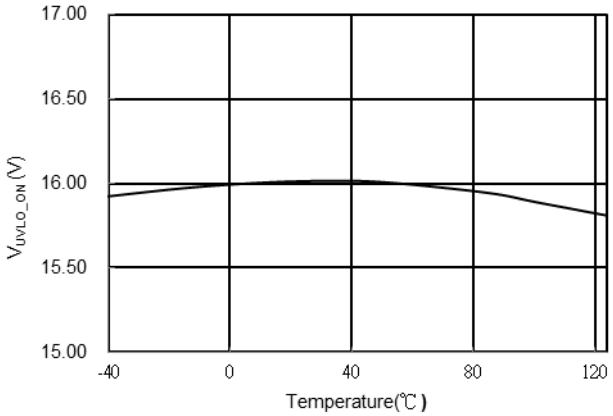


Fig. 1 V_{UVLO_ON} vs. Temperature

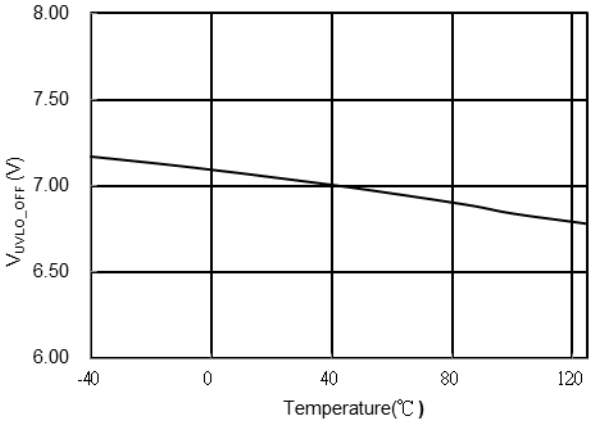


Fig. 2 V_{UVLO_OFF} vs. Temperature

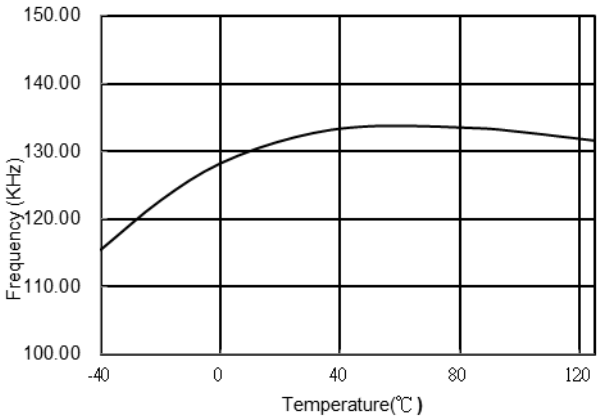


Fig. 3 Frequency vs. Temperature

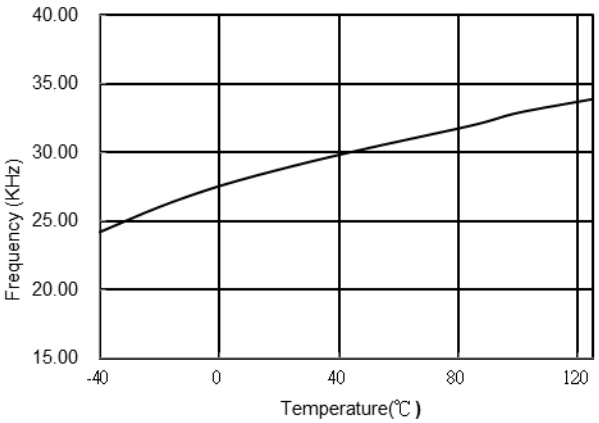


Fig. 4 Green Mode Frequency vs. Temperature

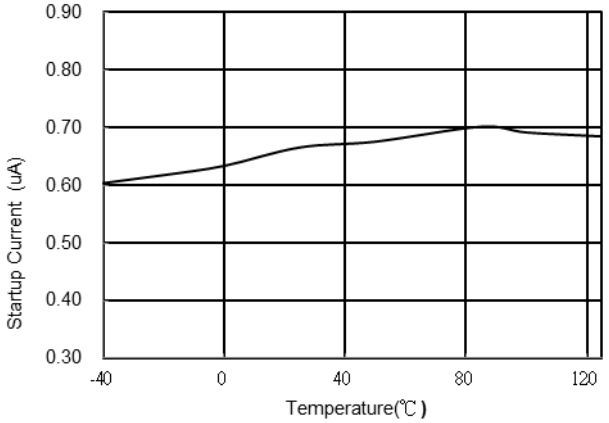


Fig. 5 Startup Current vs. Temperature

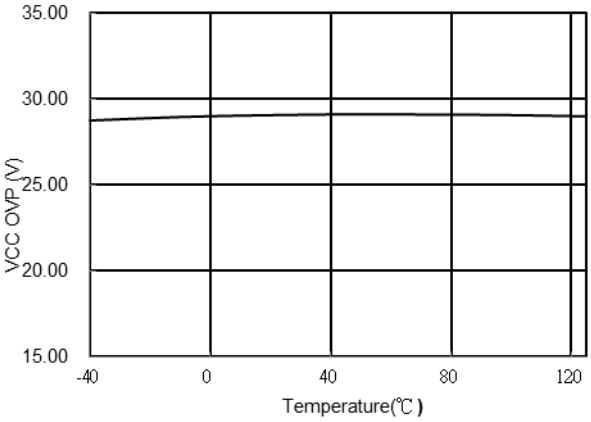


Fig. 6 VCC OVP vs. Temperature

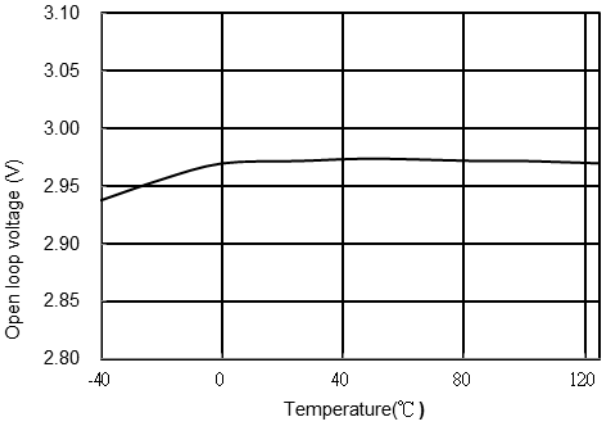


Fig. 7 Open loop voltage vs. Temperature

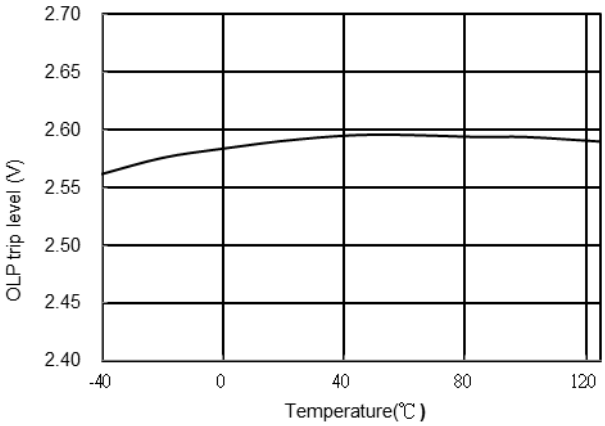


Fig. 8 OLP trip level vs. Temperature

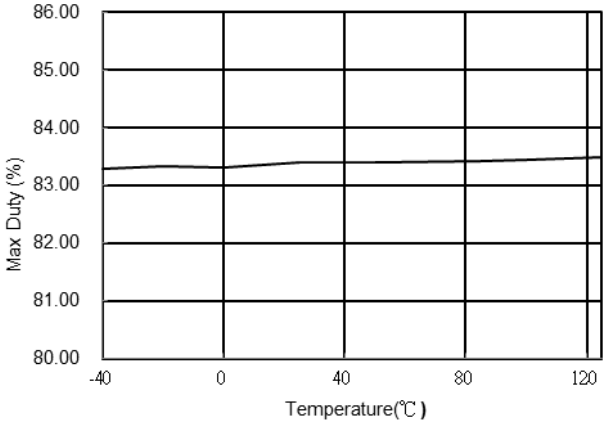


Fig. 9 Max Duty vs. Temperature

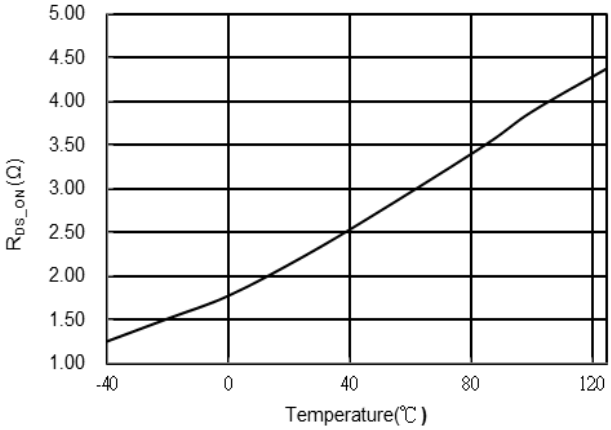


Fig. 10 R_{DS_ON} vs. Temperature

Application Information

Operation Overview

The L9704R meets the green-power requirement with a 680V MOSFET driver and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD9704R PWM controller and further to drive the power MOSFET. As shown in Fig. 11, a hysteresis is built in to prevent the shutdown from the voltage dip during startup.

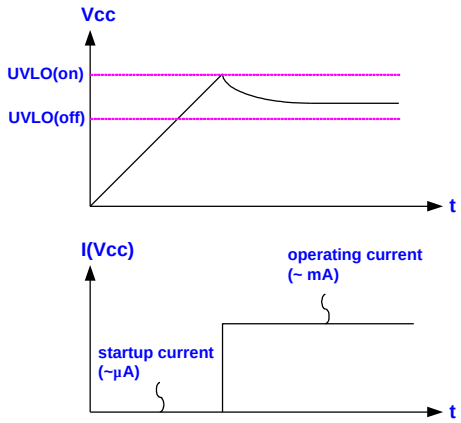


Fig. 11

Startup Current and Startup Circuit

The typical startup circuit to generate VCC of the LD9704R is shown in Fig. 12. During the startup transient, the VCC is below UVLO threshold. Before it has sufficient voltage to develop OUT pulse to operation, R1 will provide the startup current to charge the capacitor C1. Once VCC obtain enough voltage to turn on the LD9704R and it's working condition, it will enable the auxiliary winding of the transformer to provide supply current. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current for LD9704R is under 3μA.

If a higher resistance value of the R1 is chosen, it will usually take more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

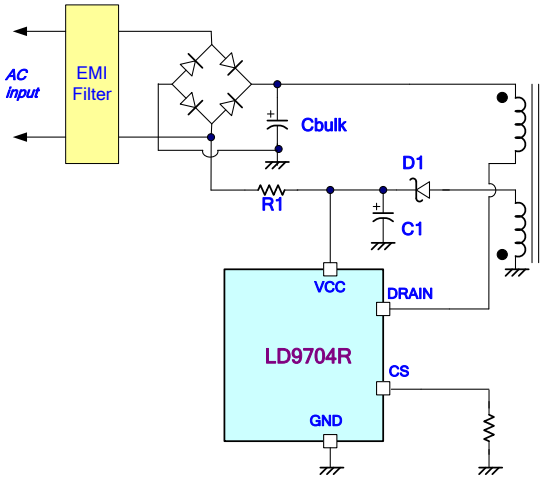


Fig. 12

Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD9704R detects the internal MOSFET current from the CS pin and pulse-by-pulse limited current. The maximum voltage threshold of the current sensing pin is Vcs_off.

Due to integrated leading edge blanking circuit and internal spike filter, the MOSFET peak current can be obtained from the equation as follows:

$$I_{PEAK(MAX)} = \frac{V_{CS\_OFF}}{R_S}$$

In general, the power MOSFET peak current is various in corresponding to AC input voltage. To compensate it, LD9704R will change the current limit Vcs_off with the duty cycles. Please refer to Fig. 13

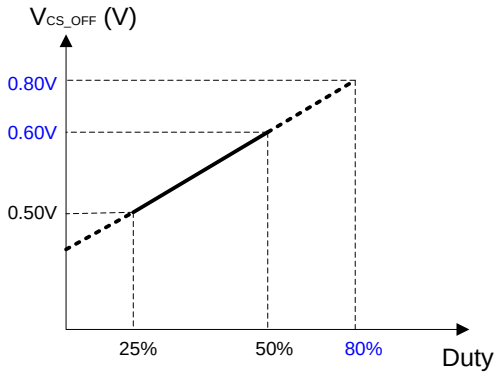


Fig. 13

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD9704R.it would carry a diode voltage offset at the stage to feed the voltage divider at the ratio, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{R}{1.5R + R} \times (V_{COMP})$$

A pull-high resistor is embedded internally and can be eliminated externally.

Oscillator and Switching Frequency

The LD9704R is implemented with Frequency Swapping function which helps the power supply designers to both optimize EMI performance and lower system cost. The switching frequency substantially centers at 130KHz, and swap between a range of ± 6KHz.

Green-Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property. Please refer to Fig. 14

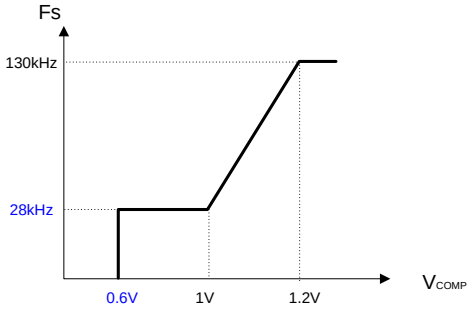


Fig. 14

On/Off Control

The LD9704R can be turned off by pulling COMP pin lower than 0.6V. The DRAIN pin of the LD9704R will be disabled immediately under such condition. The off-mode can be released when the pull-low signal is removed.

Internal Slope Compensation

In the conventional applications, the problem of the stability is a critical issue for current mode controlling,

when it operates over 50% duty-cycle. As UC384X, It takes slope compensation from injecting the ramp signal of the RT/CT pin through a coupling capacitor. It therefore requires no extra design for the LD9704R since it has integrated it already.

Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage in over-load condition and short or open-loop condition, the LD9704R is implemented with smart OLP function. It also features auto recovery function; see Fig. 15 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the V_{COMP} ramps up to the OLP threshold of 2.6V and continues over OLP delay time, the protection will

be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

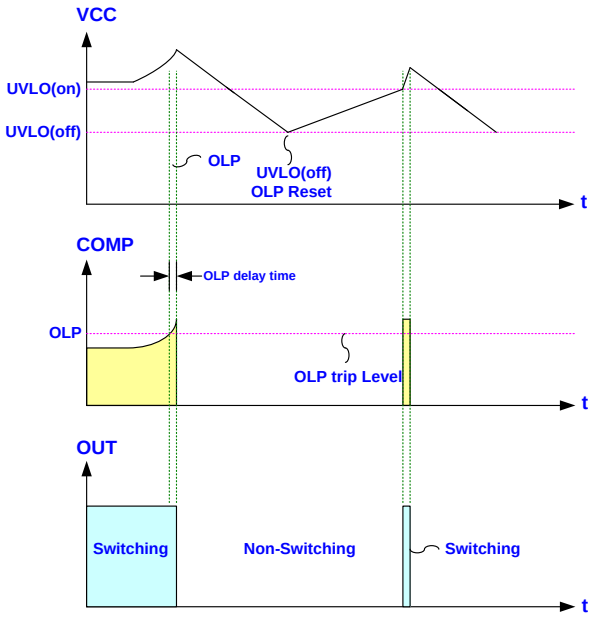


Fig. 15

Over Voltage Protection (OVP) on VCC - Auto Recovery

The Vcc OVP function of LD9704R is in auto recovery mode. As soon as the voltage of the Vcc pin rises above OVP threshold, the output gate drive circuit will be shutdown simultaneous to turn off the power MOSFET.

MOSFET Characteristic

The MOSFET is divided into three operation regions, ohmic region, saturation region, and the cut-off region, shown as Fig. 16.

For switching power supply applications, it shall operate in ohmic and cut-off region. Never reach the region of saturation; it would cause damage for acting beyond the maximum safety operating area. It's necessary to check the characteristic of MOSFET.

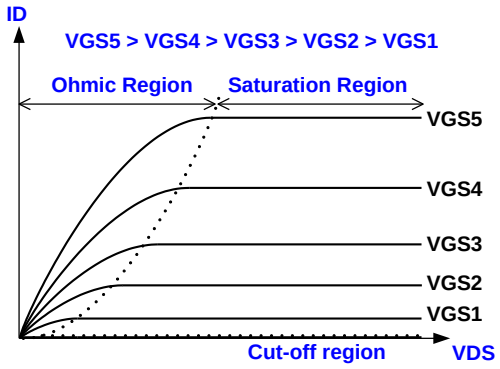


Fig. 16

OTP Pin --- Latched Mode Protection

The OTP circuit is implemented to sense whether there is any hot-spot of power circuit like power MOSFET or output rectifier. Once an over-temperature condition is detected, the OTP is enabled to shut down the controller to protect the controller. Typically, a NTC is recommended to connect with OTP pin.

The NTC resistance will decrease as the device or ambient in high temperature. The relationship is as below.

$$V_{OTP}=100\mu A \times R_{NTC}$$

When the VOTP is lower than the defined voltage threshold (typ. 0.95V), the LD9704R will shut down the gate output and latch off the power supply. There are 2 conditions required to restart it successfully. First, cool down the circuit so that NTC resistance will increase and raise V_{OTP} up above 1.05V. Then, remove the AC power cord and re-plug AC power.

Layout Guide

For PCB layout, please check spike on CS pin. This measurement method is between GND and CS pin to check positive and negative voltage. Suggest Vcs spike must be is under 0.2V at minimum load and 0.6V at full load after LEB time (~300nS). Moreover, Check negative voltage is not still lower than -2V in 200nS time continued.

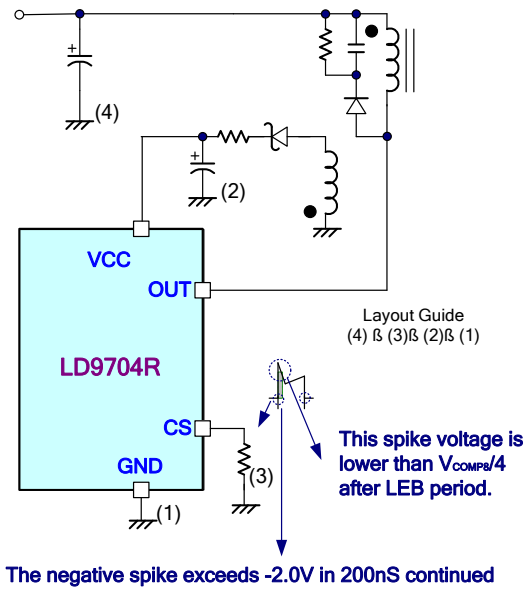
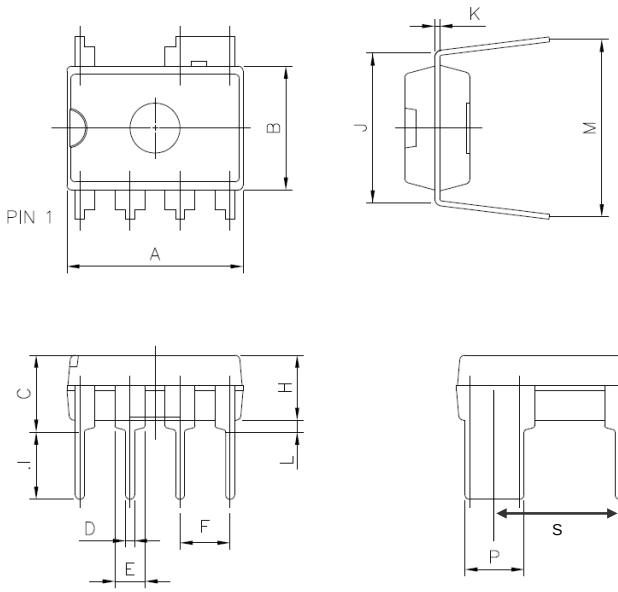

(4)
(2)
VCC
OUT
LD9704R
CS
GND
(3)
(1)
Layout Guide
(4) ß (3)ß (2)ß (1)
This spike voltage is lower than VCOMPB/4 after LEB period.
The negative spike exceeds -2.0V in 200nS continued

Fig. 17

Package Information

DIP-6



	Dimension in Millimeters		Dimensions in Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	9.017	10.160	0.355	0.400
B	6.100	6.600	0.240	0.260
C	3.300	4.320	0.130	0.170
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.480	2.600	0.098	0.102
H	3.170	3.600	0.125	0.142
I	2.921	3.810	0.115	0.150
J	7.366	7.874	0.290	0.310
K	0.246	0.305	0.010	0.012
L	0.381	0.540	0.015	0.021
M	7.493	8.255	0.295	0.325
P	2.920	3.100	0.115	0.122
S	6.273	6.427	0.247	0.253

Important Notice

Leadtrend Technology Inc. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	03/15/2017	Original Specification.