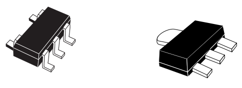
200 mA high accuracy and high PSRR voltage regulator



Maturity status link
LDK320

Features

- Input voltage from 2.5 to 18 V
- Very low-dropout voltage (100 mV typ. @ 100 mA load)
- Low quiescent current (typ. 60 µA, 1 µA in off mode)
- High PSRR: 88 dB @ 120 Hz
- Low noise
- Output voltage tolerance: ± 0.5% @ 25 °C (LDK320A) or ± 2% 25 °C
- Output current up to 200 mA
- Wide range of output voltages available on request: fixed from 1.2 V to 12 V with 100 mV step and adjustable
- Logic-controlled electronic shutdown
- Compatible with ceramic capacitor C_{OUT} = 1 µF
- Current, SOA and thermal protections
- Available in SOT23-5L and SOT-89 packages
- Temperature range: -40 °C to 125 °C

Applications

- DSC
- TV
- BD, DVD
- PC
- Industrial

Description

The LDK320 is a low drop voltage regulator, which provides a maximum output current of 200 mA from an input voltage in the range of 2.5 V to 18 V, with a typical dropout voltage of 100 mV.

It is stabilized with a ceramic capacitor on the output.

The very good dynamic characteristic, combined with low drop voltage and low quiescent current make it suitable for low power battery-powered applications.

The enable logic control function allows the LDK320 to be in shutdown mode by consuming a total current lower than 1 µA.

This device also includes a short-circuit current limiting, thermal and SOA protections.

1 Diagram

Figure 1. **Block diagram (fixed version)**

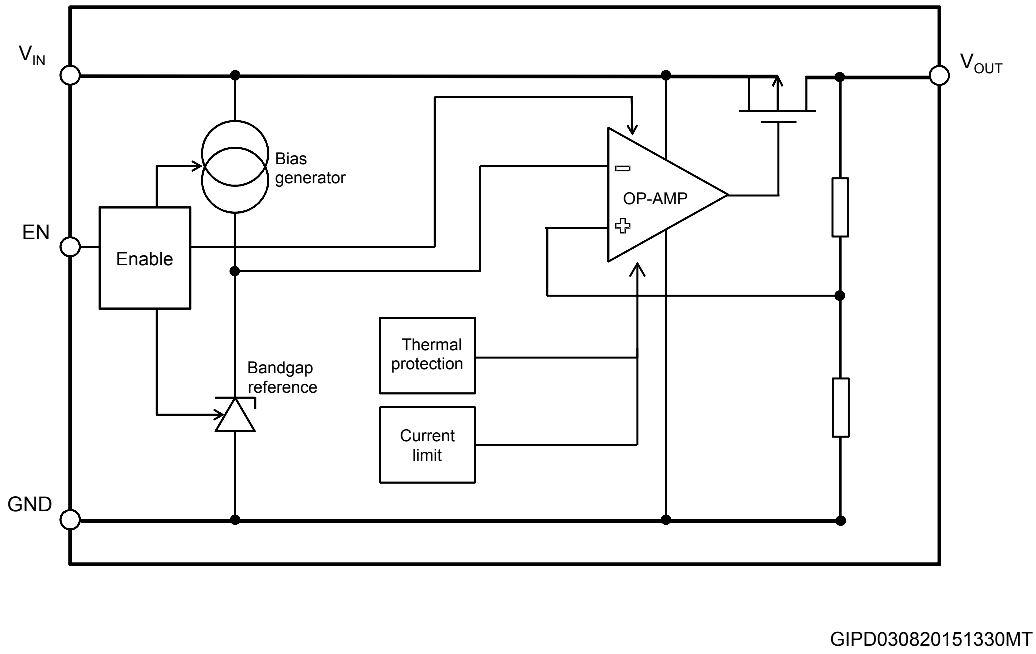
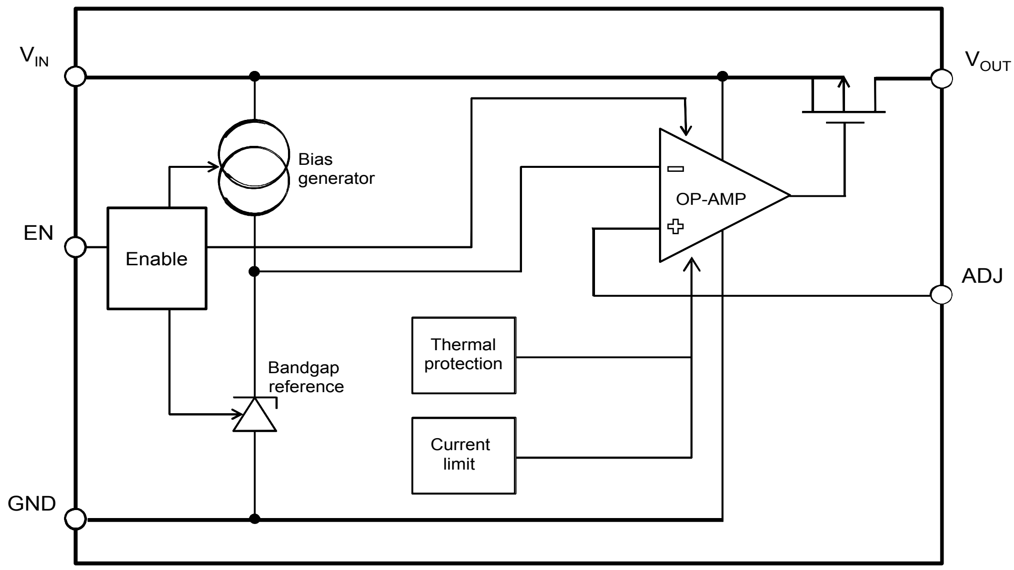


Figure 2. **Block diagram (adjustable version)**



2 Pin configuration

Figure 3. Pin connection (top view)

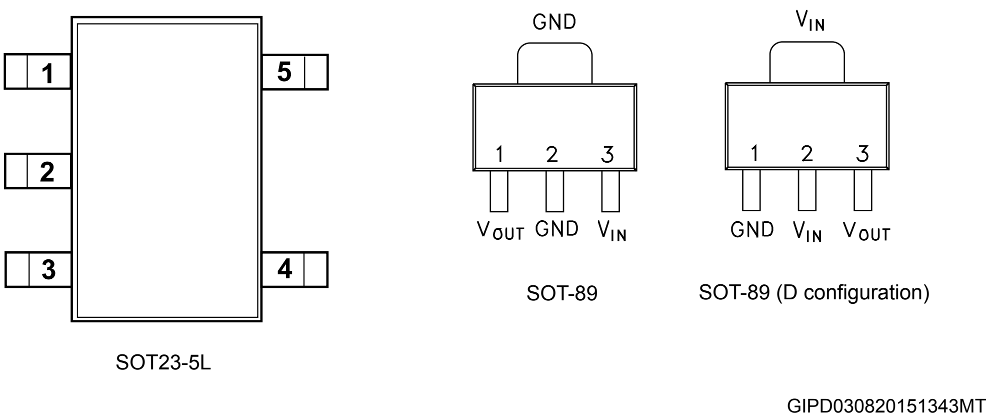


Table 1. Pin description (SOT23-5L)

Pin n°	Symbol	Function
1	IN	Input voltage of the LDO
2	GND	Common ground
3	EN	Enable pin logic input: low = shutdown, high = active
4	ADJ/NC	Adjustable pin on ADJ version, not connected on fixed version
5	OUT	Output voltage of the LDO

Table 2. Pin description (SOT-89)

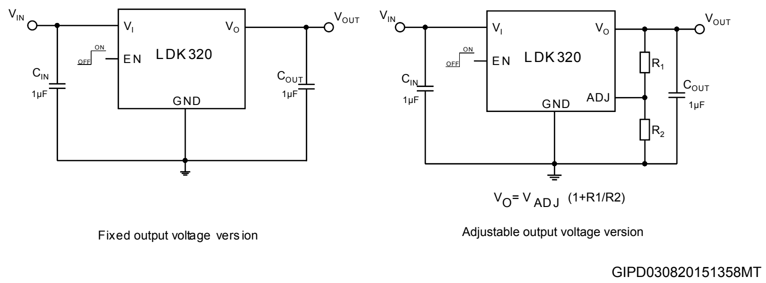
Pin n°	Symbol	Function
1	OUT	Output voltage of the LDO
2	GND	Common ground
3	IN	Input voltage of the LDO
TAB	GND	Common ground

Table 3. Pin description (SOT-89, D configuration)

Pin n°	Symbol	Function
1	GND	Common ground
2	IN	Input voltage of the LDO
3	OUT	Output voltage of the LDO
TAB	IN	Input voltage of the LDO

3 Typical application

Figure 4. **Typical application circuits**



Note: Adjustable version and enable pin are not available on SOT-89 package.

4 Maximum ratings

Table 4. Absolute maximun ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage	- 0.3 to 20	V
V_{OUT}	DC output voltage	- 0.3 to V_I + 0.3	V
V_{EN}	Enable input voltage	- 0.3 to V_I + 0.3	V
V_{ADJ}	ADJ pin voltage	- 0.3 to 2	V
I_{OUT}	Output current	Internally limited	mA
P_D (1)	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	- 65 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C

1. *Maximum power dissipation must be calculated by taking into account the package and thermal performance.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 5. Thermal data

Symbol	Parameter	SOT23-5L	SOT-89	Unit
R_{thJA}	Thermal resistance junction-ambient	160	110	°C/W
R_{thJC}	Thermal resistance junction-case	68	15	°C/W

5 Electrical characteristics

T_J = 25 °C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 1 mA, V_{EN} = V_{IN}, unless otherwise specified.

Table 6. LDK320 electrical characteristics (fixed output version)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		2.5		18	V
V_{OUT}	V_{OUT} accuracy	T_J = 25 °C	-2		2	%
		-40 °C < T_J < 125 °C	-3		3	%
	V_{OUT} accuracy, LDK320A	T_J = 25 °C	-0.5		0.5	%
		-40 °C < T_J < 125 °C	-1.5		1.5	%
ΔV_{OUT}	Static line regulation	V_{OUT} +1 V ≤ V_{IN} ≤ 18 V		0.001	0.05	%/V
ΔV_{OUT}	Static load regulation (SOT23-5L)	I_{OUT} = 1 mA to 200 mA, V_{OUT} ≤ 2 V		10	15	mV
		I_{OUT} = 1 mA to 200 mA, V_{OUT} > 2 V		0.001	0.003	%/mA
ΔV_{OUT}	Static load regulation (SOT-89)	I_{OUT} = 1 mA to 200 mA, V_{OUT} ≤ 2 V		10	25	mV
		I_{OUT} = 1 mA to 200 mA, V_{OUT} > 2 V		0.001	0.004	%/mA
V_{DROP}	Dropout voltage (1)	I_{OUT} = 100 mA, V_{OUT} = 3.3 V		100		
		I_{OUT} = 200 mA, V_{OUT} = 3.3 V -40 °C < T_J < 125 °C		200	350	mV
e_N	Output noise voltage	10 Hz to 100 kHz, I_{OUT} = 10 mA		63		$\mu V_{RMS}/V$
SVR	Supply voltage rejection	f = 120 Hz, I_{OUT} = 10 mA, V_{OUT} = 3.3 V		88		dB
		f = 1 kHz I_{OUT} = 10 mA, V_{OUT} = 3.3 V		65		
		f = 10 kHz, I_{OUT}= 10 mA V_{OUT} = 3.3 V		48		
I_Q	Quiescent current	V_{OUT} +1 V V_{IN} 18 V, I_{OUT} = 0 mA, -40 °C < T_J < 125 °C		60	90	µA
		V_{IN} = V_{OUT} +1 V I_{OUT} = 200 mA, -40 °C < T_J < 125 °C		70	100	
		V_{IN} input current in OFF mode: V_{EN} = G_{ND} T_J = 25 °C		0.2	1	
I_{SC}	Short-circuit current	R_L = 0		330		mA
		R_L = 0, V_{IN} = 16 V		200		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{EN}	Enable input logic low	V_{IN} = 2.5 V to 18 V, -40 °C < T_J < 125 °C			0.4	V
	Enable input logic high	V_{IN} = 2.5 V to 18 V, -40 °C < T_J < 125 °C	1.2			
I_{EN}	Enable pin input current	V_{EN} = V_{IN}		0.1	100	nA
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance (see Section 6: Typical characteristics)	1		22	µF

1. *Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.*

T_J = 25 °C, V_{IN} = 2.5 V, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 1 mA, V_{EN} = V_{IN}, unless otherwise specified.

Table 7. LDK320 electrical characteristics (ADJ version)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		2.5		18	V
V_{ADJ}	Adjustable voltage	T_J = 25 °C		1.185		V
	Adjustable voltage accuracy	T_J = 25 °C	-2		+2	%
		-40 °C < T_J < 125 °C	-3		+3	
	Adjustable voltage, LDK320A	T_J = 25 °C		1.2		V
	Adjustable voltage accuracy, LDK320A	T_J = 25 °C	-0.5		+0.5	%
		-40 °C < T_J < 125 °C	-1.5		+1.5	
ΔV_{OUT}	Static line regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 18 V		0.001	0.05	%/V
ΔV_{OUT}	Static load regulation	I_{OUT} = 1 mA to 200 mA		0.0002	0.003	%/mA
V_{DROP}	Dropout voltage (1)	I_{OUT} = 100 mA, V_{OUT} = 3.3 V		100		mV
		I_{OUT} = 200 mA, V_{OUT} = 3.3 V -40 °C < T_J < 125 °C		200	350	
e_N	Output noise voltage	10 Hz to 100 kHz I_{OUT} = 10 mA		60		μV_{RMS}
I_{ADJ}	Adjust pin current				1	µA
SVR	Supply voltage rejection	f = 120 Hz I_{OUT} = 10 mA, V_{OUT} = V_{ADJ}		83		dB
		f = 1 kHz I_{OUT} = 10 mA, V_{OUT} = V_{ADJ}		73		
		f = 10 kHz I_{OUT} = 10 mA, V_{OUT} = V_{ADJ}		58		
I_Q	Quiescent current	V_{OUT} +1 V ≤ V_{IN} ≤ 18 V, I_{OUT} = 0 mA, -40 °C < T_J < 125 °C		50	90	µA
		V_{IN} = V_{OUT} + 1 V, I_{OUT} = 200 mA, -40 °C < T_J < 125 °C		60	100	
		V_{IN} input current in OFF mode: V_{EN} = GND, T_J = 25 °C		0.2	1	
I_{SC}	Short-circuit current	R_L = 0		330		mA
		R_L = 0, V_{IN} = 16 V		200		
V_{EN}	Enable input logic low	V_{IN} = 2.5 V to 18 V, -40 °C < T_J < 125 °C			0.4	V
	Enable input logic high	V_{IN} = 2.5 V to 18 V, -40 °C < T_J < 125 °C	1.2			
I_{EN}	Enable pin input current	V_{EN} = V_{IN}		0.1	100	nA
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{OUT}	Output capacitor	Capacitance (see Section 6: Typical characteristics)	1		22	µF

6 Typical characteristics

Unless otherwise specified: T_J = 25 °C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, C_{IN} = C_{OUT} = 1 µF.

Figure 5. Output voltage vs. temperature (V_{IN} = 2.5 V, V_{OUT} = V_{ADJ}, I_{OUT} = 1 mA)

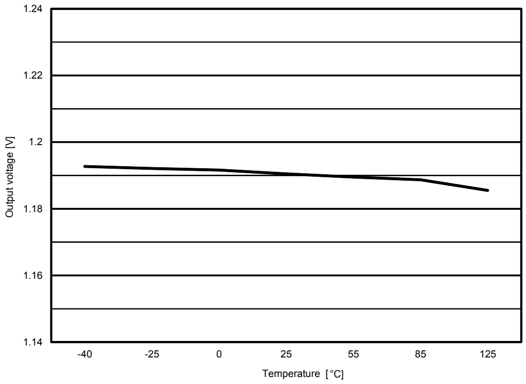


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Figure 6. Output voltage vs. temperature (V_{IN} = 2.5 V, V_{OUT} = V_{ADJ}, I_{OUT} = 200 mA)

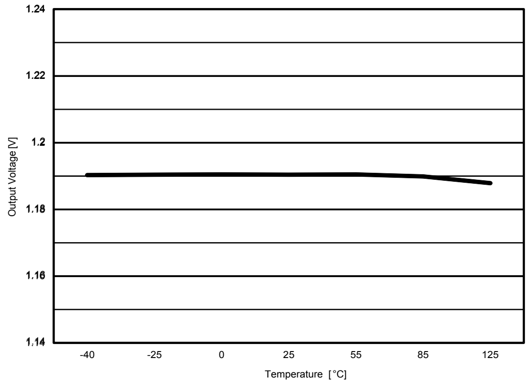

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Figure 7. Output voltage vs. temperature (V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA)

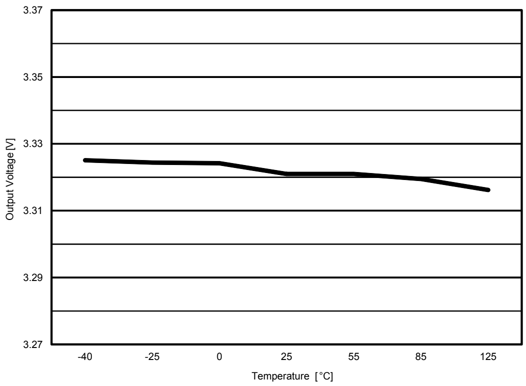

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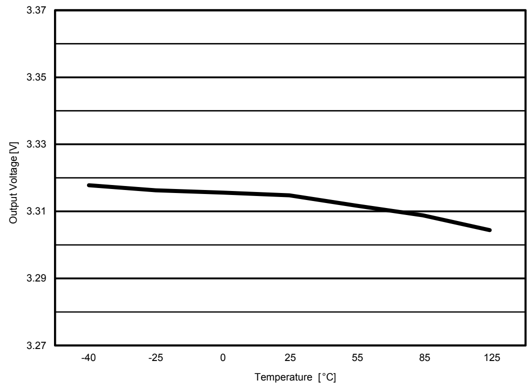
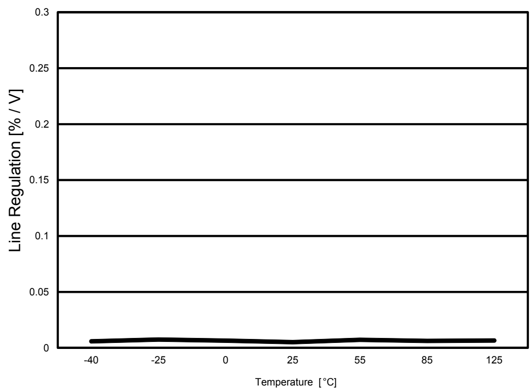
Figure 8. Output voltage vs. temperature (V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 200 mA)



GIPD040820151210MT

Figure 9. Line regulation vs. temperature (V_{IN} = 4.3 to 18 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA)



GIPD040820151211MT

Figure 10. Line regulation vs. temperature (V_{IN} = 2.5 to 18 V, V_{OUT} = V_{ADJ}, I_{OUT} = 1 mA)

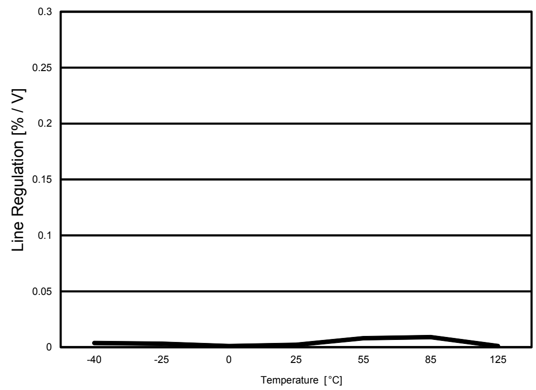


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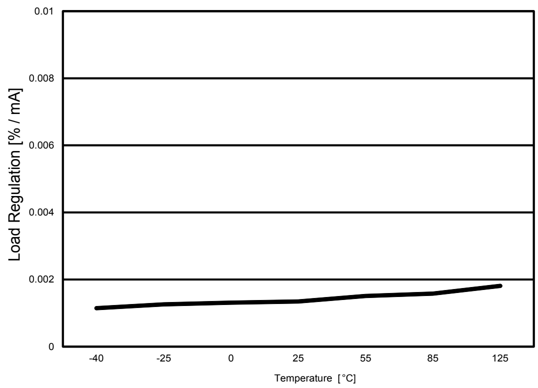
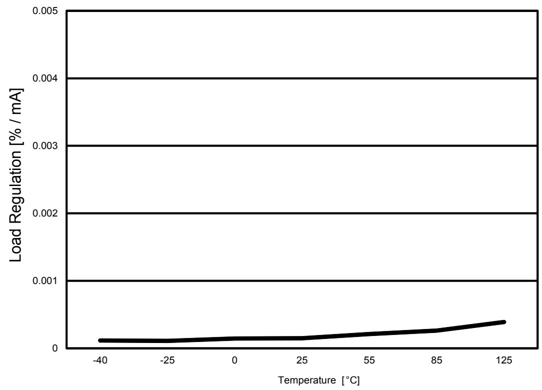
Figure 11. Load regulation vs. temperature (V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 1 to 200 mA)



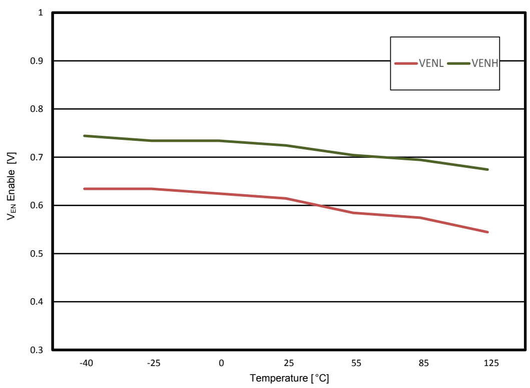
GIPD040820151213MT

Figure 12. Load regulation vs. temperature (V_{IN} = 2.5 V, V_{OUT} = V_{ADJ}, I_{OUT} = 1 to 200 mA)



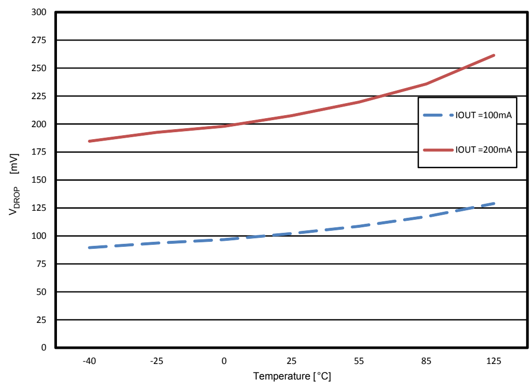
GIPD040820151214MT

Figure 13. Enable thresholds vs. temperature (I_{OUT} = 1 mA)



GIPD040820151215MT

Figure 14. Dropout voltage vs. temperature



GIPD040820151216MT

Figure 15. Quiescent current vs. input voltage (I_{OUT} = 1 mA)

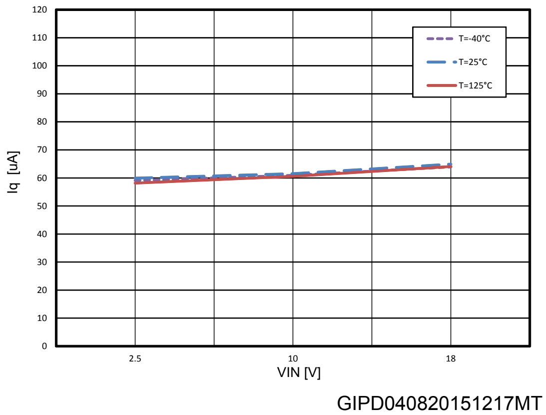


Figure 16. Quiescent current vs. temperature (I_{OUT} = 1 mA)

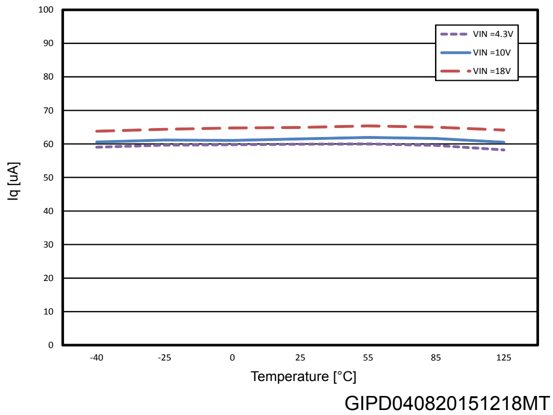


Figure 17. Quiescent current vs. output current (V_{IN} = 4.3 V)

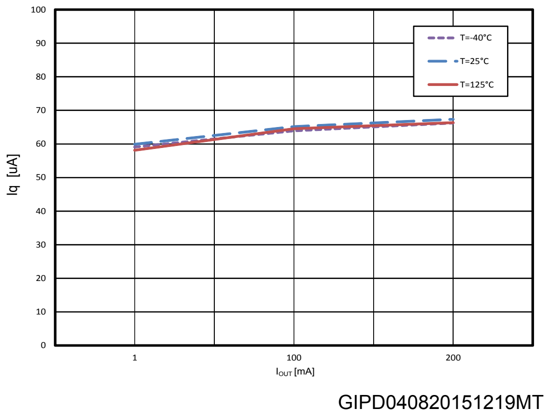


Figure 18. Quiescent current vs. temperature (I_{OUT} = 200 mA)

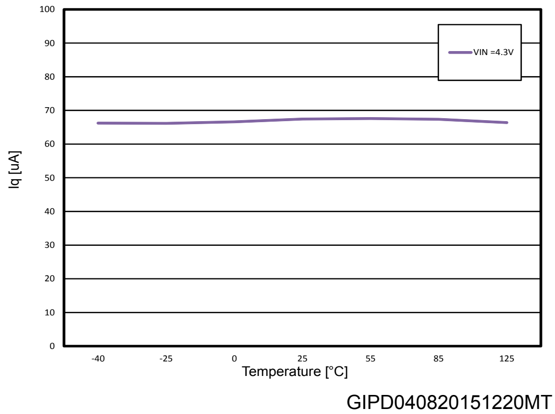


Figure 19. Off-state current vs. temperature

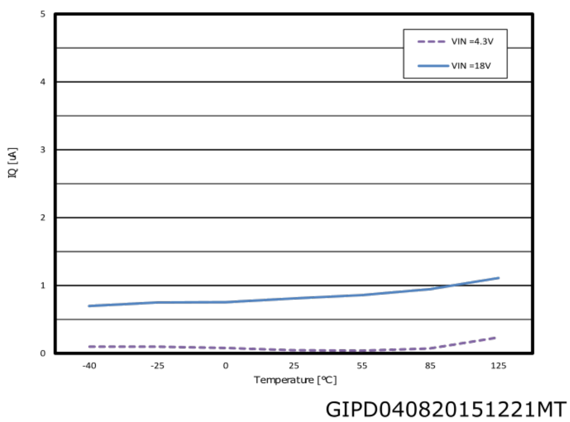


Figure 20. Short-circuit current vs. temperature (V_{IN} = 4.3 V)

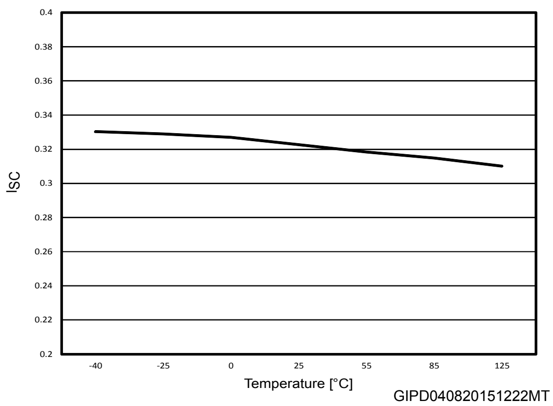


Figure 21. Dropout voltage vs. I_{OUT}

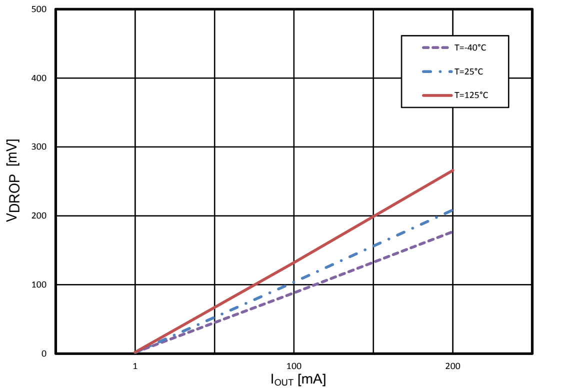


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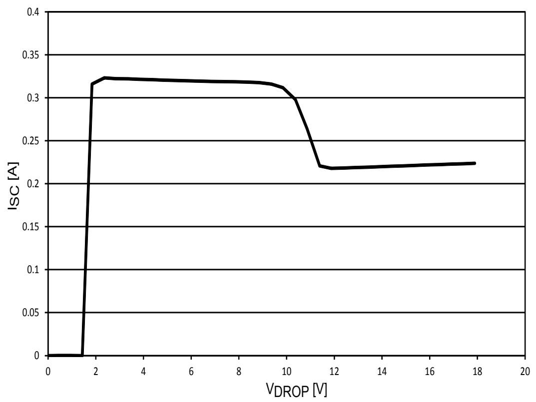
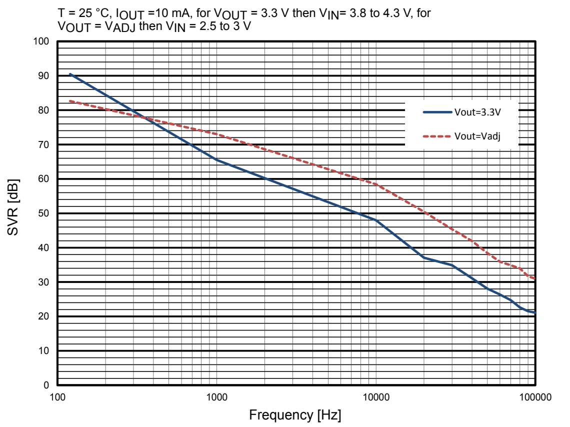
Figure 22. Short-cicuit current vs. drop voltage



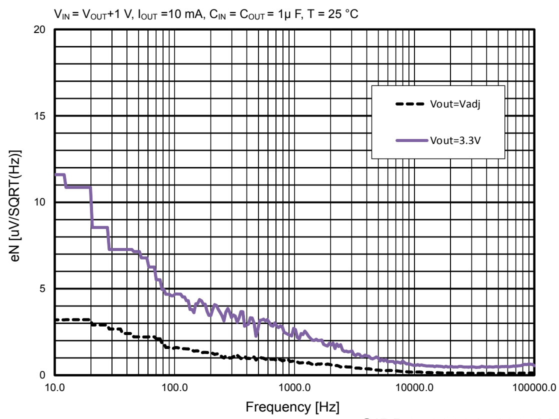
GIPD040820151224MT

Figure 23. SVR vs. frequency



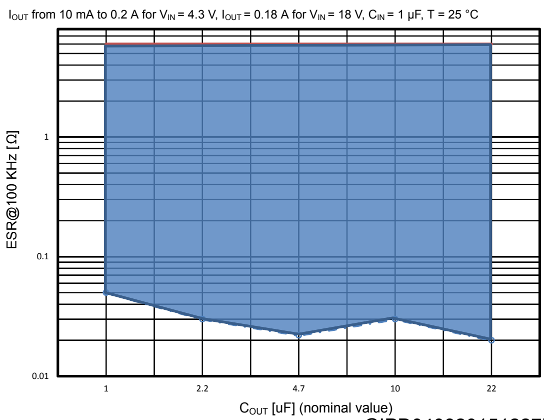
GIPD040820151225MT

Figure 24. Output noise spectral density



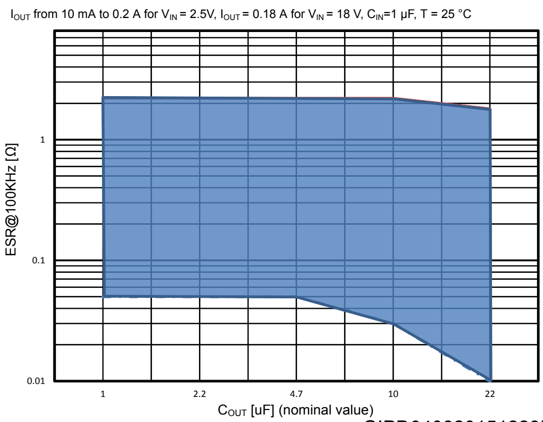
GIPD040820151226MT

Figure 25. Stability plan (V_{OUT} = 3.3 V)



GIPD040820151227MT

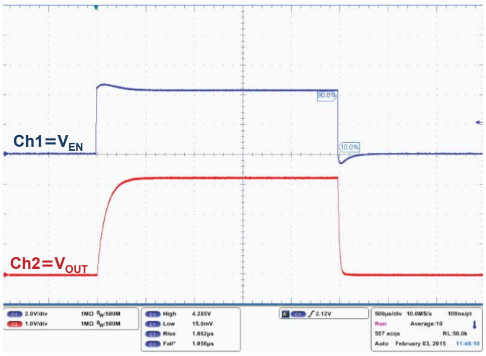
Figure 26. Stability plan (V_{OUT} = V_{ADJ})



GIPD040820151228MT

Figure 27. Startup with enable (V_{OUT} = 3.3 V)

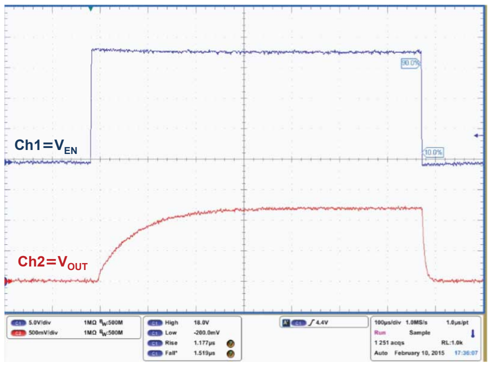
VIN = 4.3 V, VEN = from 0 to Vin, IOUT = 200 mA, CIN = COUT = 1 µF trise = tfall = 1 µs



GIPD040820151229MT

Figure 28. Startup with enable (V_{OUT} = V_{ADJ})

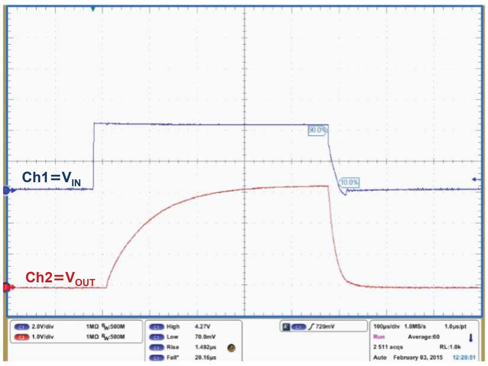
V_{IN} = 18 V, V_{EN} = from 0 to V_{in}, I_{OUT} =200 mA, C_{IN} = C_{OUT} =1 µF trise = t_{fall} = 1 µs



GIPD040820151230MT

Figure 29. Turn-on time (V_{OUT} = 3.3 V)

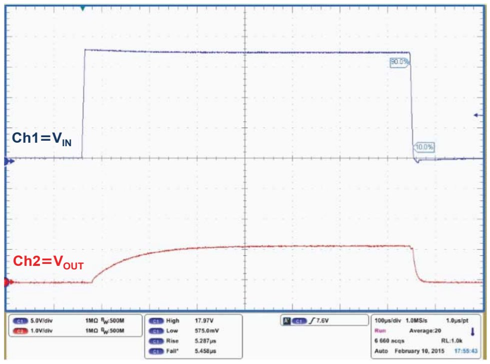
V_{IN} = V_{EN} = from 0 to 4.3 V, I_{OUT} = 200 mA, C_{IN} = C_{OUT} = 1 µF, T_{rise} = 1 µs



GIPD040820151231MT

Figure 30. Turn-on time (V_{OUT} = V_{ADJ})

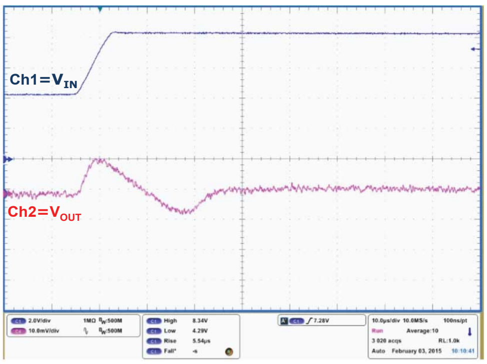
V_{IN} = V_{EN} = from 0 to 18 V, I_{OUT} = 200 mA V_{OUT} = V_{REF}, C_{IN} = C_{OUT} = 1 µF T_{rise} = 5 µs



GIPD040820151232MT

Figure 31. Line transient (V_{OUT} = 3.3 V, rise)

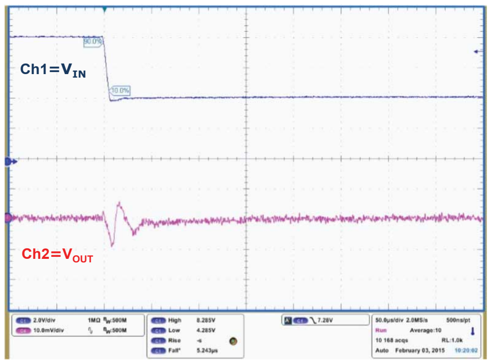
V_{IN} = V_{EN} = from 4.3 to 8.3 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF T_{rise} = 5 µs



GIPD040820151233MT

Figure 32. Line transient (V_{OUT} = 3.3 V, fall)

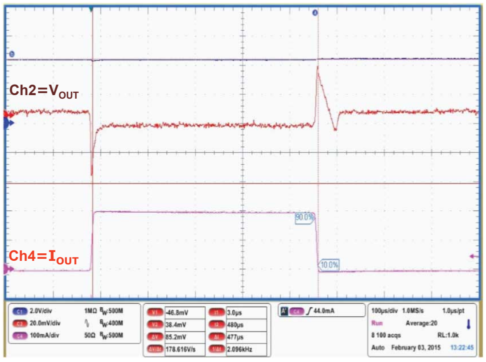
V_{IN} = V_{EN} = from 4.3 to 8.3 V, I_{OUT} =10 mA, C_{IN} = C_{OUT} =1 µF T_{fall} = 5 µs



GIPD040820151234MT

Figure 33. **Load transient (V_{OUT} = 3.3 V, rise)**

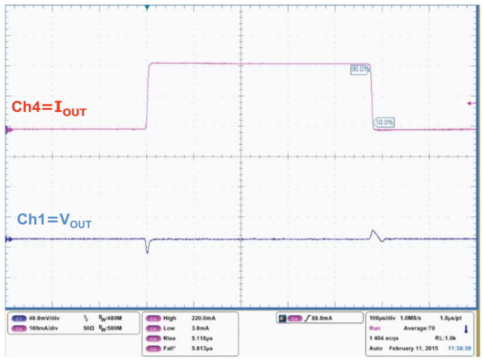
V_{IN} = V_{EN} = 4.3 V, I_{OUT} = from 1 to 200 mA, C_{IN} = C_{OUT} = 1 µF T_{rise} = 5 µs



GIPD040820151236MT

Figure 34. **Load transient (V_{OUT} = V_{ADJ}, fall)**

V_{IN} = V_{EN} = 2.5 V, I_{OUT} = from 1 to 200 mA, C_{IN} = C_{OUT} = 1 µF T_{rise} - T_{fall} = 5 µs



GIPD040820151237bMT

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SOT23-5L package information

Figure 35. SOT23-5L package outline (option A)

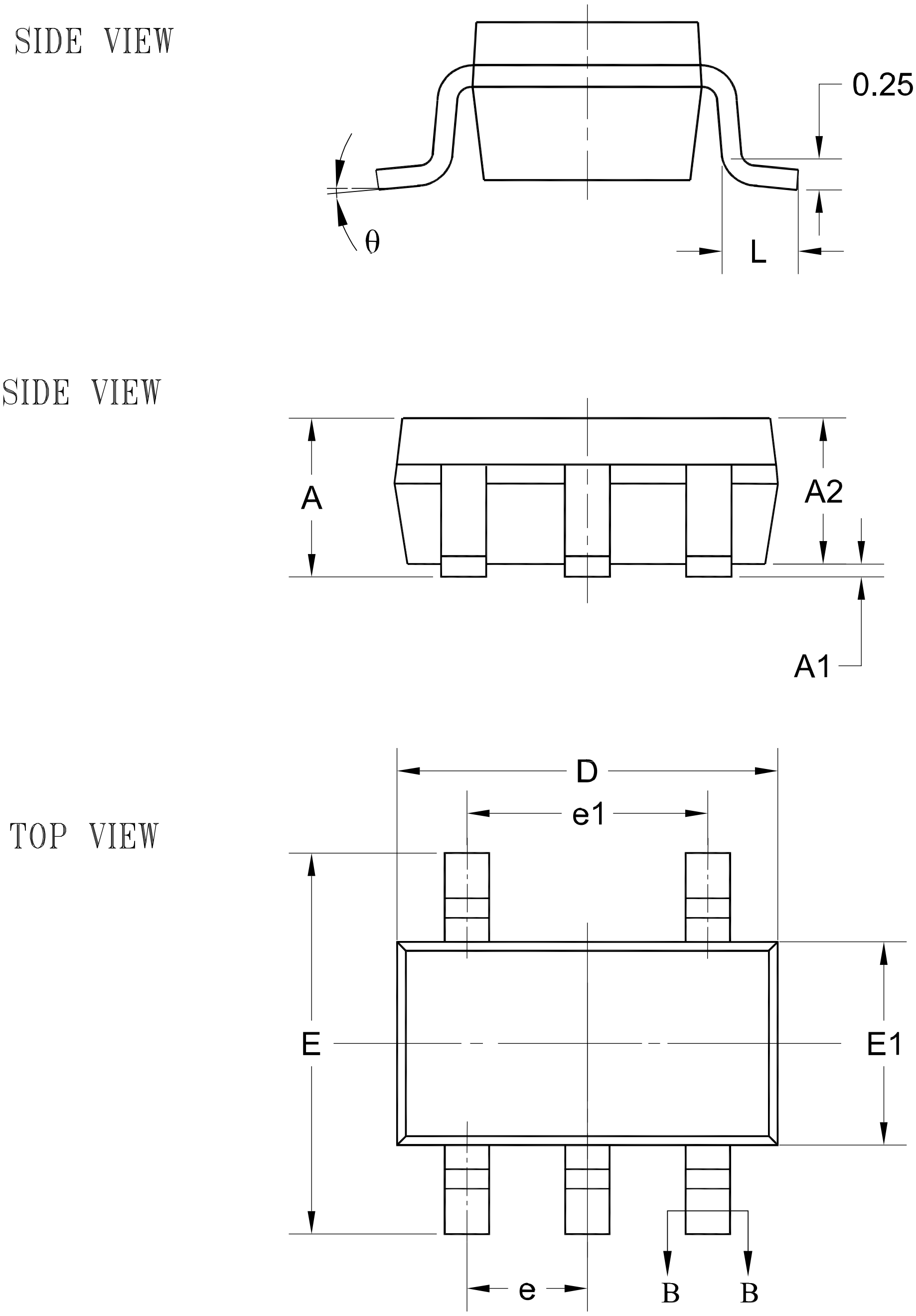


Table 8. **SOT23-5L mechanical data (option A)**

Dimensions (mm)			
Symbol	Min.	Nom.	Max.
A	-	-	1.25
A1	0.04	-	0.10
A2	1.00	1.10	1.20
b	0.33	-	0.41
b1	0.32	0.35	0.38
c	0.15	-	0.19
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	-	0.60
Θ	0°		8°

7.2 SOT23-5L package information

Figure 36. SOT23-5L package outline (option B)

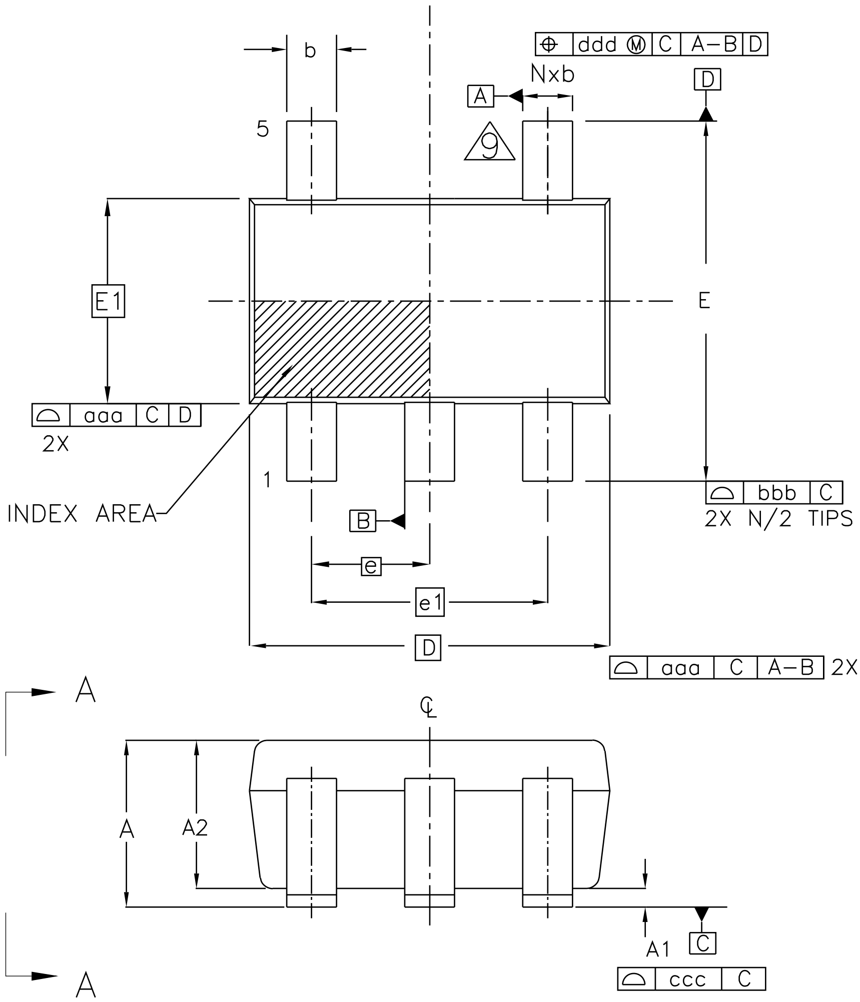
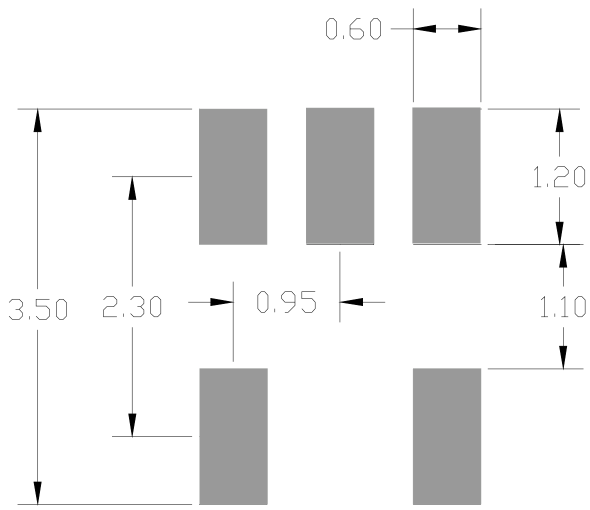


Table 9. SOT23-5L package mechanical data (option B)

Dim.	mm		
	Min.	Typ.	Max.
A	0.90		1.45
A1	0		0.15
A2	0.90		1.30
b	0.30		0.50
c	0.14		0.20
c1	0.14	0.15	0.16
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
e1	1.90 BSC		
L	0.30		0.55
L2	0.25		
N	5		
θ	0°		8°
	Tolerance		
aaa	0.15		
bbb	0.20		
ccc	0.10		
ddd	0.20		
eee	0.08		

Figure 37. SOT23-5L recommended footprint



Note: Dimensions are in mm

7.3 SOT23-5L packing information

Figure 38. SOT23-5L tape and reel outline

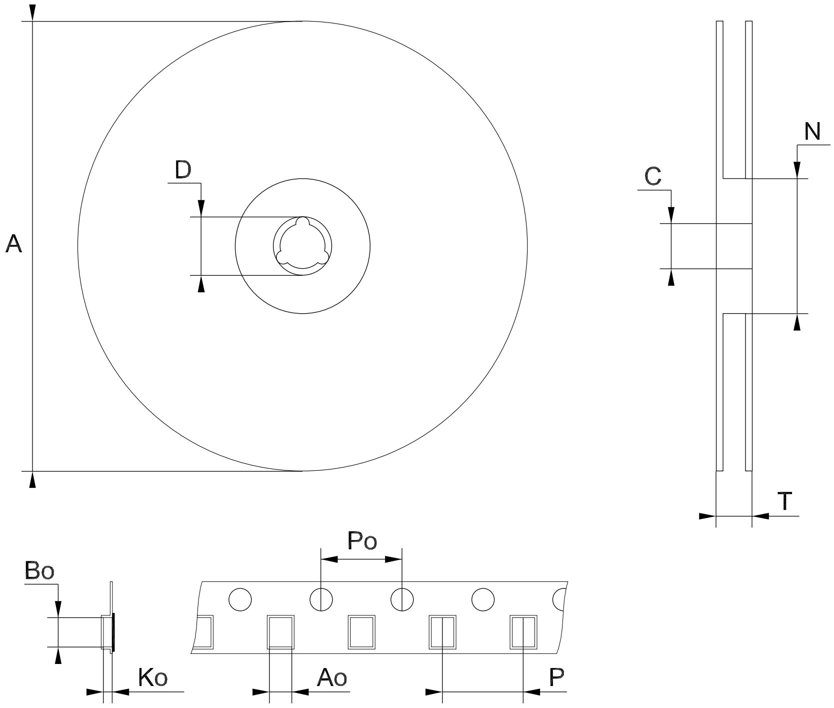


Table 10. SOT23-5L tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			180
C	12.8	13.0	13.2
D	20.2		
N	60		
T			14.4
Ao	3.13	3.23	3.33
Bo	3.07	3.17	3.27
Ko	1.27	1.37	1.47
Po	3.9	4.0	4.1
P	3.9	4.0	4.1

7.4 SOT-89 package information

Figure 39. SOT-89 package outline

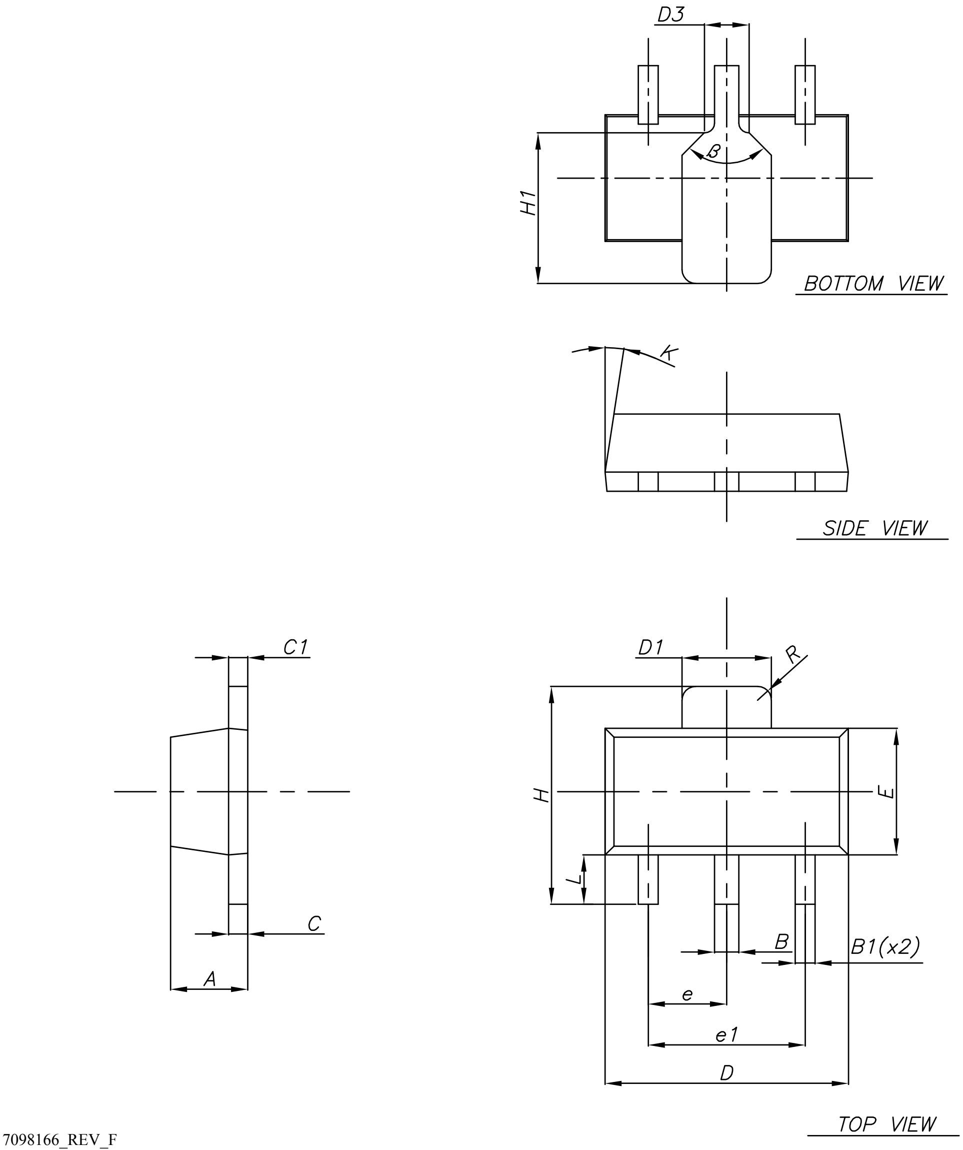
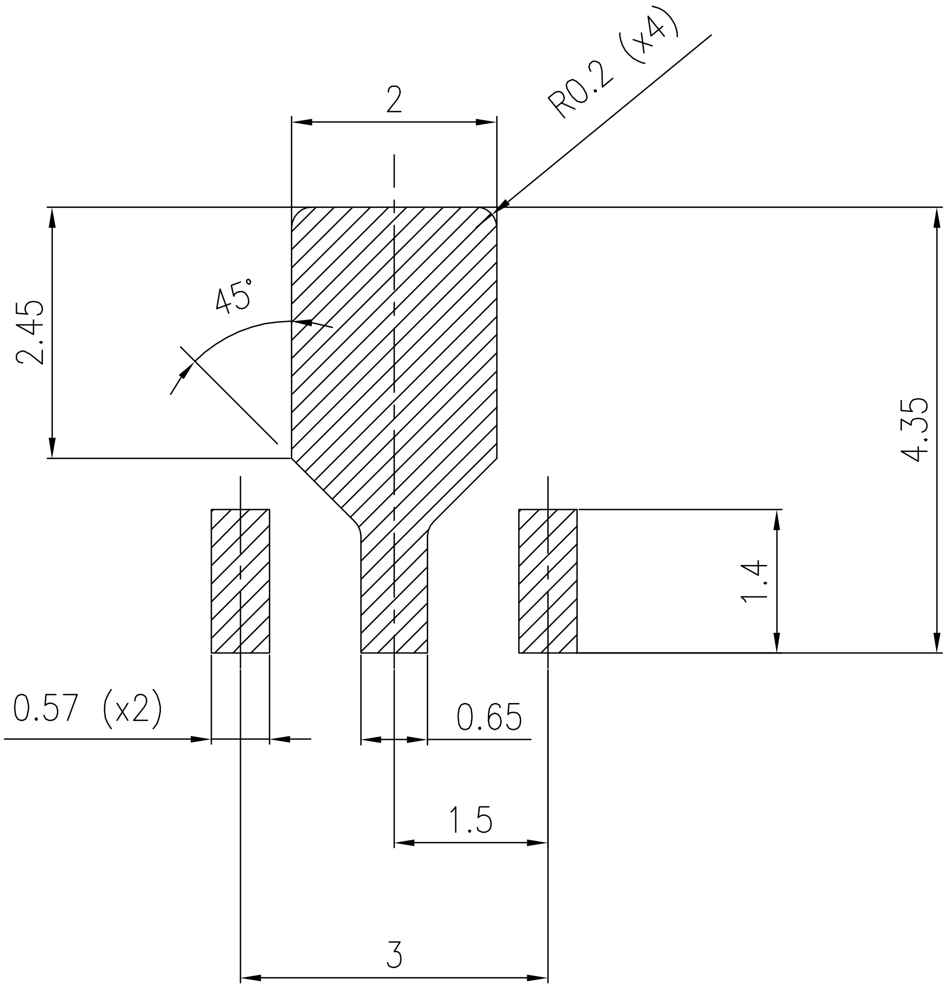


Table 11. SOT-89 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.40		1.60
B	0.44		0.56
B1	0.36		0.48
C	0.35		0.44
C1	0.35		0.44
D	4.40		4.60
D1	1.62		1.83
D3		0.90	
E	2.29		2.60
e	1.42		1.57
e1	2.92		3.07
H	3.94		4.25
H1	2.70		3.10
K	1°		8°
L	0.89		1.20
R		0.25	
β		90°	

Figure 40. SOT-89 recommended footprint



7.5 SOT-89 packing information

Figure 41. **SOT-89 carrier tape outline**

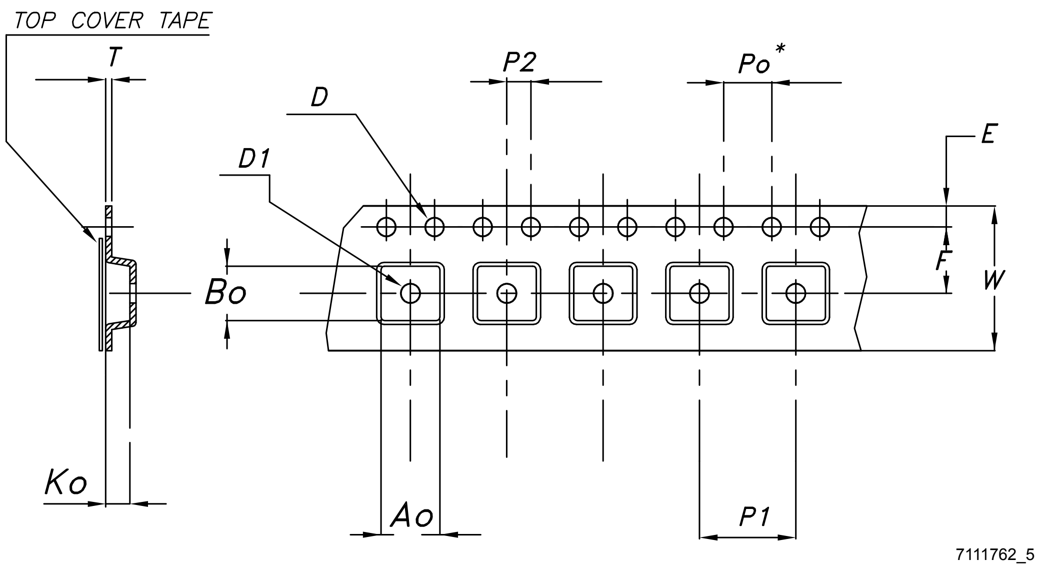


Figure 42. **SOT-89 device orientation**

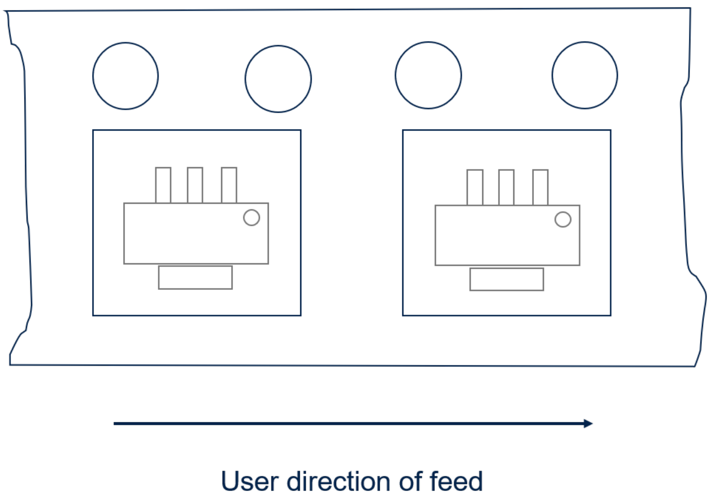
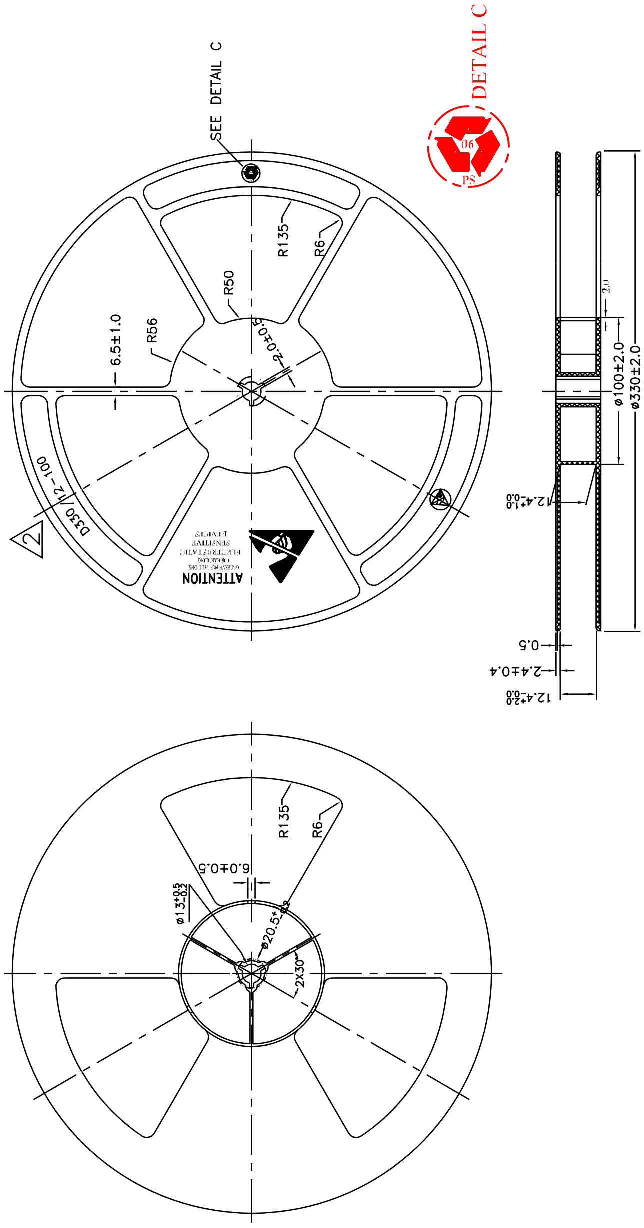


Table 12. SOT-89 carrier tape mechanical data

Dim.	mm	
	Value	Tolerance
Ao	4.91	± 0.10
Bo	4.52	± 0.10
Ko	1.90	± 0.10
F	5.50	± 0.10
E	1.75	± 0.10
W	12	± 0.30
P2	2	± 0.10
Po	4	± 0.10
P1	8	± 0.10
T	0.30	± 0.10
D	Ø 1.55	± 0.05
D1	Ø 1.60	± 0.10

Figure 43. **SOT-89 reel drawing**



8 Ordering information

Table 13. **Order code**

SOT23-5L	SOT-89 (D configuration)	SOT-89	Marking	Accuracy (%)	Output voltage
LDK320AM-R			ADA	0.5	ADJ
LDK320M-R			KAD	2	
LDK320AM12R [(1)]				0.5	1.2
LDK320M12R [(1)]				2	
LDK320AM15R [(1)]			15A	0.5	1.5
LDK320AM18R [(1)]			18A	0.5	1.8
LDK320M18R			K18	2	
LDK320AM25R			25A	0.5	2.5
LDK320M25R			K25	2	
LDK320AM30R			30A	0.5	3
	LDK320ADU30R		30	0.5	
LDK320M30R			K30	2	
LDK320AM33R			33A	0.5	3.3
	LDK320ADU33R		33	0.5	
LDK320M33R			K33	2	
LDK320AM36R			36A	0.5	3.6
LDK320AM50R			50A	0.5	5
	LDK320ADU50R		50	0.5	
		LDK320AU50R	E0	0.5	
LDK320M50R			K50	2	
LDK320AM120R			120A	0.5	12
	LDK320ADU120R		A2	0.5	
LDK320M120R [(1)]				2	

1. *Available on request.*

Revision history

Table 14. **Document revision history**

Date	Revision	Changes
16-Nov-2015	1	First release.
01-Jun-2016	2	Document status promoted from preliminary data to production data. Updated title and features in cover page. Updated Section 8: “Ordering information”. Minor text changes.
05-Jul-2017	3	Updated Section 8: "Ordering information". Minor text changes.
09-Oct-2018	4	Updated ΔV_{OUT} test condition in Table 6. LDK320 electrical characteristics (fixed output version). Added new order code LDK320AU50R in Table 12. Order code.
28-Oct-2019	5	Added ΔV_{OUT} for SOT-89 in Table 6. LDK320 electrical characteristics (fixed output version).
23-Jul-2020	6	Updated Figure 2. Block diagram (adjustable version).
10-Nov-2020	7	Updated Table 12. Order code.
12-Nov-2020	8	Added new Marking column in Table 13. Order code.
26-Apr-2022	9	Updated Section 7.2. Added new Section 7.1 SOT23-5L package information.
05-Dec-2023	10	Updated VADJ and VDROP test conditions in Table 7.
04-Jun-2024	11	Updated Figure 35

Contents

List of tables

List of figures