Enabling Visual Communication

LEADIS®

LDS274

Data Sheet

528 Source (176 x 3) + 240 Gate
260K-Color One-Chip TFT Driver

Oct. 11, 2004 PRELIMINARY

CONTENTS

Document No: LTT274DS-050

Prepared by: Ted Park

REVISION HISTORY

Date	Contents	Version
May. 27, 2003	- Preliminary Version 0.0	Ver 0.00 (Preliminary)
July. 14, 2003	- Serial interface mode added - RGB interface input bus pad changed. - Interface selection pad and method changed - Gamma curve added (Section 5.9.4) - Reference application updated (Section 8) - Minor change	Ver 0.10
July. 26, 2003	- Section 5.13 (Input/Output Pin State) added. - Extended command set minor updated. (Section 6) - Default value added (Section 5.2.8) - ID3 valued fixed to 10h - VDD1 range changed: 1.65V ~ 1.95V -> 1.65V ~ 2.50V - Minor change	Ver 0.11
Aug. 06, 2003	- Page6: FRM, EXTC pad added. - Page6: GS1, GS0 description updated. - Page 69, 70: 2.75V->2.5V/2.75V, 2.6V->2.3V - WRID2 command added - EPWRIN / EPWROUT command updated (Flow chart) - Section 6.3.3 EEPROM Access Control added - Default value of Vertical Scroll Area (VSA) changed to 00h - AC spec changed (Cycle time: 160ns -> 150ns)	Ver 0.20
Sep. 08, 2003	- Page6: GS1, GS0 removed and changed to TEST4, TEST5. - One more dummy gate added (G241) - ENABLE signal polarity changed (Fig5.2.1, 5.2.3) - Column/row address counter status table added (Section 5.2.3) - Section 5.7.2 and 5.7.3 gate drive option 2,3 exchanged. - Section 5.9.4 Gamma curve generation circuit updated. - SLEEP In discharge time (voltage stabilization time) changed to 120msec - Section 6.1.18 RAMRD command updated (16-bit-> both 16 and 18-bit) - Section 6.1.34 INVCTR command updated - Section 6.1.35 PATCTR command updated - Section 6.1.36 GAMCTR command updated - Section 6.1.37 IFMODE command updated - Section 6.1.38 EPWROUT command updated (Flow chart) - Section 6.1.39 EPWRIN command updated (Flow chart) - Section 6.1.42 VCOMOFS command updated - Section 6.1.43 VCOMCTR command updated - Section 6.1.50 SGTCTR command updated (parameter name changed)	Ver 0.30

	- Section 6.1.52 REGAPP command added - Section 6.3.3 EEPROM access sequence updated - Section 7.6.1 DC Characteristics updated - Section 7.7.3 Serial AC characteristics added - Section 6.1.43 VCOMCTR command updated - Section 8.3 added. - Section 9 Chip information & Pad coordinates added.	
Jan. 27, 2004	- Page 6: TESTF -> TEST2 - Page 10: !CS -> !SCE - Page 14 and 15: P/!S = "L" removed - Page 17 and 18: P/!S = "L" removed, !RD and !WR -> R/!W and E - Page 28: 65K Color -> 262k Color - Page 52: 130^{th} -> 208^{th} - Page 74: Note 2) changed - Page 79: ST8, ST7, ST6 changed - Page 164: Connection With LCD Panel changed - Page 170: VSS2 -> VSS - Page 171 and 172: VSS1 -> VSS	Ver 0.31
Feb. 04, 2004	- Section 9 Chip information & Pad coordinates updated.	Ver 0.32
July 24, 2004	- Section 5.9.4.2 updated - Section 6.1.36 GAMCTR command updated - Page 131: VCOFS command restriction and flow chart updated - Page 132: VCOMCTR command restriction and flow chart updated	Ver 0.40
July 28, 2004	- Page 73 and 119: INVCTR command updated - Page 122: GAMCTR command updated	Ver 0.41
Aug. 02, 2004	- Page 73 and 122: GAMCTR command, parameter position changed - Page 128: DISCLK command, frame frequency calculation method and default value updated. - Page 113 and 144: COLMOD command, parameter default value updated.	Ver 0.42
Oct. 11, 2004	- Page 28: 18-bit per pixel data transfer in 8-bit parallel interface bit assignment changed (D[5:0] -> D[7:2]) - Page 50: Table 5.2.12 TE signal AC timing updated - Page 74: Instruction code table updated (AMPCTR, SGTCTR and REGAPP1 command) - Page 74 and 143: REGAPP1 command added - Page 119: INVCTR command default value changed - Page 128 and 129: DISCLK command, default vale and equation for frame frequency updated - page 132: VCOMCTR command updated - Page 133: PWRCTR command restriction added - Page 134: OUTCTR command updated - Page 135: REGCTR command default value changed - Page 136: AMPCTR command description updated, ACS, LACS parameter removed - Page 137 and 138: BSTCLK command restriction and default value changed - Page 140: STRCTR command updated, SZS and SZE parameter removed - Page 77, 116 and 145: ID3 default value changed from 10h to 14h	Ver 0.50

	- Page 151 and 152: DC characteristic updated - Page 166: External component connection drawing updated (two shot-key diode added)	

1 DESCRIPTION

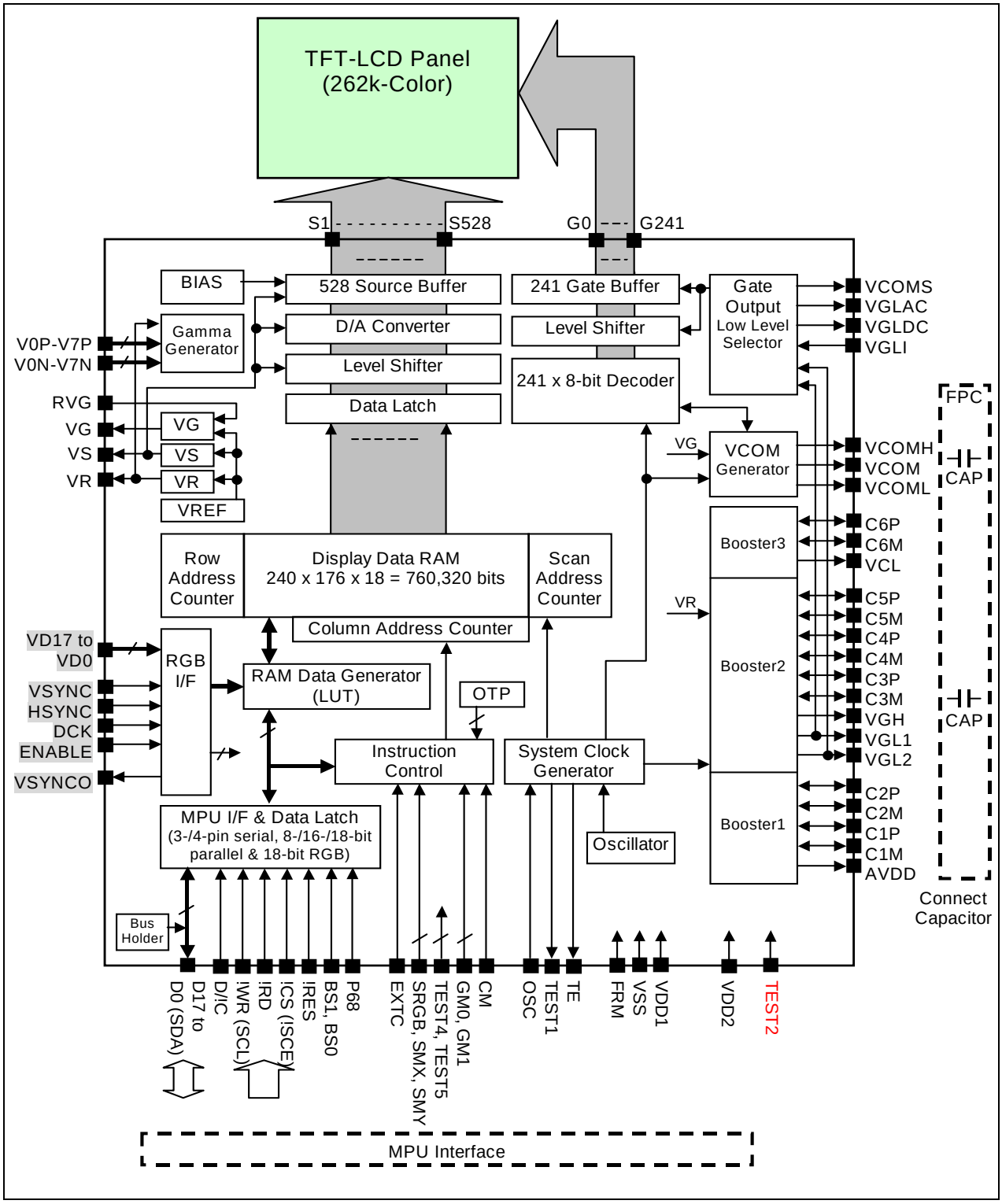
LDS274 is a single chip low power CMOS LCD controller/driver for color TFT-LCD displays of 240, 220 or 208 gates and 176xRGB columns. It has a 760k-bit (176 x 18bit x 240) display RAM and a full set of control functions. LDS274 offers 8 kinds microprocessor interfaces: 8080-system (8-bit, 16-bit or 18-bit), 6800-system (8-bit, 16-bit or 18-bit) and serial (3-pin or 4-pin). It also supply 18-bit RGB interface for driving Video signal directly from controller.

2 FEATURES

- Single chip TFT-LCD controller/driver
- Outputs:
  - 528 source outputs (176 x RGB)
  - Selectable 208, 220 or 240 gate outputs plus two dummy gate outputs
  - Common electrode output
- Display mode (Color modes):
  - Full colors (Idle mode off): 262k- or 65k-colors
  - Reduced color (Idle mode on): 8-colors (3-bit binary mode)
- Interface mode (Color modes on the display host interface) :
  - 8 bit/pixel: (RGB) = (332) using the 760k-bit frame memory and a look up table (LUT) with a bit connection
  - 12 bit/pixel: (RGB) = (444) using the 760k-bit frame memory and a look up table (LUT) with a bit connection
  - 16 bit/pixel: (RGB) = (565) using the 760k-bit frame memory and a bit connection (Red and Blue)
  - 18 bit/pixel: (RGB) = (666) using the 760k-bit frame memory directly
- Display data RAM (frame memory): 240 x 176 x 18-bit = 760k bit
- MPU Interfaces:
  - 3-pin or 4-pin serial interface
  - 8-bit, 16-bit or 18-bit interface with 8080-series MPU
  - 8-bit, 16-bit or 18-bit interface with 6800-series MPU
  - 18-bit RGB interface with graphic controller
- Display features
  - Area scrolling
  - Partial display mode
  - Software programmable color depth mode
  - N-line inversion for low cross talk
- On chip:
  - DC/DC converter
  - Adjusted VCOM generation
  - OTP to store initialization register setting
  - Oscillator for display clock generation.
- Driving algorithm:
  - 2 or 3 level gate drive with common electrode modulation drive
  - Line inversion, frame inversion

- Logic supply voltage range VDD1 to VSS
  1.65 to 2.50V
- Analog supply voltage range for VLCD generation VDD2 to VSS2:
  2.3 to 2.9V
- Output voltage levels:
  - Source output voltage range VS to VSS2: 3.0 to 5.5 V
  - Common electrode output voltage range VCOM to VSS2: -2.5 to 5.5 V
  - Positive Gate output voltage range: +9.0 to +15.75 V
  - Negative Gate output voltage range: -6.0 to –15.75 V
- Low power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Optimized layout for COG assembly

3 BLOCK DIAGRAM



4 PIN DESCRIPTION

Table 4.1.1 Pin Description

Name	Type	Description
Driver output pins		
S1 to S528	O	Source driver outputs
G0 to G241	O	Gate driver outputs. G0 and G241 are dummy gate outputs. Selectable 2 or 3 level output. 2-Level: VGH and VGL2 (or VGL1), 3-level: VGH, VGL1 and VGL2
Power supply pins		
VDD1	P	Power supply for logic system
VDD2	P	Power supply for analog system and boosting input voltage
VSS	P	System ground for internal system
VSS1	P	System ground for a manufacturer's special use. Should be connected to VSS.
LCD supply voltage generation (DC-DC converter and Regulator)		
C1P, C1M C2P, C2M C3P, C3M C4P, C4M C5P, C5M C6P, C6M	I/O	Capacitor connection pin for booster circuit.
AVDD	O	Output of booster1 circuit (output of 2-times or 3-times output of VDD2). Connect capacitor to VSS (GND)
VR	O	Output of the VR regulator and be used as input of booster2 circuit. Connect capacitor to VSS (GND)
VS	O	Output of the VS regulator and be used as positive power of source driver Connect capacitor to VSS (GND)
VG	O	Output of the VG regulator and be used as positive power of gamma voltage generator. Connect capacitor to VSS (GND)
RVG	I	External resistor input for VS/VR regulator.
VGH	O	Positive output voltage of the booster2 (2*VR or 3*VR) The boosting step is selected by how the external capacitor is connected.
VGL1	O	Negative output voltage of the booster2 (-1*VR or -2*VR) The boosting step is selected by how the external capacitor is connected.
VGL2	O	Negative output voltage of the booster2 (-2*VR or -3*VR) The boosting step is selected by how the external capacitor is connected.
VCL	O	Negative voltage output of booster3 circuit for VCOM (-1*VDD2)
VCOMH	O	Positive voltage output of VCOM.
VCOML	O	Negative voltage output of VCOM.
VCOM	O	Common output signal. The swing voltage level is VCOML to VCOMH.
V0P to V7P V0N to V7N	I	External gamma voltage V0P to V7P: positive polarity voltages, V0N to V7N: negative polarity voltages

Table 4.1.2 Pin Description (continued)

Name	Type	Description
VCOMS	O	VCOM switch control output for gate drive option 2 Refer to the Gate drive option 2
VGLAC	O	Gate low level AC output for gate drive option 2 Refer to the Gate drive option 2
VGLDC	O	Gate low level DC output for gate drive option 3 Refer to the Gate drive option 3
VGLI	I	Gate low level input for gate drive option 2 and 3 Refer to the Gate drive option 2 and Gate drive option 3
Host interface pins		
P68, BS1, BS0	I	Interface mode setting
!RES	I	External reset This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
!CS (!SCE)	I	Chip select input pin (“Low” enable). This pin can be permanently fixed “Low” in parallel interface mode only. If !CS is connected to ground in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.
D/!C	I	Display data / Command selection pin in parallel interface. If not used, please open this pin.
!WR (R/!W) (SCL)	I	Write enable in 8080-series parallel interface. Read write selection in 6800-series parallel interface. If not used, please open this pin.
!RD (E)	I	Read enable in 8080-series parallel interface. Read/write enable in 6800-series parallel interface. If not used, please open this pin.
TE	O	Tearing effect output. If not used, please open this pin.
D17 to D8, D7 to D0	I/O	18-Bit bi-directional display data bus for parallel interface with MPU. 8-Bit bi-directional display data bus for 8-bit parallel interface. 8-Bit command bus for 18-bit, 16-bit or 8-bit parallel interface. In 8-bit parallel, D7 to D0 are used and the others (D17to D8) should be open. In 16-bit parallel, D17 and D16 are not used and should be open.
Mode Select		
SRGB	I	Module RGB order select pin.
SMX	I	Module Source output direction select pin.
SMY	I	Module Gate output direction select pin.
GM1, GM0	I	Gate output number select pins. GM1,GM0 = (00): G0 to G208 are output the gate signal and the others become VSS GM1,GM0 = (01): G0 to G220 are output the gate signal and the others become VSS GM1,GM0 = (1X): G0 to G240 are output the gate signal.

Table 4.1.3 Pin Description (continued)

Name	Type	Description
CM	I	Output color mode select pin. CM=1: 262k color mode is selected and read data becomes 18-bit data format. CM=0: 65k color mode is selected and read data becomes 16-bit data format.
EXTC	I	Extended command code access pin. To use extended command set (like EEPROM program), please connect this to VDD1. During normal operation, please open this pin. (Internal Rpull-down=15KΩ)
FRM	I	This pin can select the free running mode for burn-in test. The display data alternates between full black and full white independent of input data in the free running mode. Leave this open and fix "L" after free running. (Internal Rpull-down=15KΩ) FRM=L: Normal operation mode, FRM=H: Free running mode (Using internal oscillator).
Clock input and RGB interface		
OSC	I	Oscillator input for test purpose. If not used, please open this pin.
VSYNC	I	RGB interface vertical sync input for RGB interface. It used as start pulse input for gate driver. If not used, please open this pin.
HSYNC	I	RGB interface horizontal sync input for RGB interface. It used as start pulse input to receive the valid data for source driver. If not used, please open this pin.
DCK	I	RGB interface pixel clock pin. When the RGB interface is used, the dot clock is input. The RGB data that has been input into VD17 to VD0 are read at the rising time or falling time of this signal. If not used, please open this pin.
ENABLE	I	RGB interface enable pin. This pin is used for the data enable signal when RGB interface is used. If not used, please open this pin.
VD17 to VD0	I	RGB interface data bus. During RGB interface VD17 to VD0 makes 18-bit RGB data bus. If not used, please open these pins.
VSYNCO	O	RGB interface vertical sync output for RGB interface. If not used, please open this pin.
Test pins		
TEST1	O	Test pin, not accessible to user must be left open.
TEST2	I	Test pin, not accessible to user must be left open.
TEST4, TEST5	I	Test pin, please connect these to VDD1

NOTE: DUMMY – These pins should be open (float).

5 FUNCTIONAL DESCRIPTION

5.1 MPU INTERFACE

LDS274 can interface with MPU at high speed. However, if the interface cycle time is faster than the limit, MPU needs to have dummy wait(s) to meet the cycle time limit.

5.1.1 Interface Type Selection

The selection of a given interfaces are done by setting P68, BS1 and BS0 pins as shown in ***Table 5.1.1*** and ***Table 5.1.2.***

Table 5.1.1 Interface Type Selection

P68	BS1	BS0	Interface	Read back select
0	0	0	3-Pin Serial Interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
0	0	1	8080 MPU 8-bit Parallel	!RD strobe (8-bit read data and 8-bit read parameter)
0	1	0	8080 MPU 16-bit Parallel	!RD strobe (16-bit read data and 8-bit read parameter)
0	1	1	8080 MPU 18-bit Parallel	!RD strobe (18-bit read data and 8-bit read parameter)
1	0	0	4-Pin Serial Interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	0	1	6800 MPU 8-bit Parallel	E strobe (8-bit read data and 8-bit read parameter)
1	1	0	6800 MPU 16-bit Parallel	E strobe (16-bit read data and 8-bit read parameter)
1	1	1	6800 MPU 18-bit Parallel	E strobe (18-bit read data and 8-bit read parameter)

Table 5.1.2 Pin Connection according to the Interface Type

P68	BS1	BS0	Interface	!RD	!WR	D/!C	D17-D0
0	0	0	3-Pin Serial Interface	*1)	SCL	*1)	*1) D17-D1: Unused, D0: SDA
0	0	1	8080 MPU 8-bit Parallel	!RD	!WR	D/!C	*1) D17-D8: Unused, D7-D0: 8-bit Data
0	1	0	8080 MPU 16-bit Parallel	!RD	!WR	D/!C	*1) D17-D16: Unused, D15-D0: 16-bit Data
0	1	1	8080 MPU 18-bit Parallel	!RD	!WR	D/!C	D17-D0: 18-bit Data
1	0	0	4-Pin Serial Interface	*1)	SCL	D/!C	*1) D17-D1: Unused, D0: SDA
1	0	1	6800 MPU 8-bit Parallel	E	R/!W	RS	*1) D17-D8: Unused, D7-D0: 8-bit Data
1	1	0	6800 MPU 16-bit Parallel	E	R/!W	RS	*1) D17-D16: Unused, D15-D0: 16-bit Data
1	1	1	6800 MPU 18-bit Parallel	E	R/!W	RS	D17-D0: 18-bit Data

NOTE: 1) Unused pins can be open, connected to VSS or connected to VDD1.

5.1.2 General Protocol

For programming of the LCD driver, the general supported protocol is shown in ***Fig. 5.1.1***

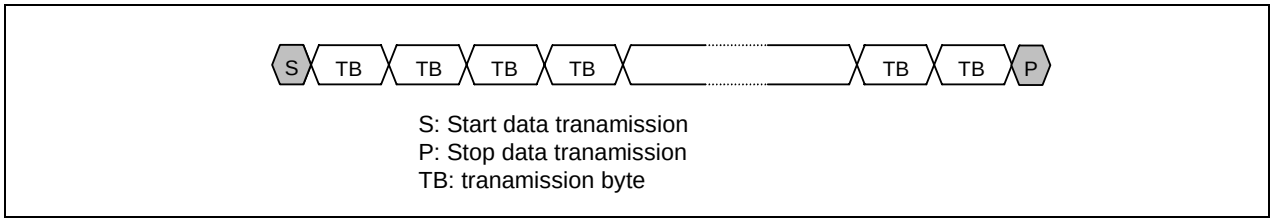


Fig. 5.1.1 Programming protocol

If data write or parameter write is interrupted by any other command, data write command or parameter write command should be done again to write the remained data or parameter.

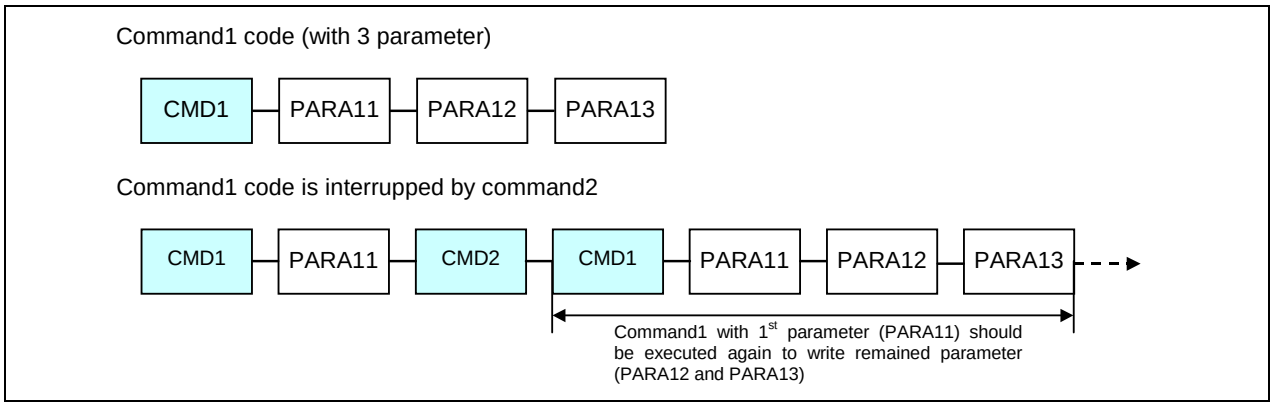


Fig. 5.1.2 Write interrupt sequence

5.1.3 Serial Interface

Communication with the microprocessor can also be done via a clock-synchronized serial peripheral interface. The selection of this interface is done when both BS1 and BS0 are low state (VSS).

The serial interface is a 3-pin or 4-pin bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-pin serial use: !SCE (chip enable), SCL (serial clock) and SDA (serial data input/output) and 4-pin serial use: !SCE (chip enable), D/!C (D1 pad, data / command select), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary.

5.1.3.1 Write Mode

The write mode of the interface means the micro controller writes commands and data to the LDS274. 3-Pin serial data packet contains a control bit D/!C and a transmission byte and in 4-pin serial case, data packet contains just transmission byte and control bit D/!C is transferred by D/!C pin. If D/!C is low, the transmission byte is interpreted as command byte. If D/!C is high, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the LDS274. The MSB is transmitted first. The serial interface is initialized when !SCE is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on !SCE enables the serial interface and indicates the start of data transmission.

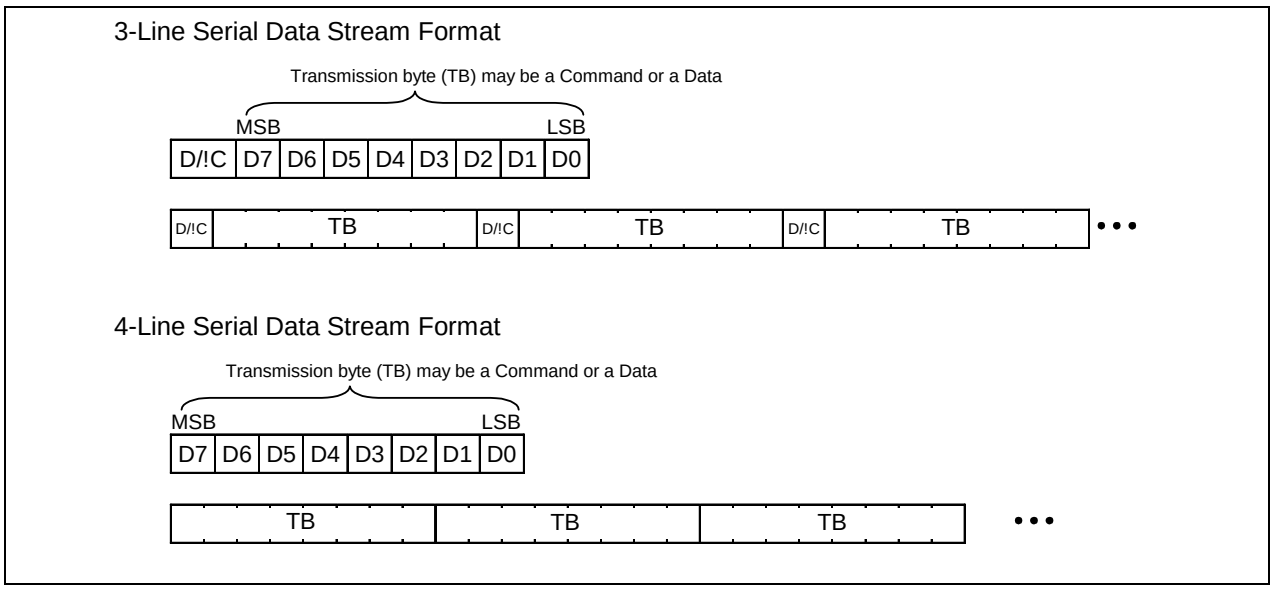


Fig. 5.1.3 Serial data stream, write mode

It is possible to invoke a pause by !SCE while transferring display data or multiple parameter data. If !SCE is high after a whole byte of display data or multiple parameter data has been completed, then LDS274 will wait and continue the display data or multiple parameter data transmission from the point where it was paused as shown in ***Fig. 5.1.4.***

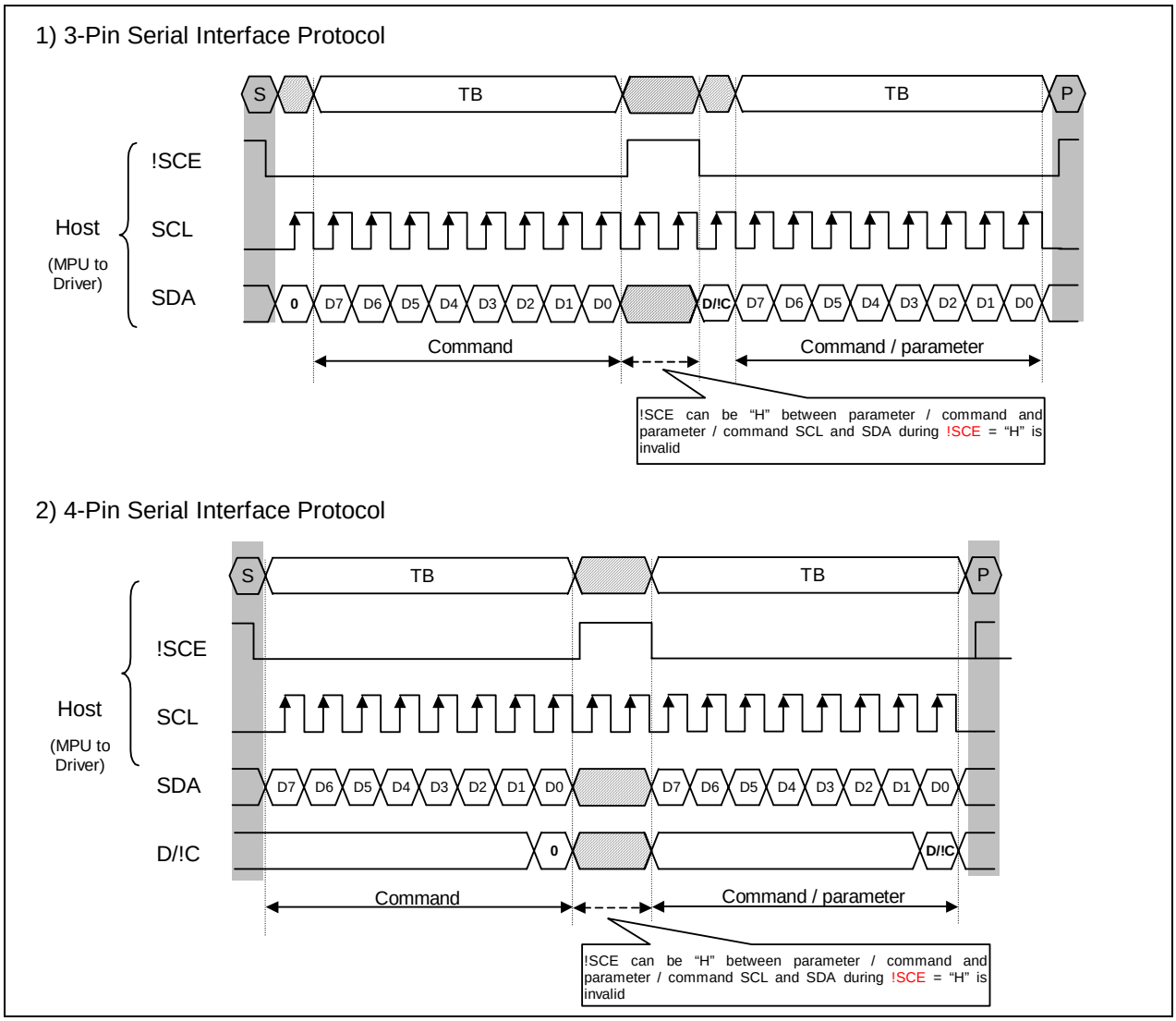


Fig. 5.1.4 Serial bus protocol, write to register with control bit in transmission

5.1.3.2 Read Mode

The read mode of the interface means that the micro controller reads register value from the LDS274. To do so the micro controller first has to send a command (Read ID or Read Register command) and then the following byte is transmitted in the opposite direction. After that !SCE is required to go high before a new command is send (see ***Fig. 5.1.5*** and ***Fig. 5.1.6***). The LDS274 samples the SDA (input data) at the rising edges, but shifts SDA (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges.
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling SCL edge of the last bit (see ***Fig. 5.1.5*** and ***Fig. 5.1.6***).

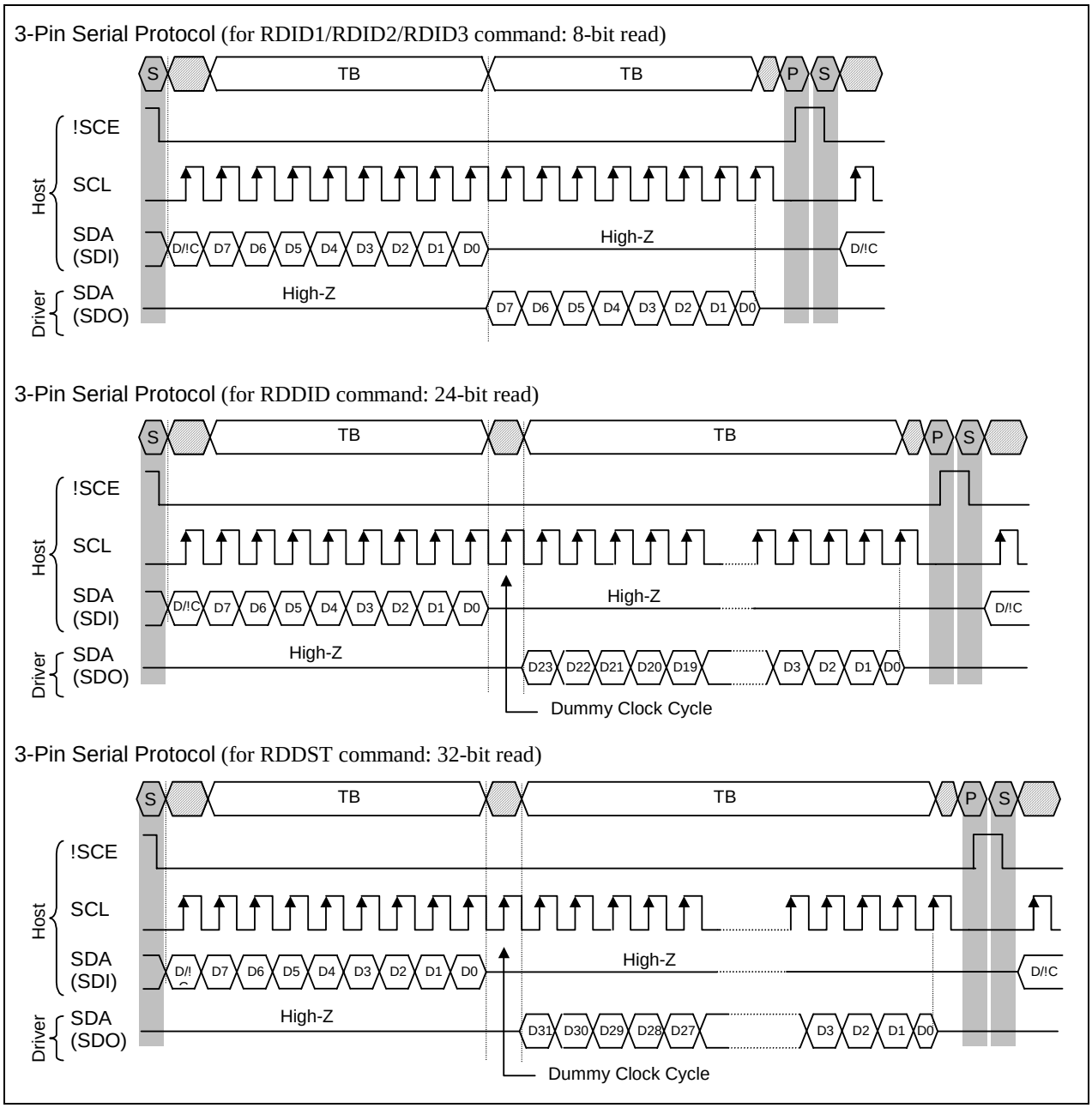
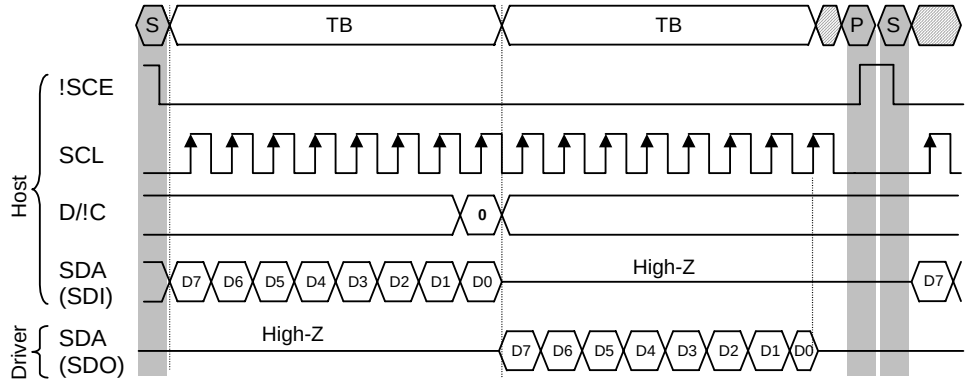
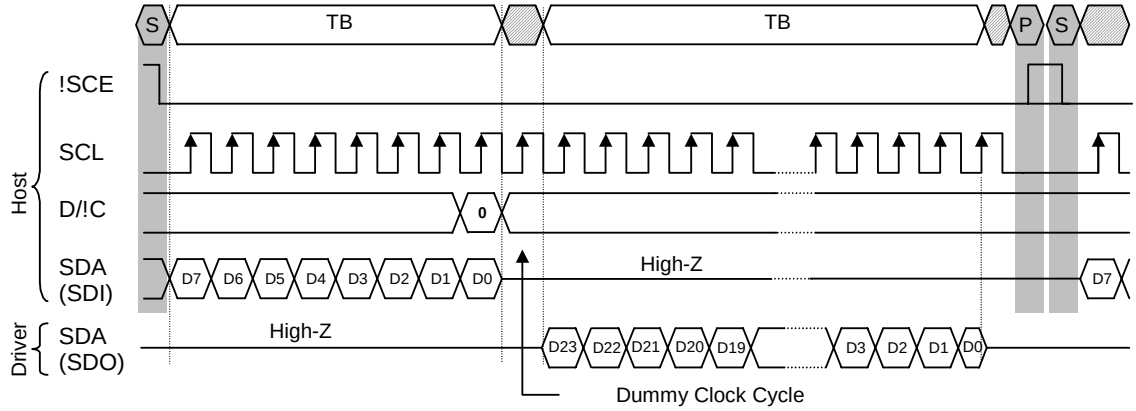


Fig. 5.1.5 Serial bus protocol, read mode (3-Pin serial interface case)

4-Pin Serial Protocol (for RDID1/RDID2/RDID3 command: 8-bit read)



4-Pin Serial Protocol (for RDDID command: 24-bit read)



4-Pin Serial Protocol (for RDDST command: 32-bit read)

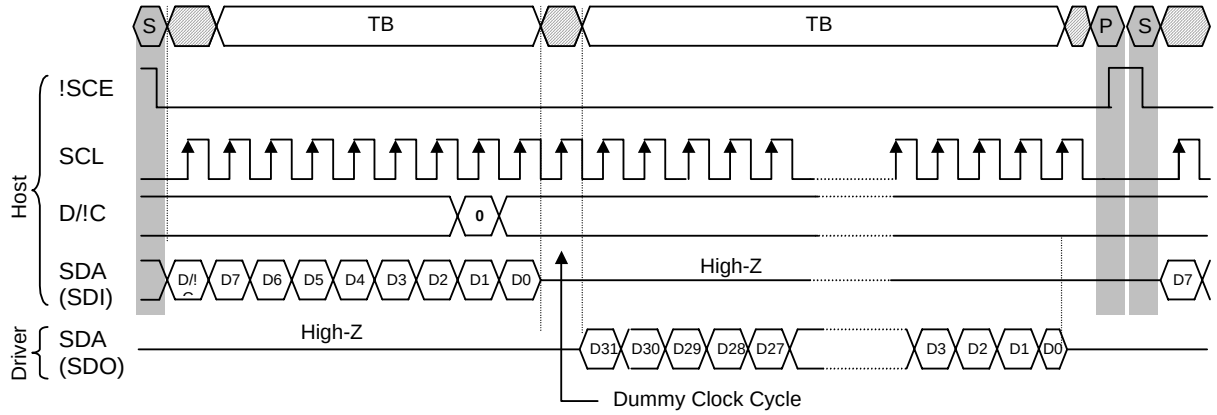


Fig. 5.1.6 Serial bus protocol, read mode (4-Pin serial interface case)

5.1.4 8080-Series Parallel Interface

The 8080-series bi-directional interface can be used for communication between the micro controller and the LCD driver chip. The selection of this interface is done when P68 pin is Low state (VSS). Interface bus width can be selected with BS1 and BS0.

The interface functions of the parallel interface (8080-series) are given in ***Table 5.1.3.***

Table 5.1.3 Parallel Interface Function (8080-series, P68="Low")

BS1	BS0	Interface	D/!C	8080-series		Function
				!RD	!WR	
0	1	8-bit interface	1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
			0	1	↑	Write 8-bit command (D7 to D0)
			1	↑	1	Read 8-bit display data (D7 to D0)
			1	↑	1	*1) Read 8-bit parameter or status (D7 to D0)
1	0	16-bit interface	1	1	↑	Write 16-bit display data (D15 to D0) or 8-bit parameter (D7 to D0)
			0	1	↑	Write 8-bit command (D7 to D0)
			1	↑	1	Read 16-bit display data (D15 to D0)
			1	↑	1	*1) Read 8-bit parameter or status (D7 to D0)
1	1	18-bit interface	1	1	↑	Write 18-bit display data (D17 to D0) or 8-bit parameter (D7 to D0)
			0	1	↑	Write 8-bit command (D7 to D0)
			1	↑	1	Read 18-bit display data (D17 to D0)
			1	↑	1	*1) Read 8-bit parameter or status (D7 to D0)

NOTE: "↑"= rising edge

**1) Applied for command code0 : DAh, DBh, DCh, 04h and 09h*

command code1: DAh, DBh and DCh

The parallel interface timing diagram is given in ***Fig. 5.1.7*** and ***Fig. 5.1.8.***

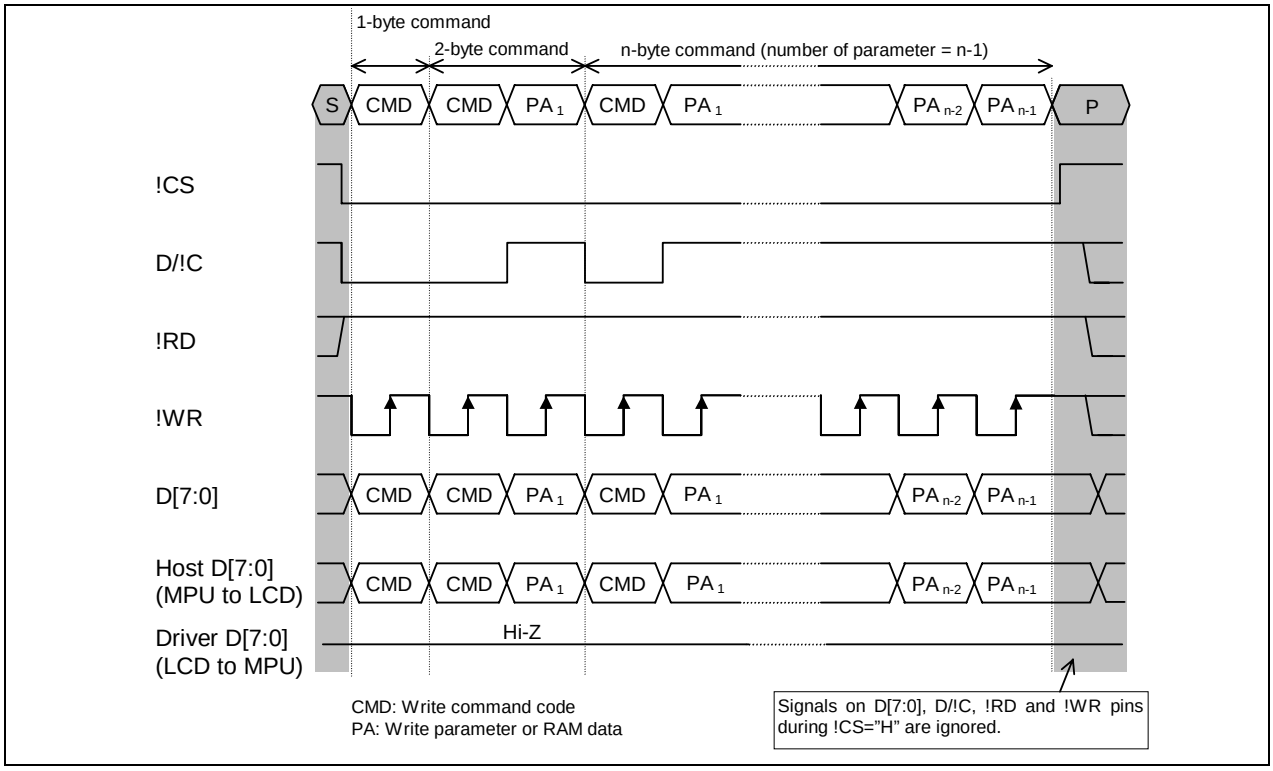


Fig. 5.1.7 8080-Series parallel bus protocol, write to register or display RAM

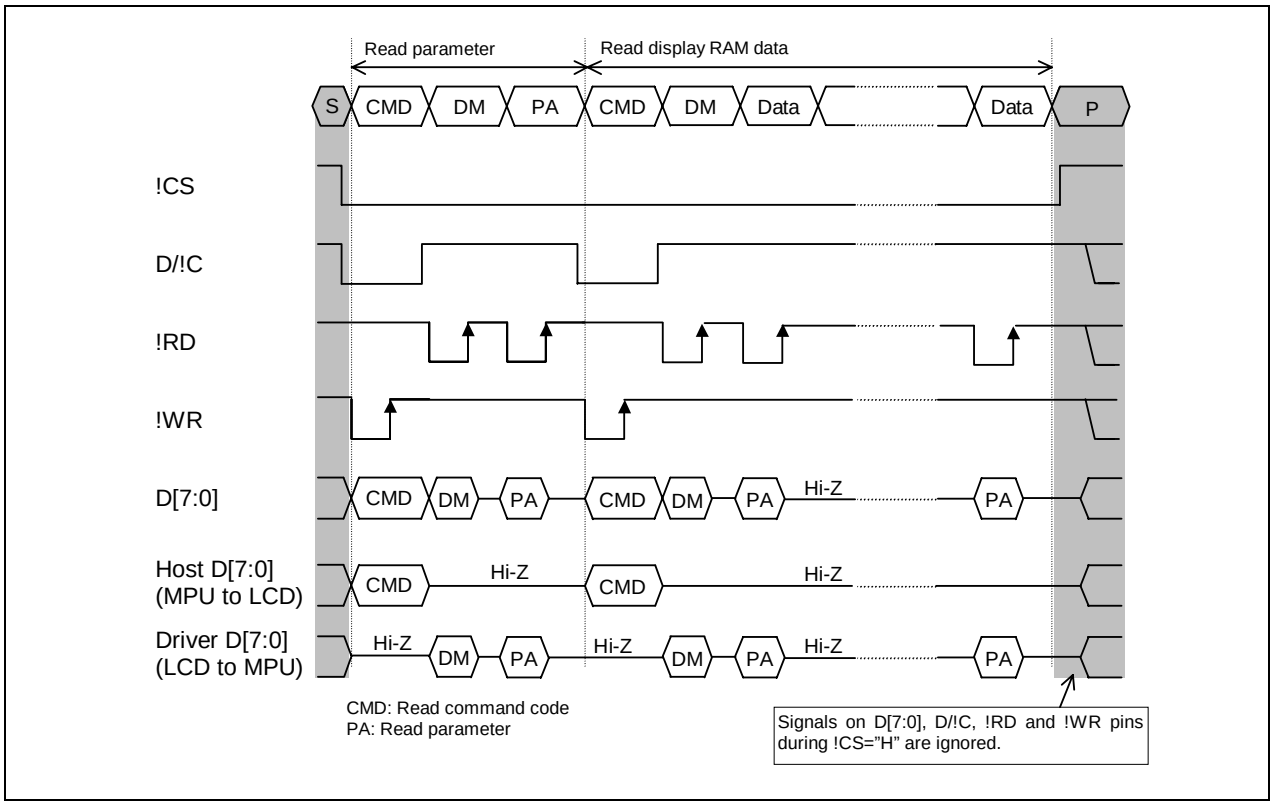


Fig. 5.1.8 8080-Series parallel bus protocol, read from register

5.1.5 6800-Series Parallel Interface

The 6800-series bi-directional interface can be used for communication between the micro controller and the LCD driver chip. The selection of this interface is done when P68 pin is High state (VDD1). Interface bus width can be selected with BS1 and BS0.

The interface functions of the parallel interface (6800-series) are given in ***Table 5.1.4.***

Table 5.1.4 Parallel Interface Function (6800-series, P68="High")

BS1	BS0	Interface	D/!C	6800-series		Function
				R/!W	R/!W	
0	1	8-bit interface	1	0	↓	Write 8-bit display data or 8-bit parameter (D7 to D0)
			0	0	↓	Write 8-bit command (D7 to D0)
			1	1	↓	Read 8-bit display data (D7 to D0)
			1	1	↓	*1) Read 8-bit parameter or status (D7 to D0)
1	0	16-bit interface	1	0	↓	Write 16-bit display data (D15 to D0) or 8-bit parameter (D7 to D0)
			0	0	↓	Write 8-bit command (D7 to D0)
			1	1	↓	Read 16-bit display data (D15 to D0)
			1	1	↓	*1) Read 8-bit parameter or status (D7 to D0)
1	1	18-bit interface	1	0	↓	Write 18-bit display data (D17 to D0) or 8-bit parameter (D7 to D0)
			0	0	↓	Write 8-bit command (D7 to D0)
			1	1	↓	Read 18-bit display data (D17 to D0)
			1	1	↓	*1) Read 8-bit parameter or status (D7 to D0)

NOTE: "↓"= falling edge

**1) Applied for command code0 : DAh, DBh, DCh, 04h and 09h*

command code1: DAh, DBh and DCh

The 6800-series parallel interface timing diagram is given in ***Fig. 5.1.9*** and ***Fig. 5.1.10***.

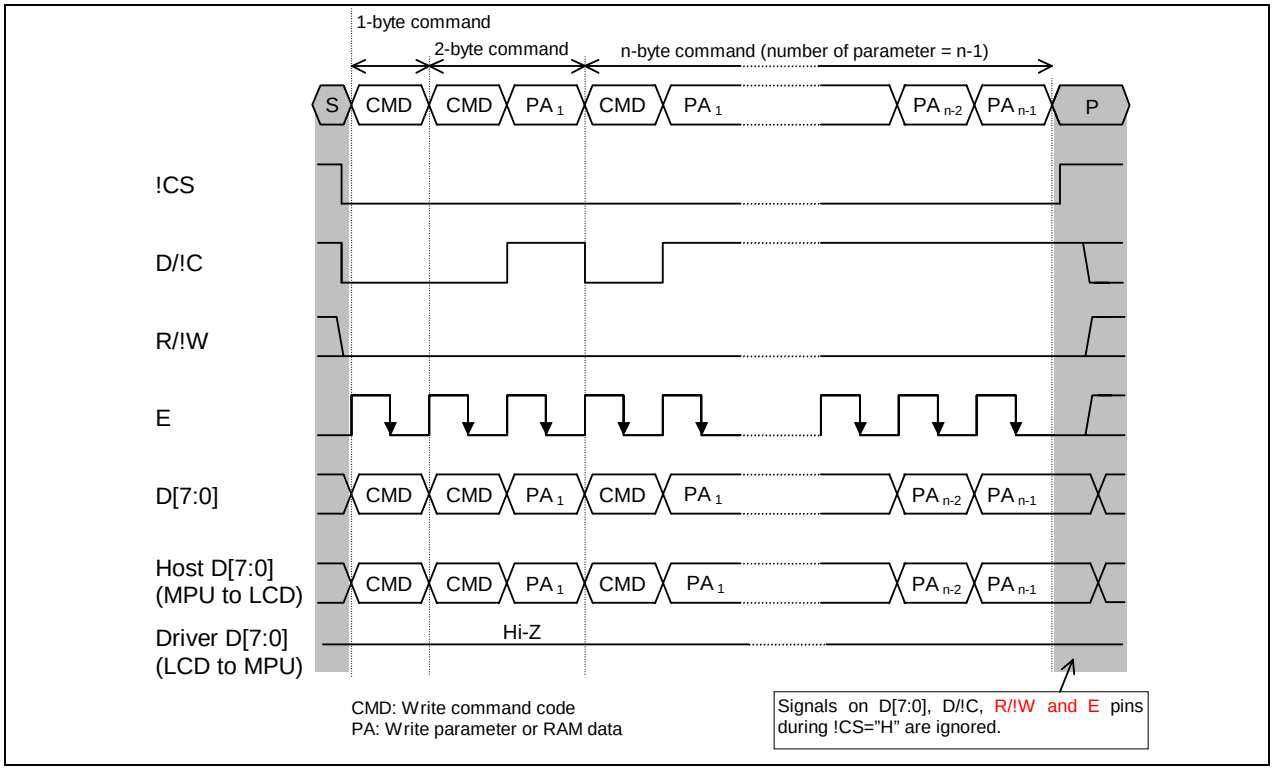


Fig. 5.1.9 6800-Series parallel bus protocol, write to register or display RAM

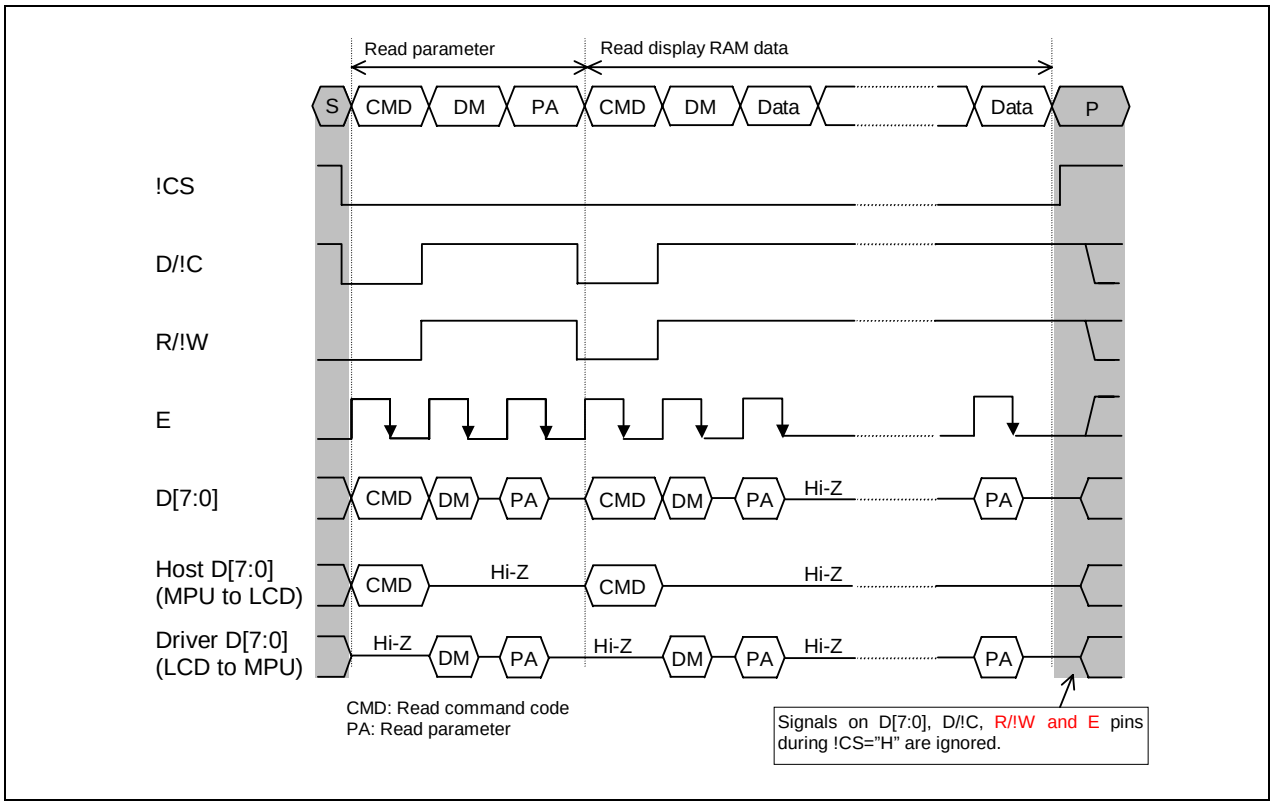


Fig. 5.1.10 6800-Series parallel bus protocol, read from register

5.1.6 Interface Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then LDS274 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

5.1.6.1 Parallel Interface Pause

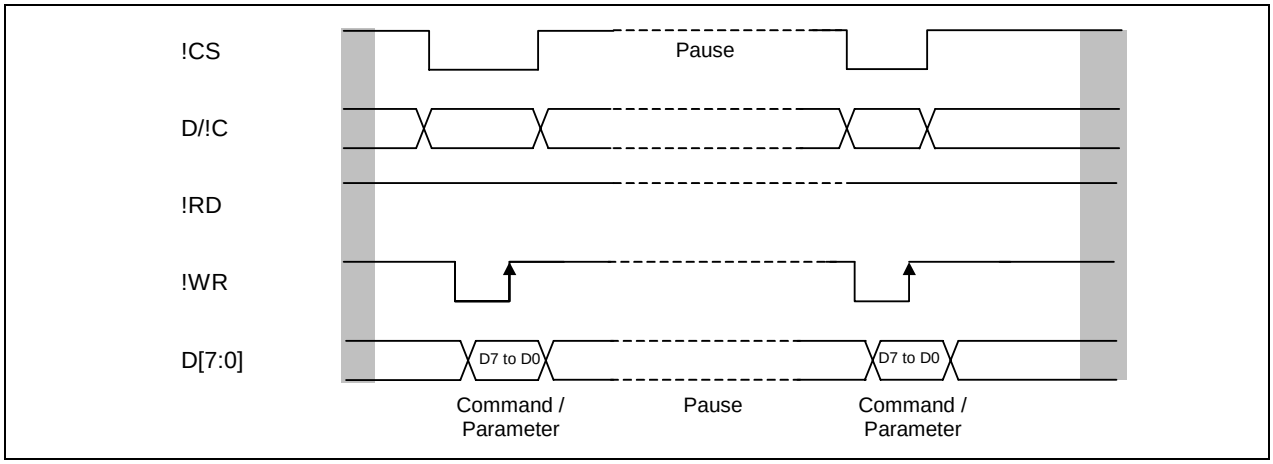


Fig. 5.1.11 Parallel bus protocol, write mode – paused by !CS

5.1.6.2 Serial Interface Pause

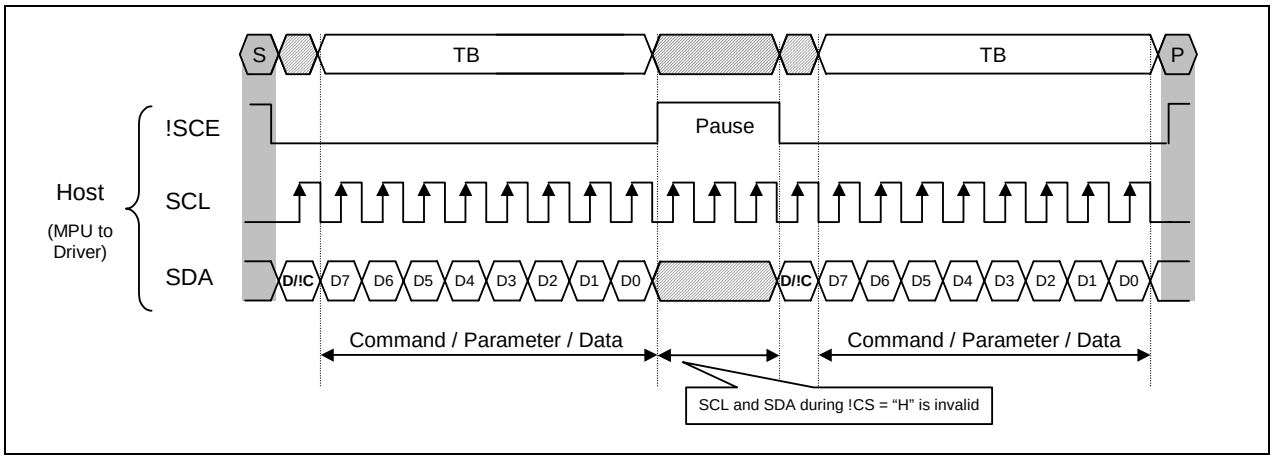


Fig. 5.1.12 Serial bus protocol, write mode – paused by !SCE (3-Pin serial case)

5.1.7 Data Transfer Recovery

If there is a break in data transmission by !RES pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then LDS274 will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (!SCE) is next activated after !RES have been High state. See the following example (See ***Fig. 5.1.13***)

If there is a break in data transmission by !SCE pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then LDS274 will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (!SCE) is next activated. See the following example (See ***Fig. 5.1.14***)

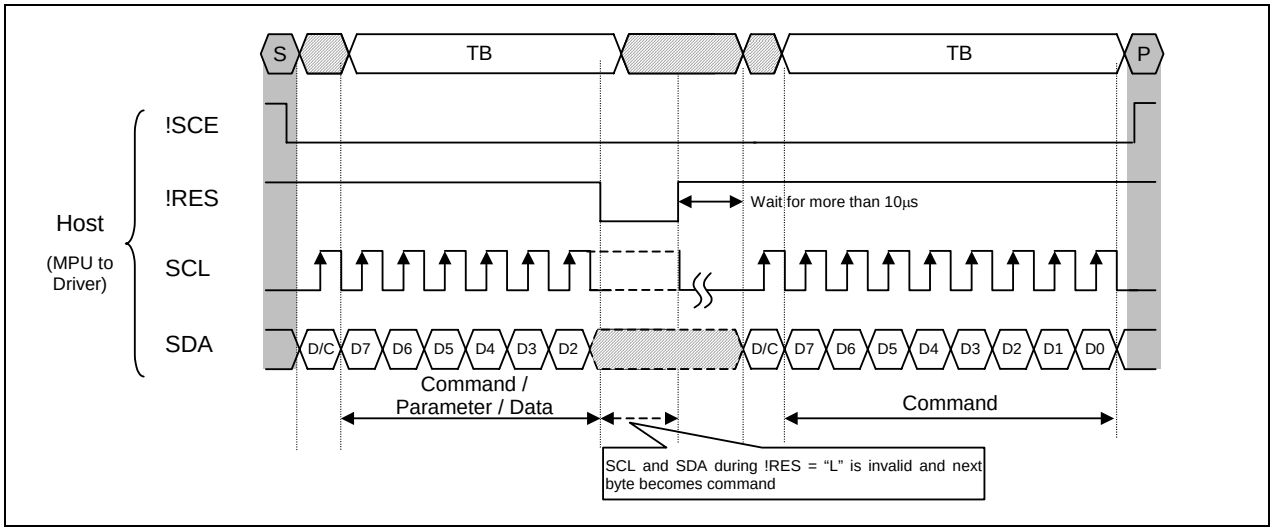


Fig. 5.1.13 Serial bus protocol, write mode – interrupted by !RES

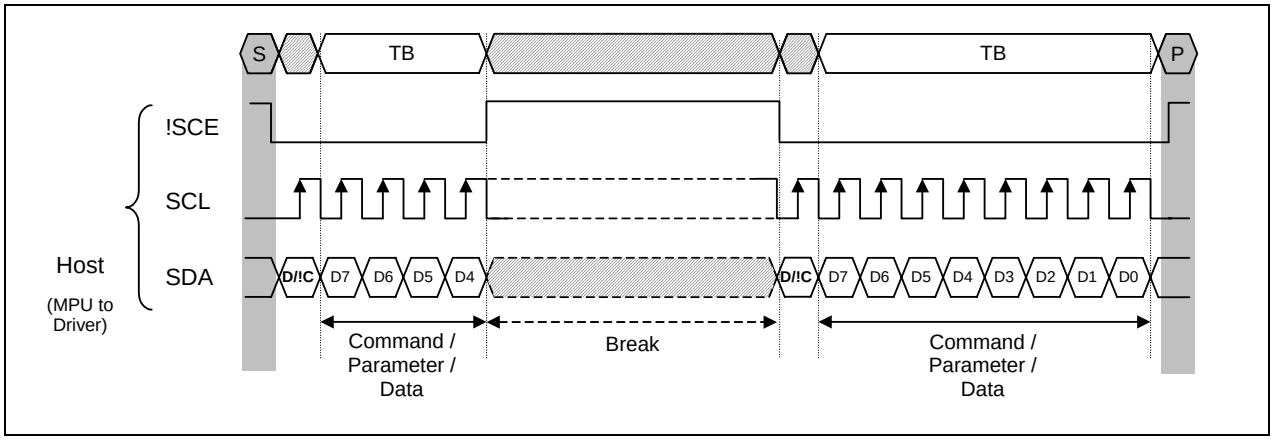


Fig. 5.1.14 Serial bus protocol, write mode – interrupted by !SCE

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown in ***Fig. 5.1.15***.

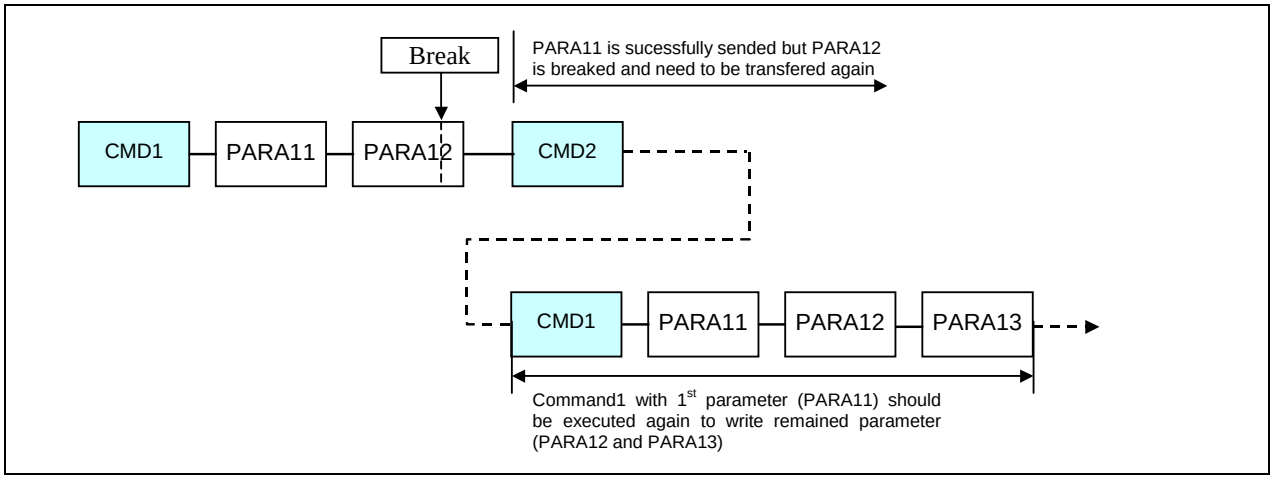


Fig. 5.1.15 Write interrupt recovery (serial interface)

If a 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

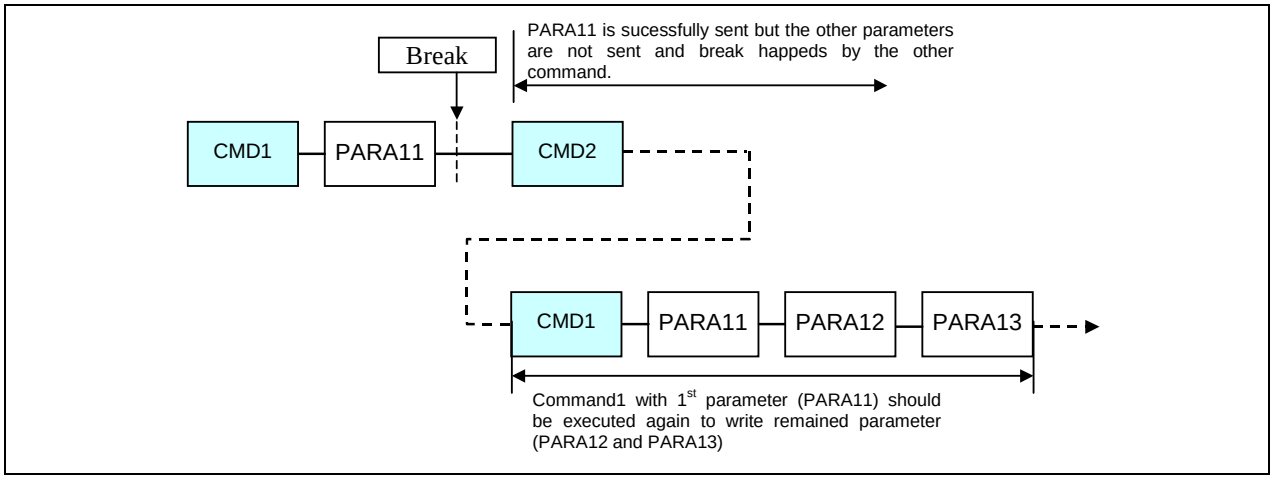


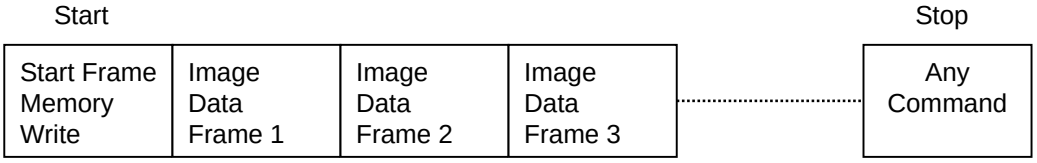
Fig. 5.1.16 Write interrupt recovery (both serial and parallel interface)

5.1.8 Display Module Data Transfer Modes

The Module has four kinds color modes for transferring data to the display RAM. These are 8-bit color per pixel, 12-bit color per pixel, 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

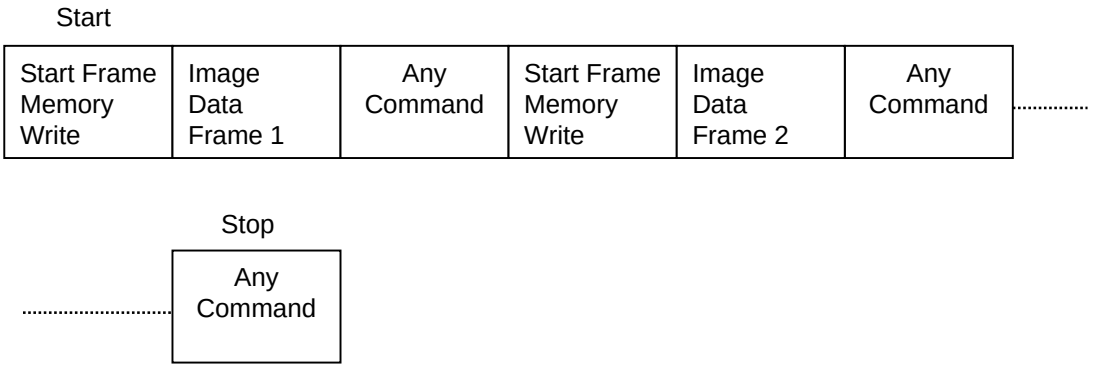
5.1.8.1 Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



5.1.8.2 Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



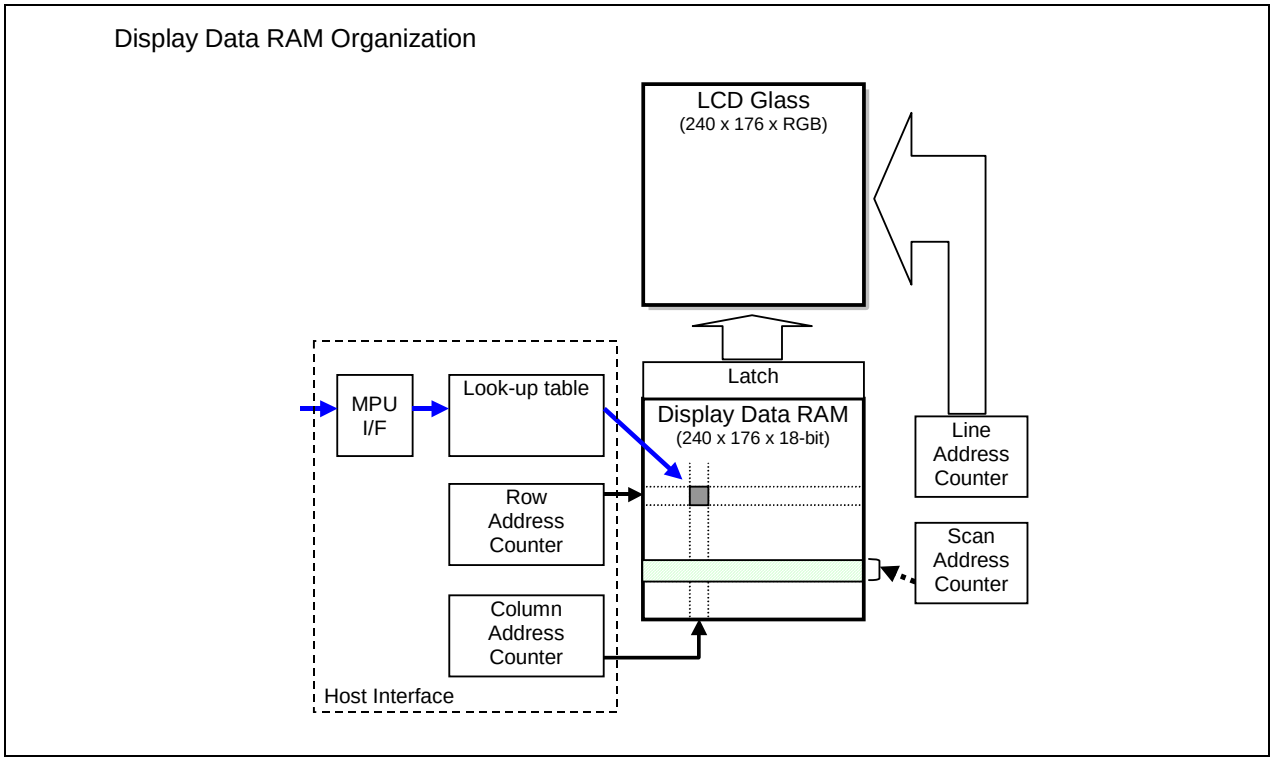
Note:

1) These apply to all Data Transfer Color modes on both Serial and Parallel interfaces.

2) The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

5.2 DISPLAY DATA RAM (DDRAM)

The LDS274 has an integrated 240x176x18-bit graphic type static RAM. This 760k-bit memory allows to store on-chip a 240x176 (RGB) image with a 18-bpp resolution (262k-color).



5.2.1 Display Data Formats

5.2.1.1 LSB Expanding for Red and Blue Data

LDS274 has 18-bit graphic memory, so in 65k color mode (16-bit data) data bit should be expended to 18-bit like below.

16-bit Data (Transferred data)	D15 (R4)	D14 (R3)	D13 (R2)	D12 (R1)	D11 (R0)		D10 (G5)	D9 (G4)	D8 (G3)	D7 (G2)	D6 (G1)	D5 (G0)	D4 (B4)	D3 (B3)	D2 (B2)	D1 (B1)	D0 (B0)	
LSB Expanding	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
18-bit Data (Frame Memory)	D17 (R5)	D16 (R4)	D15 (R3)	D14 (R2)	D13 (R1)	D12 (R0)	D11 (G5)	D10 (G4)	D9 (G3)	D8 (G2)	D7 (G1)	D6 (G0)	D5 (B5)	D4 (B4)	D3 (B3)	D2 (B2)	D1 (B1)	D0 (B0)

5.2.1.2 Serial or 8-Bit Parallel Interface Mode

Different display data formats are available for three colors depth supported by the LDS274 listed below.

256 colors, RGB 3-3-2-bits input (see ***Table 5.2.1***)

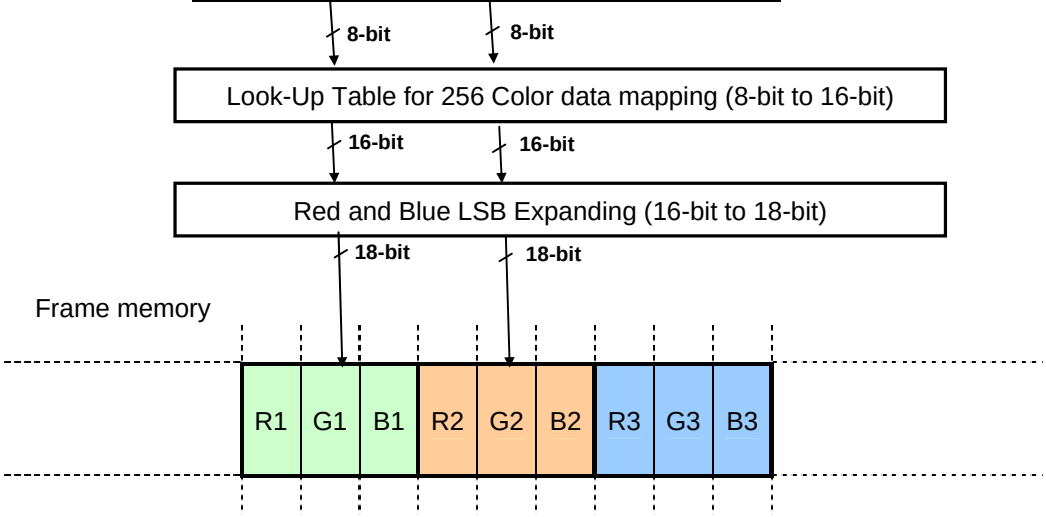
4k colors, RGB 4-4-4-bits input (see ***Table 5.2.2***)

65k colors, RGB 5-6-5-bits input (see ***Table 5.2.3***)

262k colors, RGB 6-6-6-bits input (see ***Table 5.2.4***)

Table 5.2.1 Write data for RGB 3-3-2-bits input

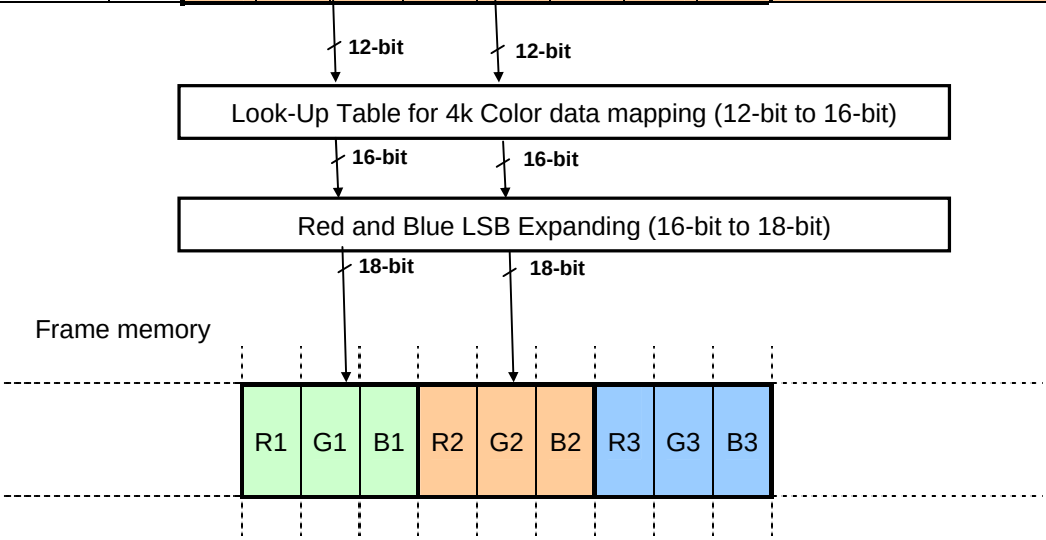
256 Color data	D/!C	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	Memory Write Command Code								-
1st write	1	$R1_2$	$R1_1$	$R1_0$	$G1_2$	$G1_1$	$G1_0$	$B1_1$	$B1_0$	1st pixel data write (R1/G1/B1)
2nd write	1	$R2_2$	$R2_1$	$R2_0$	$G2_2$	$G2_1$	$G2_0$	$B2_1$	$B2_0$	2nd pixel data write (R2/G2/B2)



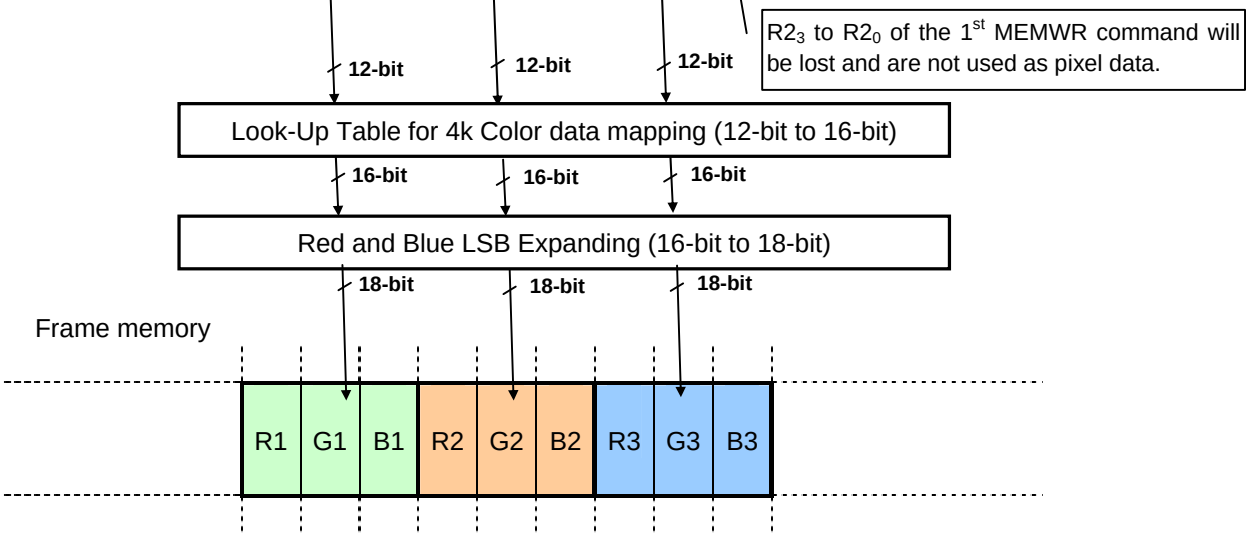
NOTE: In one transfer, 1 pixel data is transmitted with the 8-bit color depth information.
The most significant bits are: Rx_2, Gx_2 and Bx_1.
The least significant bits are: Rx_0, Gx_0 and Bx_0.

Table 5.2.2 Write data for RGB 4-4-4-bits input

4k Color data	D/!C	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	Memory Write Command Code								-
1st write	1	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	-
2nd write	1	$B1_3$	$B1_2$	$B1_1$	$B1_0$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	1st pixel data write (R1/G1/B1)
3rd write	1	$G2_3$	$G2_2$	$G2_1$	$G2_0$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel data write (R2/G2/B2)



4k Color data	D/!C	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	Memory Write Command Code								-
1st write	1	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	-
2nd write	1	$B1_3$	$B1_2$	$B1_1$	$B1_0$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	1st pixel data write (R1/G1/B1)
CMD	0	The other command								Memory write mode terminated
MEMWR	0	Memory Write Command Code								-
1st write	1	$R2_3$	$R2_2$	$R2_1$	$R2_0$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	-
2nd write	1	$B2_3$	$B2_2$	$B2_1$	$B2_0$	$R3_3$	$R3_2$	$R3_1$	$R3_0$	2nd pixel data write (R2/G2/B2)
3rd write	1	$G3_3$	$G3_2$	$G3_1$	$G3_0$	$B3_3$	$B3_2$	$B3_1$	$B3_0$	3rd pixel data write (R3/G3/B3)



NOTE: 3 times transfer is used to transmit 2 pixels data or 2 times transfer are used to transmit 1 pixel data with the 12-bit color depth information.

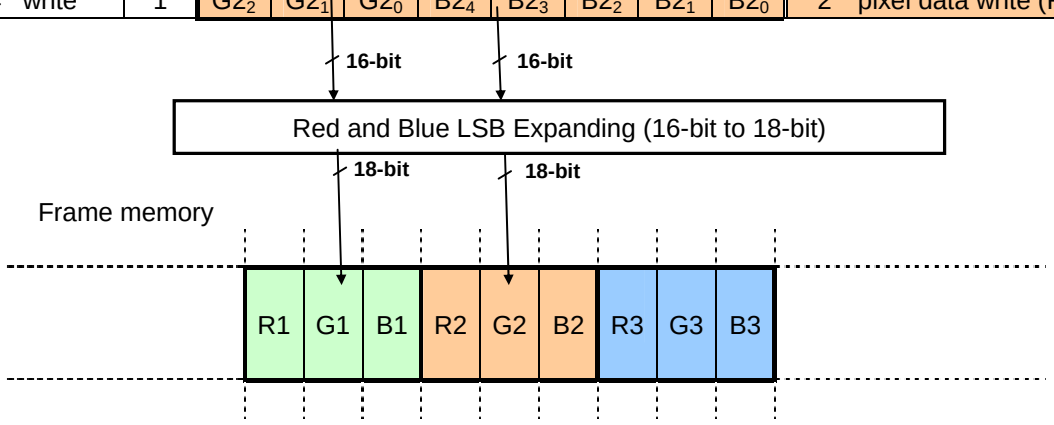
The most significant bits are: Rx_3, Gx_3 and Bx_3.

The least significant bits are: Rx_0, Gx_0 and Bx_0.

Only complete pixels are stored to the frame memory.

Table 5.2.3 Write data for RGB 5-6-5-bits input

65k Color data	D/!C	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	Memory Write Command Code								-
1st write		$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_5$	$G1_4$	$G1_3$	-
2nd write	1	$G1_2$	$G1_1$	$G1_0$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	1st pixel data write (R1/G1/B1)
3rd write		$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	$G2_5$	$G2_4$	$G1_3$	-
4th write	1	$G2_2$	$G2_1$	$G2_0$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel data write (R2/G2/B2)

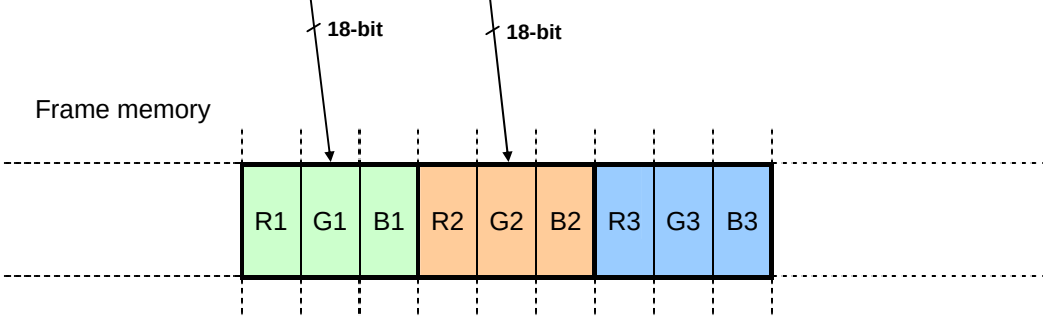


NOTE: 2 times transfer is used to transmit 1 pixel data with the 16-bit color depth information.
The most significant bits are: Rx4, Gx5 and Bx4.
The least significant bits are: Rx0, Gx0 and Bx0.

Table 5.2.4 Write data for RGB 6-6-6-bits input

"X" : Don't care

262k Color data	D/!C	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	Memory Write Command Code								-
1st write	1	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	x	x	-
2nd write	1	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	x	x	-
3rd write	1	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	x	x	1st pixel data write (R1/G1/B1)
4th write	1	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	x	x	-
5th write	1	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	x	x	-
6th write	1	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	x	x	2nd pixel data write (R2/G2/B2)



NOTE: 3 times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
The most significant bits are: Rx5, Gx5 and Bx5.
The least significant bits are: Rx0, Gx0 and Bx0.

5.2.1.3 16-Bit Parallel Interface Mode

Different display data formats are available for three colors depth supported by the LDS274 listed below.

256 colors, RGB 3-3-2-bits input (see ***Table 5.2.5***)

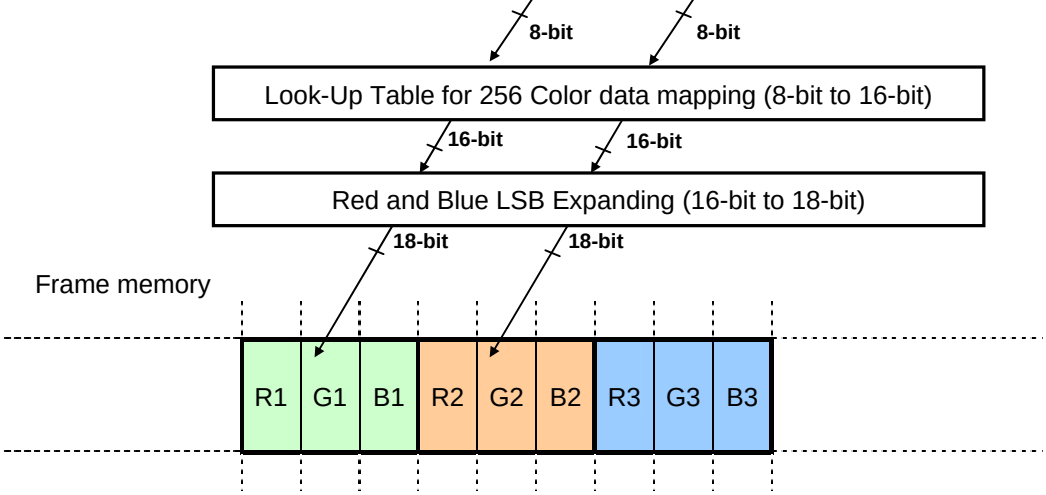
4k colors, RGB 4-4-4-bits input (see ***Table 5.2.6***)

65k colors, RGB 5-6-5-bits input (see ***Table 5.2.7***)

Table 5.2.5 Write data for RGB 3-3-2-bits input in 16-bit parallel Interface

"X" : Don't care

8 Color data	D/!C	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	x								Memory Write Command Code								-
1st write	1	x	x	x	x	x	x	x	x	$R1_2$	$R1_1$	$R1_0$	$G1_2$	$G1_1$	$G1_0$	$B1_1$	$B1_0$	1st pixel (R1/G1/B1)
2nd write	1	x	x	x	x	x	x	x	x	$R2_2$	$R2_1$	$R2_0$	$G2_2$	$G2_1$	$G2_0$	$B2_1$	$B2_0$	2nd pixel (R2/G2/B2)



NOTE: In one transfer (D7 to D0), 1 pixel data is transmitted with the 8-bit color depth information.

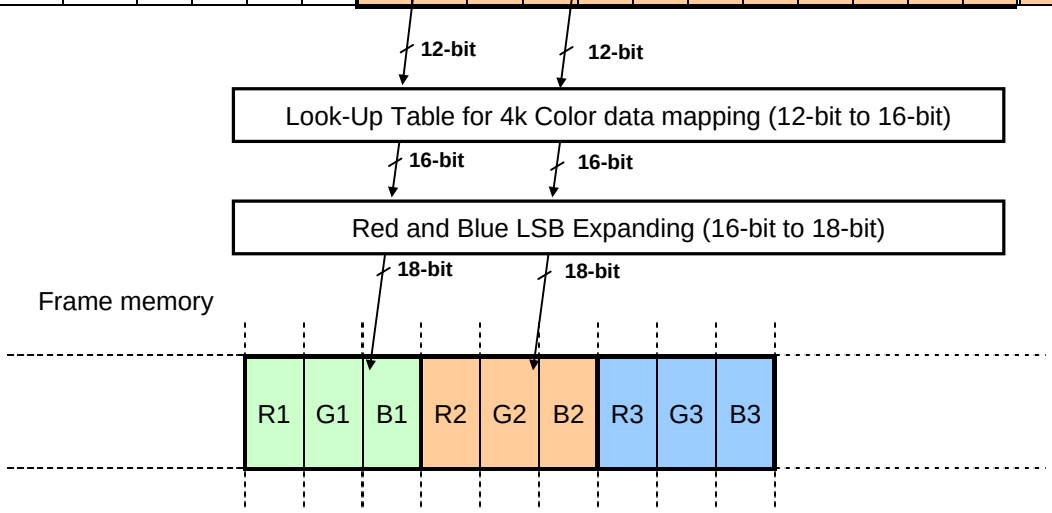
The most significant bits are: Rx_2, Gx_2 and Bx_1.

The least significant bits are: Rx_0, Gx_0 and Bx_0.

Table 5.2.6 Write data for RGB 4-4-4-bits input in 16-bit parallel Interface

"X" : Don't care

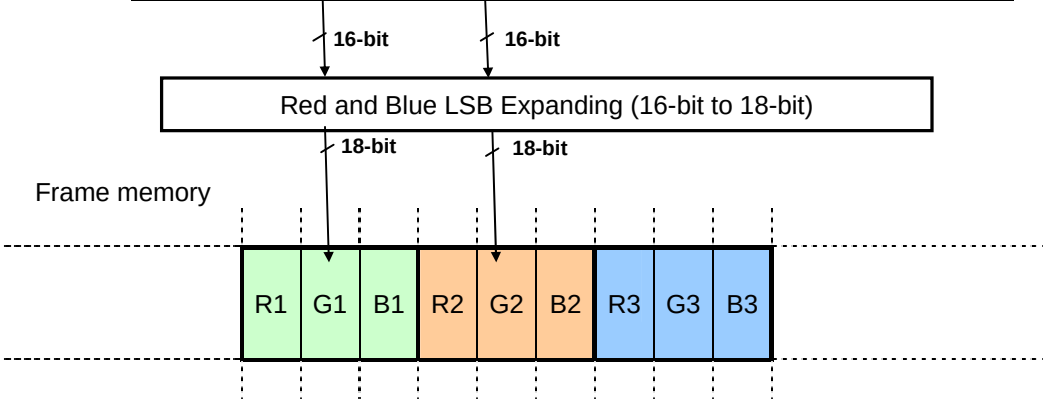
4k Color data	D/!C	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	x								Memory Write Command Code								-
1st write	1	x	x	x	x	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	1st pixel (R1/G1/B1)
2nd write	1	x	x	x	x	$R2_3$	$R2_2$	$R2_1$	$R2_0$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel (R2/G2/B2)



NOTE: In one transfer (D11 to D0), 1 pixel data is transmitted with the 12-bit color depth information.
The most significant bits are: Rx_3, Gx_3 and Bx_3.
The least significant bits are: Rx_0, Gx_0 and Bx_0.
Only complete pixels are stored to the frame memory.

Table 5.2.7 Write data for RGB 5-6-5-bits input in 16-bit parallel Interface

65k Color data	D/!C	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	x								Memory Write Command Code								-
1st write	1	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	1st pixel (R1/G1/B1)
2nd write	1	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel (R2/G2/B2)



NOTE: In one transfer (D15 to D0), 1 pixel data is transmitted with the 16-bit color depth information.
The most significant bits are: Rx4, Gx5 and Bx4.
The least significant bits are: Rx0, Gx0 and Bx0.

5.2.1.4 18-Bit Parallel Interface Mode

Different display data formats are available for four colors depth supported by the LDS274 listed below.

256 colors, RGB 3-3-2-bits input (see ***Table 5.2.8***)

4k colors, RGB 4-4-4-bits input (see ***Table 5.2.9***)

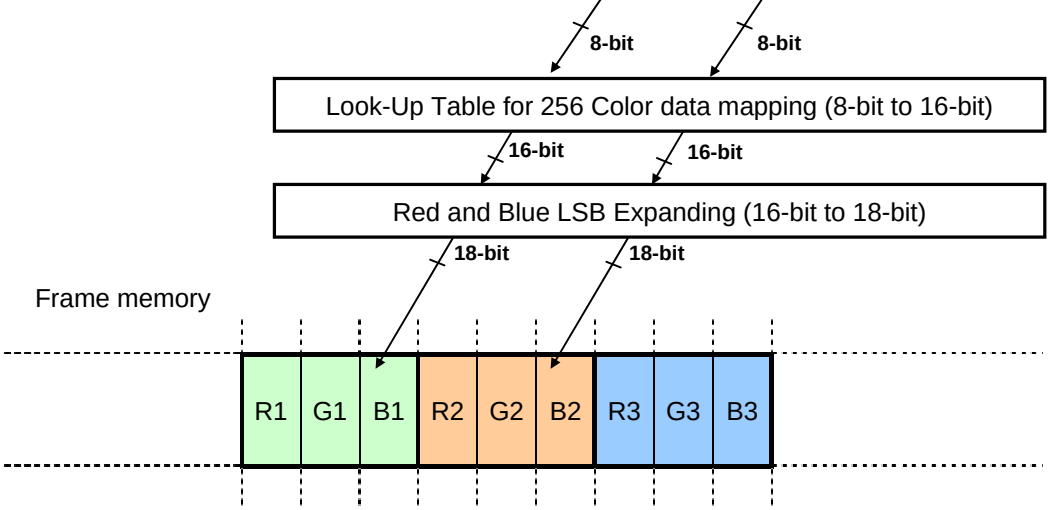
65k colors, RGB 5-6-5-bits input (see ***Table 5.2.10***)

262k colors, RGB 6-6-6-bits input (see ***Table 5.2.11***)

Table 5.2.8 Write data for RGB 3-3-2-bits input in 18-bit parallel Interface

"X" : Don't care

8 Color data	D/!C	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	x										Memory Write Command Code								-
1st write	1	x	x	x	x	x	x	x	x	x		$R1_2$	$R1_1$	$R1_0$	$G1_2$	$G1_1$	$G1_0$	$B1_1$	$B1_0$	1st pixel (R1/G1/B1)
2nd write	1	x	x	x	x	x	x	x	x	x		$R2_2$	$R2_1$	$R2_0$	$G2_2$	$G2_1$	$G2_0$	$B2_1$	$B2_0$	2nd pixel (R2/G2/B2)

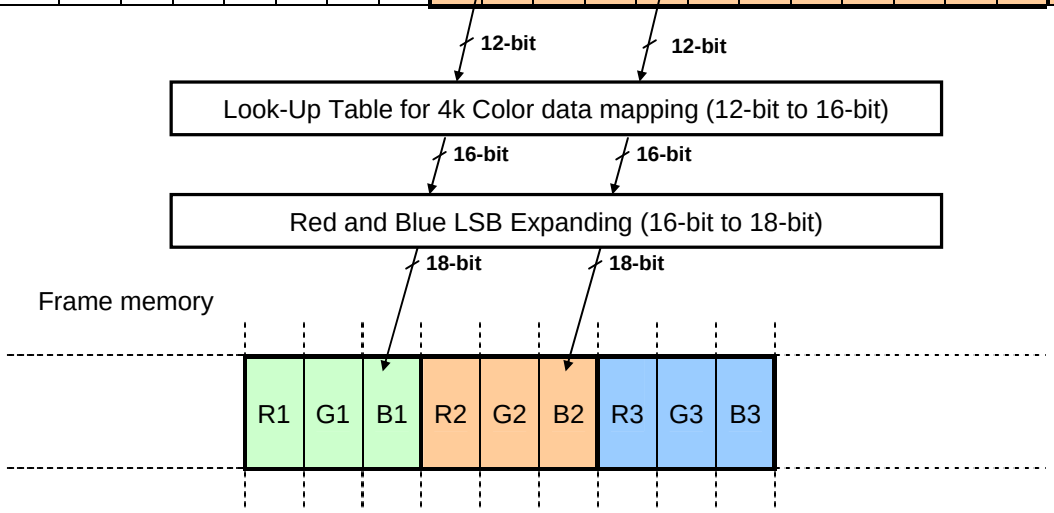


NOTE: In one transfer (D7 to D0), 1 pixel data is transmitted with the 8-bit color depth information.
The most significant bits are: Rx_2, Gx_2 and Bx_1.
The least significant bits are: Rx_0, Gx_0 and Bx_0.

Table 5.2.9 Write data for RGB 4-4-4-bits input in 18-bit parallel Interface

"X" : Don't care

4k Color data	D/!C	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	x										Memory Write Command Code								-
1st write	1	x	x	x	x	x	x	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	1st pixel (R1/G1/B1)
2nd write	1	x	x	x	x	x	x	$R2_3$	$R2_2$	$R2_1$	$R2_0$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel (R2/G2/B2)

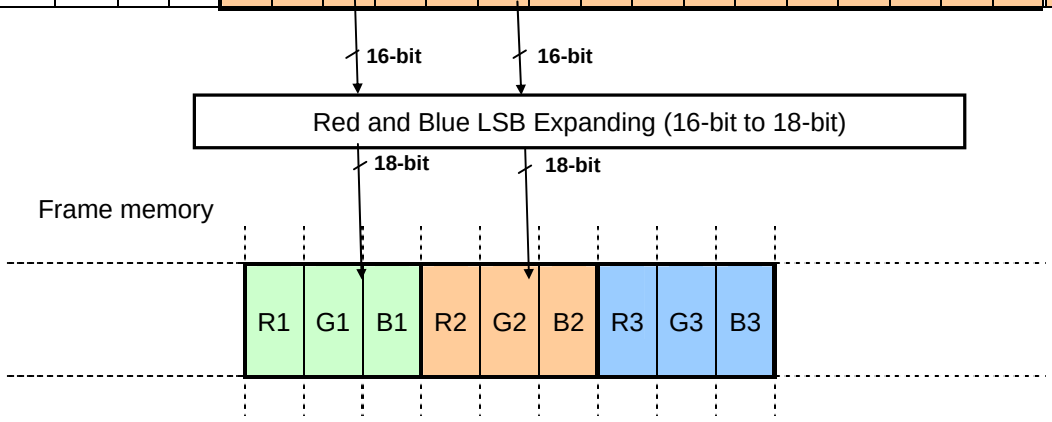


NOTE: In one transfer (D11 to D0), 1 pixel data is transmitted with the 12-bit color depth information.
The most significant bits are: Rx_3, Gx_3 and Bx_3.
The least significant bits are: Rx_0, Gx_0 and Bx_0.
Only complete pixels are stored to the frame memory.

Table 5.2.10 Write data for RGB 5-6-5-bits input in 18-bit parallel Interface

"X" : Don't care

65k Color data	D/!C	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	x										Memory Write Command Code								-
1st write	1	x	x	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	1st pixel (R1/G1/B1)
2nd write	1	x	x	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel (R2/G2/B2)

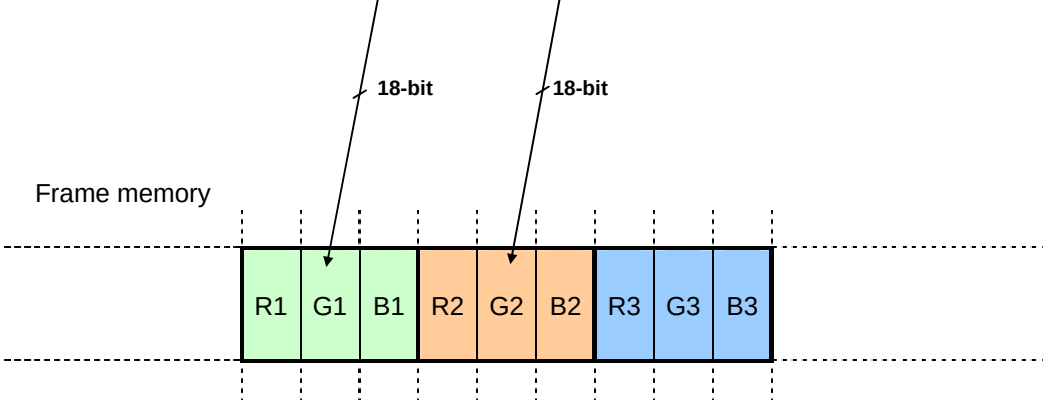


NOTE: In one transfer (D15 to D0), 1 pixel data is transmitted with the 16-bit color depth information.
The most significant bits are: Rx4, Gx5 and Bx4.
The least significant bits are: Rx0, Gx0 and Bx0.

Table 5.2.11 Write data for RGB 6-6-6-bits input in 18-bit parallel Interface

"X" : Don't care

262k Color data	D/!C	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Memory Write
MEMWR	0	x										Memory Write Command Code								-
1st write	1	$R1_5$	$R1_4$	$R1_3$	$R1_2$	$R1_1$	$R1_0$	$G1_5$	$G1_4$	$G1_3$	$G1_2$	$G1_1$	$G1_0$	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	1st pixel (R1/G1/B1)
2nd write	1	$R2_5$	$R2_4$	$R2_3$	$R2_2$	$R2_1$	$R2_0$	$G2_5$	$G2_4$	$G2_3$	$G2_2$	$G2_1$	$G2_0$	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	2nd pixel (R2/G2/B2)



NOTE: In one transfer (D17 to D0), 1 pixel data is transmitted with the 18-bit color depth information.
The most significant bits are: Rx5, Gx5 and Bx5.
The least significant bits are: Rx0, Gx0 and Bx0.

5.2.2 RGB Interface

For direct interface with both graphic controller and MPU, LDS274 offer RGB interface mode to display video signal. In RGB interface mode, video data bus becomes (VD17 to VD0) and controller can write 18-bit RGB data to predefined row and column address area (by CASET and RASET command) of the frame memory. Command and parameter to control LDS274 can be accessed by MPU via D17 to D0 pad as serial, 8-bit, 16-bit or 18-bit 8080- or 6800-series interface mode.

5.2.2.1 RGB Interface Bus Width Set

All 3-kinds of bus width can be available during RGB interface mode (selected by the 2nd parameter of IFMODE command: DW1, DW0).

DW1	DW0	VD17	VD16	VD15	VD14	VD13	VD12	VD11	VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Bus Width
0	0	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bit data
0	1	R4	R3	R2	R1	R0	x	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	x	16-bit data
1	0	x	x	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	6-bit data
		x	x	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	
		x	x	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	

NOTE: Unused RGB data bus can be opened or connected with VDD1 or VSS.

5.2.2.2 RGB Interface Mode Set

All 3-kinds of RGB interface mode can be available to fit the various controller type.

RGB I/F Mode	DCK	ENABLE	Video Data Bus VD17 to VD0	VSYNC	VSYNCO	HSYNC	Reference clock for display
RGB Mode1	Used	Used	Used	Not used	Used	Not used	Internal Oscillator
RGB Mode2	Used	Used	Used	Used	Not used	Not used	Internal Oscillator
RGB Mode3	Used	Used	Used	Used	Not used	Used	DCK

NOTE: Unused RGB data bus or control pins can be opened or connected with VDD1 or VSS.

RGB Interface Mode1

Data write to the frame memory is done by DCK and Video Data Bus (VD17 to VD0) when ENABLE is Low state.
To make the internal displaying clock, internal oscillator is used. So, to write the video data without flickering, controller need to transfer the data with synchronous to the VSYNCO output signal.

RGB Interface Mode2

Data write to the frame memory is done by DCK and Video Data Bus (VD17 to VD0) when ENABLE is Low state.
To make the internal displaying clock, internal oscillator is used. But frame display starts with synchronous to VSYNC input. So, to write the video data without flickering, controller must always transfer VSYNC signal to LDS274.

RGB Interface Mode3

Data write to the frame memory is done by DCK and Video Data Bus (VD17 to VD0) when ENABLE is Low state.
To make the internal displaying clock, external clocks (DCK, VSYNC and HSYNC) are used. So, controller must always transfer DCK, VSYNC and HSYNC signal to LDS274.

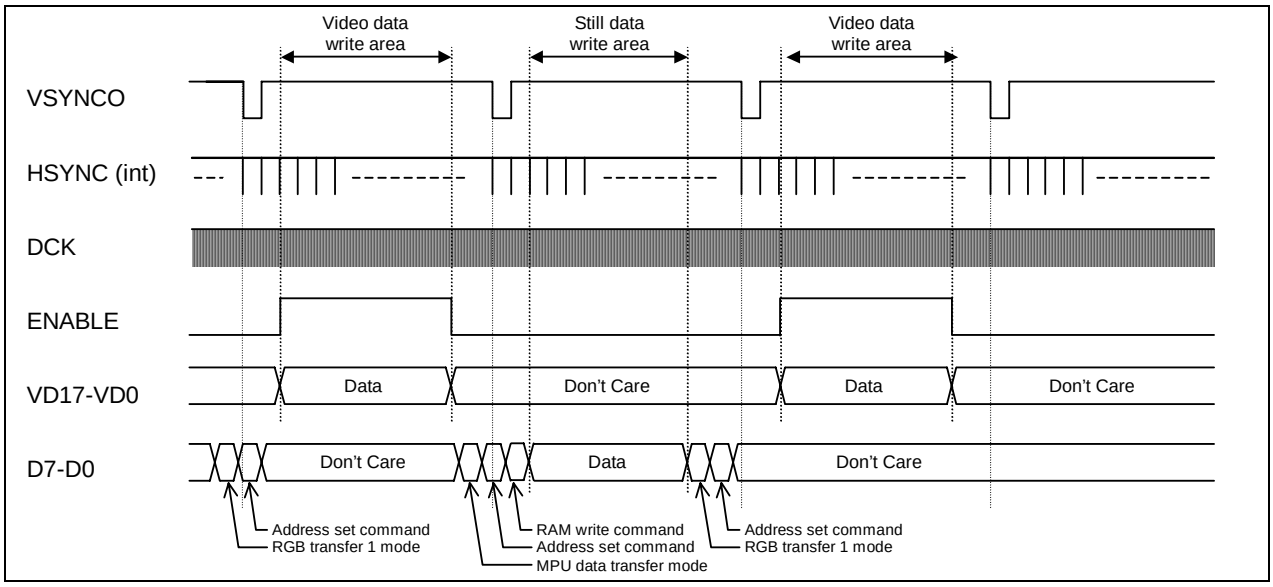


Fig. 5.2.1 An example to overwrite still picture data during moving picture display (RGB Interface Mode1)

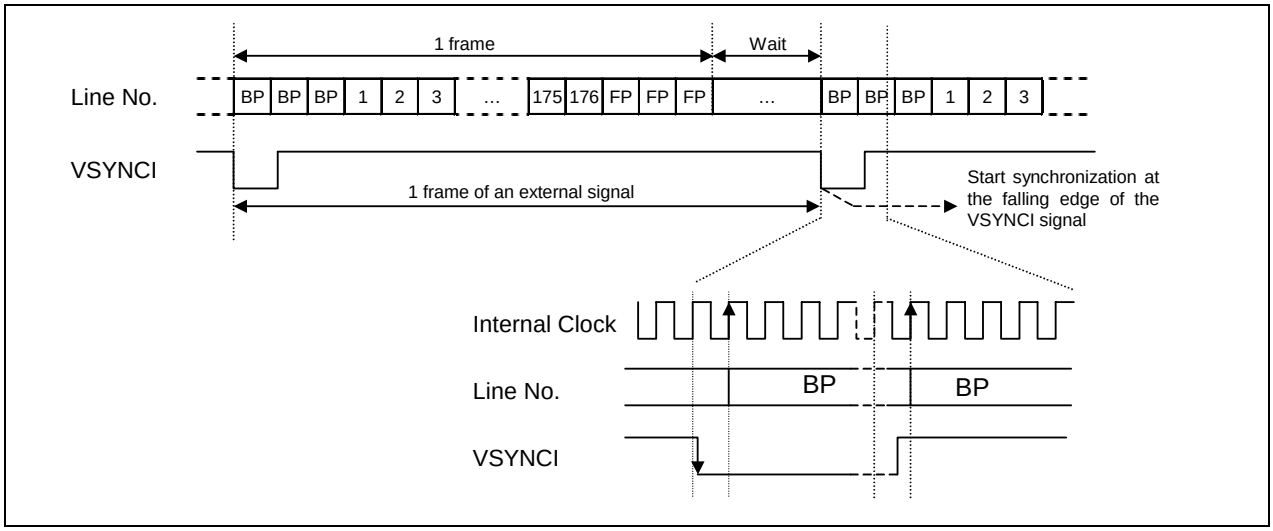


Fig. 5.2.2 An example of RGB Interface Mode2

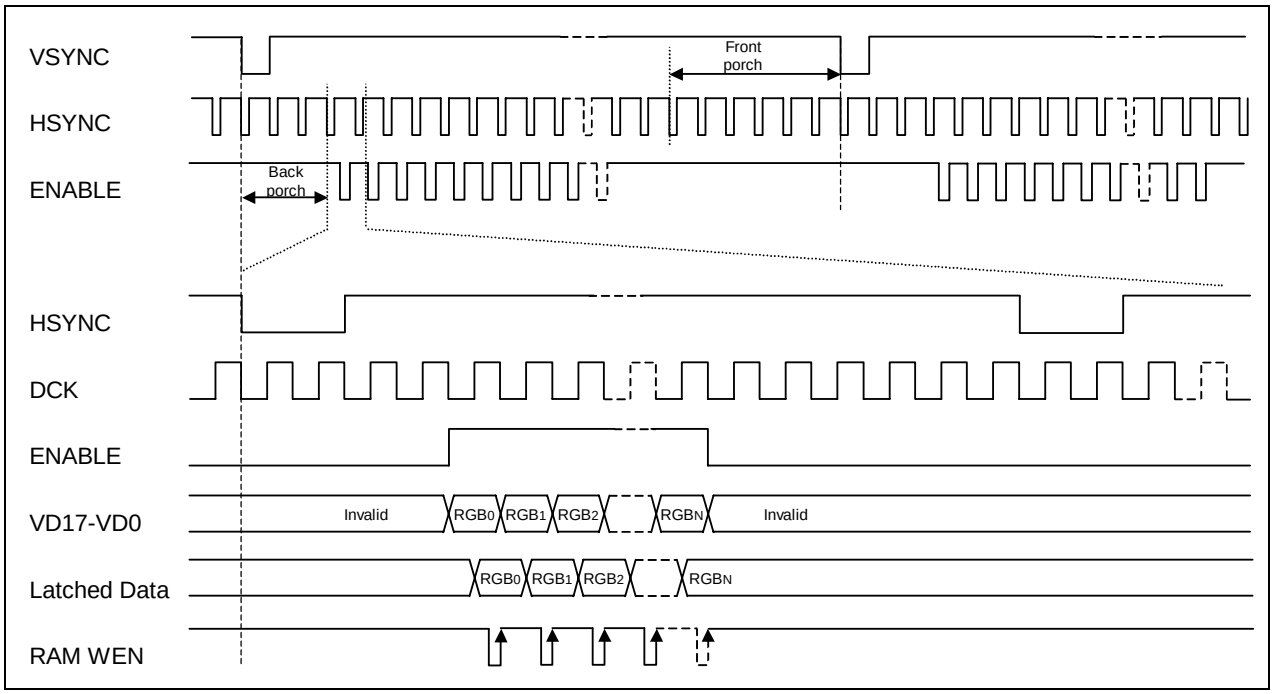


Fig. 5.2.3 Video signal data writing method in RGB Interface Mode 3

5.2.3 Address Counter

The address counter sets the addresses of the display data RAM for writing.

Data is written pixel-wise into the RAM matrix of LDS274. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=175 (AF h) and Y=0 to Y=239 (EF h). Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined into which will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=175 (AF h), YE=239 (EF h).

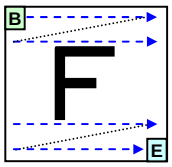
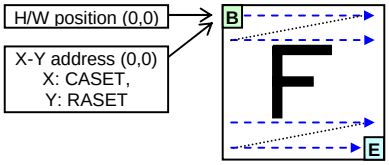
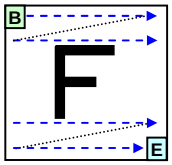
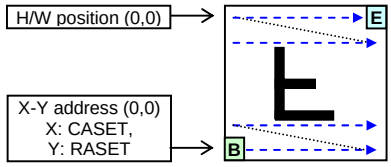
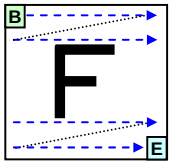
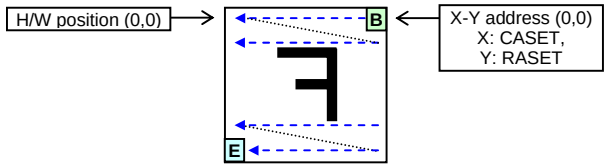
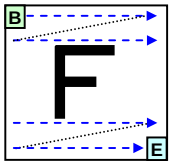
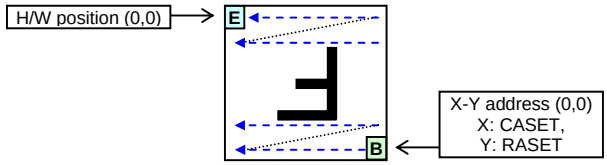
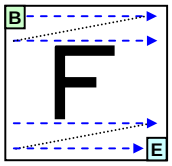
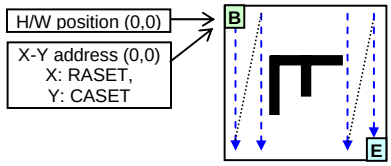
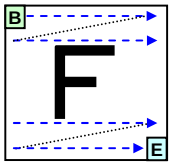
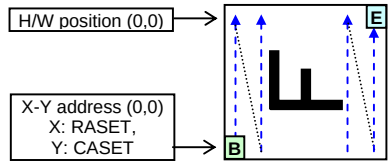
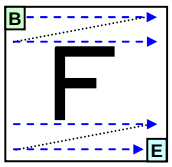
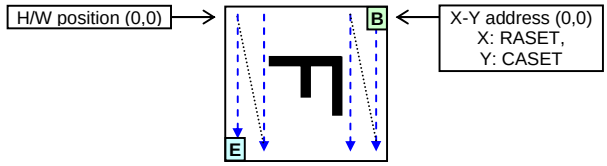
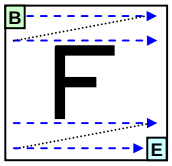
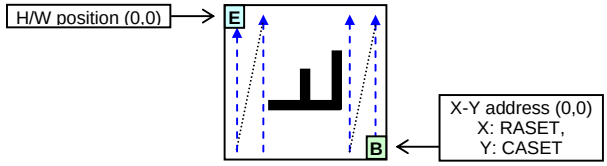
In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTL" (see section "6 INSTRUCTION DESCRIPTION"), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. ***Fig .5.2.4*** show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below:

Condition	Column Counter	Row Counter
When RAMWR command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

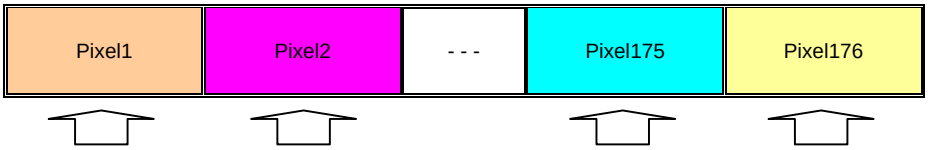
Fig. 5.2.4 Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

NOTE: MV=D5 parameter of MADCTL command, MX=D6 parameter of MADCTL command, MY=D7 parameter of MADCTL command

5.2.4 Memory Map

5.2.4.1 240 Gate Output Mode (GM1="H", GM0="L")



Source Out	S1	S2	S3	S4	S5	S6	- - -	S523	S524	S525	S526	S527	S528	
	RGB=0 / RGB=1						RGB Order							
RA MY=0	RA MY=1													SA ML=0 / SA ML=1
0	239	R0$_{5-0}$	G0$_{5-0}$	B0$_{5-0}$	R1$_{5-0}$	G1$_{5-0}$	B1$_{5-0}$	- - -	R174$_{5-0}$	G174$_{5-0}$	B174$_{5-0}$	R175$_{5-0}$	G175$_{5-0}$	B175$_{5-0}$	0 / 239
1	238							- - -							1 / 238
2	237							- - -							2 / 237
3	236							- - -							3 / 236
4	235							- - -							4 / 235
5	234							- - -							5 / 234
6	233							- - -							6 / 233
7	232							- - -							7 / 232
8	231							- - -							8 / 231
9	230							- - -							9 / 230
10	229							- - -							10 / 229
11	228							- - -							11 / 228
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	: / :
232	7							- - -							232 / 7
233	6							- - -							233 / 6
234	5							- - -							234 / 5
235	4							- - -							235 / 4
236	3							- - -							236 / 3
237	2							- - -							237 / 2
238	1							- - -							238 / 1
239	0							- - -				RN$_{5-0}$	GN$_{5-0}$	BN$_{5-0}$	239 / 0
CA	MX=0	0			1			- - -	174			175			
	MX=1	175			174			- - -	1			0			

NOTE: RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command
ML = Scan direction parameter, D4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, D3 parameter of MADCTL command

5.2.4.2 220 Gate Output Mode (GM1="L", GM0="H")

Source Out		S1	S2	S3	S4	S5	S6	- - -	S523	S524	S525	S526	S527	S528		
RA		RGB=0	RGB=1		RGB=0	RGB=1		RGB Order	RGB=0	RGB=1		RGB=0	RGB=1		SA	
MY=0	*MY=1*														*ML=0*	*ML=1*
0	219	R0$_{5-0}$	G0$_{5-0}$	B0$_{5-0}$	R1$_{5-0}$	G1$_{5-0}$	B1$_{5-0}$	- - -	R174$_{5-0}$	G174$_{5-0}$	B174$_{5-0}$	R175$_{5-0}$	G175$_{5-0}$	B175$_{5-0}$	0	219
1	218							- - -							1	218
2	217							- - -							2	217
3	216							- - -							3	216
4	215							- - -							4	215
5	214							- - -							5	214
6	213							- - -							6	213
7	212							- - -							7	212
8	211							- - -							8	211
9	210							- - -							9	210
10	209							- - -							10	209
11	208							- - -							11	208
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:
212	7							- - -							212	7
213	6							- - -							213	6
214	5							- - -							214	5
215	4							- - -							215	4
216	3							- - -							216	3
217	2							- - -							217	2
218	1							- - -							218	1
219	0							- - -				RN$_{5-0}$	GN$_{5-0}$	BN$_{5-0}$	219	0
CA	*MX=0*	0			1			- - -	174			175				
	MX=1	175			174			- - -	1			0				

NOTE: RA = Row Address,

CA = Column Address,

SA = Scan Address,

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB= Red, Green and Blue pixel position change, D3 parameter of MADCTL command

5.2.4.3 208 Gate Output Mode (GM1="L", GM0="L")

Source Out	S1	S2	S3	S4	S5	S6	- - -	S523	S524	S525	S526	S527	S528
	RGB=0 / RGB=1			RGB=0 / RGB=1			RGB Order	RGB=0 / RGB=1			RGB=0 / RGB=1		

RA MY=0	RA MY=1														SA ML=0	SA ML=1
0	207	R0$_{5-0}$	G0$_{5-0}$	B0$_{5-0}$	R1$_{5-0}$	G1$_{5-0}$	B1$_{5-0}$	- - -	R174$_{5-0}$	G174$_{5-0}$	B174$_{5-0}$	R175$_{5-0}$	G175$_{5-0}$	B175$_{5-0}$	0	207
1	206							- - -							1	206
2	205							- - -							2	205
3	204							- - -							3	204
4	203							- - -							4	203
5	202							- - -							5	202
6	201							- - -							6	201
7	200							- - -							7	200
8	199							- - -							8	199
9	198							- - -							9	198
10	197							- - -							10	197
11	196							- - -							11	196
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
200	7							- - -							200	7
201	6							- - -							201	6
202	5							- - -							202	5
203	4							- - -							203	4
204	3							- - -							204	3
205	2							- - -							205	2
206	1							- - -							206	1
207	0							- - -				RN$_{5-0}$	GN$_{5-0}$	BN$_{5-0}$	207	0
CA	MX=0	0			1			- - -	174			175				
	MX=1	175			174			- - -	1			0				

NOTE: RA = Row Address,

CA = Column Address,

SA = Scan Address,

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

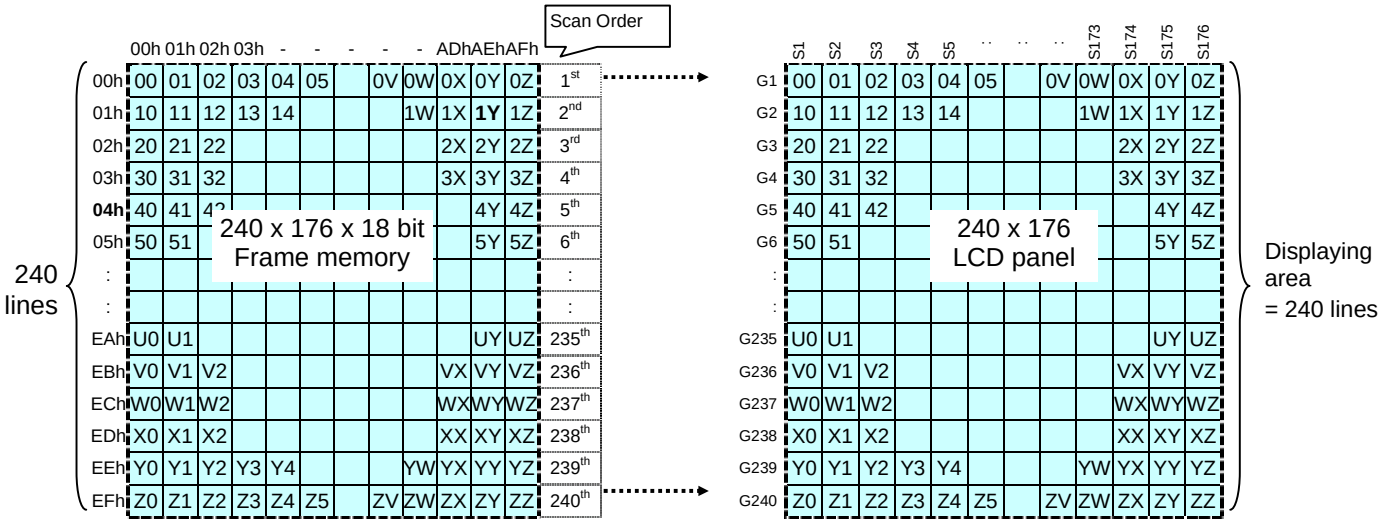
ML = Scan direction parameter, D4 parameter of MADCTL command

RGB= Red, Green and Blue pixel position change, D3 parameter of MADCTL command

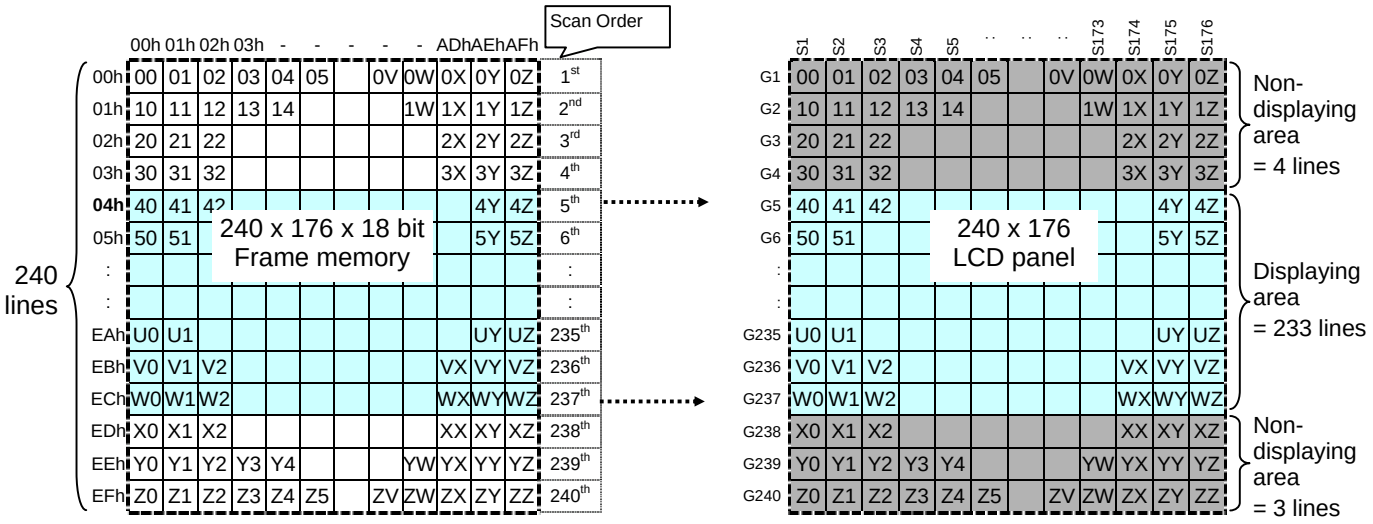
5.2.5 Normal Display On or Partial Mode On, Vertical Scroll Off

In this mode, contents of the frame memory within an area where column address is 00h to AF h and row address is 00h to EF h is displayed.
To display a dot on leftmost top corner, store the dot data at (column address, row address) = (1,1).

Example1) Normal Display On (GM1="H", GM0="L": 240-Gate mode)



Example2) Partial Display On: PSL [7:0] = EDh, PEL [7:0] = 03h, MADCTR (ML)=0
(GM1="H", GM0="L": 240-Gate mode)



5.2.6 Vertical Scroll

There is a vertical scrolling mode, which is determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

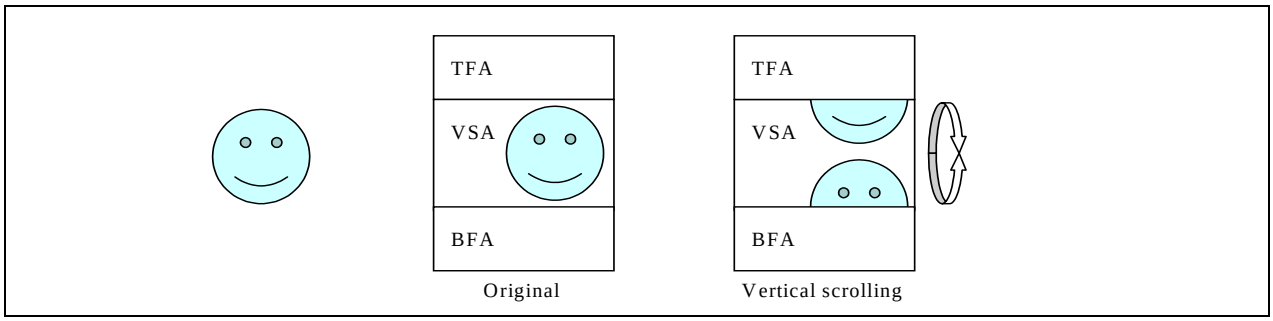
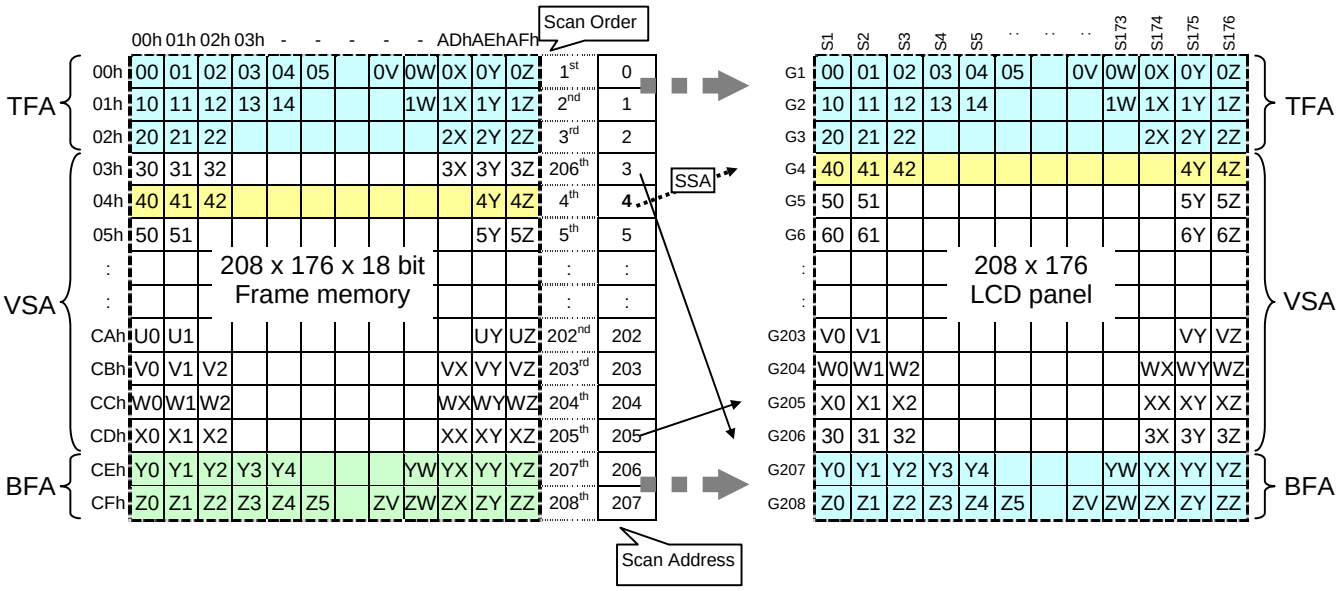
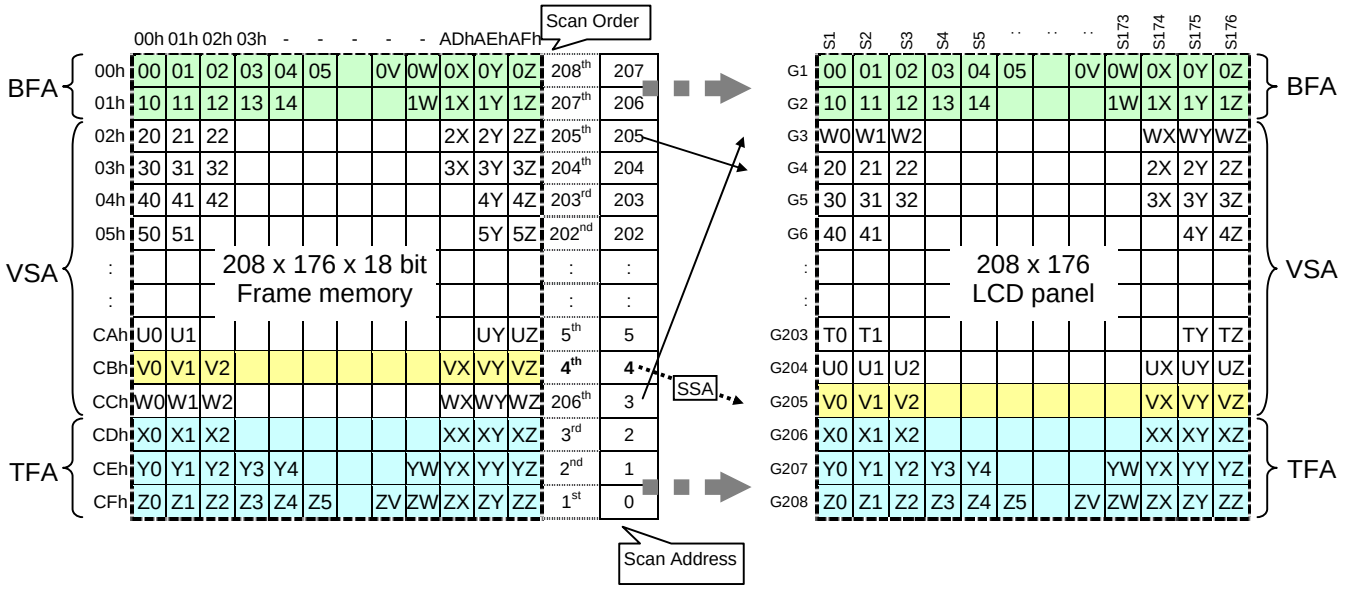


Fig. 5.2.5 Vertical Scrolling

Example1) Panel size=208 x 176 (GM [1:0]=00), TFA =2, VSA=204, BFA=2, SSA=4, MADCTR (ML)=0
(GM1="L", GM0="L": 208-Gate mode)



Example2) Panel size=208 x 176 (GM [1:0]=00), TFA =2, VSA=204, BFA=2, SSA=4,
MADCTR (ML)=1 (TFA and BFA are exchanged)
(GM1="L", GM0="L": 208-Gate mode)



Note: 1. When Vertical Scroll Definition Parameters (TFA+VSA+BFA) ≠ 208 (when GM[1:0]= 00), (TFA+VSA+BFA) ≠ 220 (when GM[1:0]= 01) or (TFA+VSA+BFA) ≠ 240 (when GM[1:0]= 10), Scrolling Mode is undefined.

2. In this example it was assumed that prior to sending the Vertical Scrolling Start Address, "New Data" had been written to the Frame Memory in the area described and the Vertical Scrolling Start Address was (Current Position-1Lines).

5.2.6.2 Vertical Scroll Example

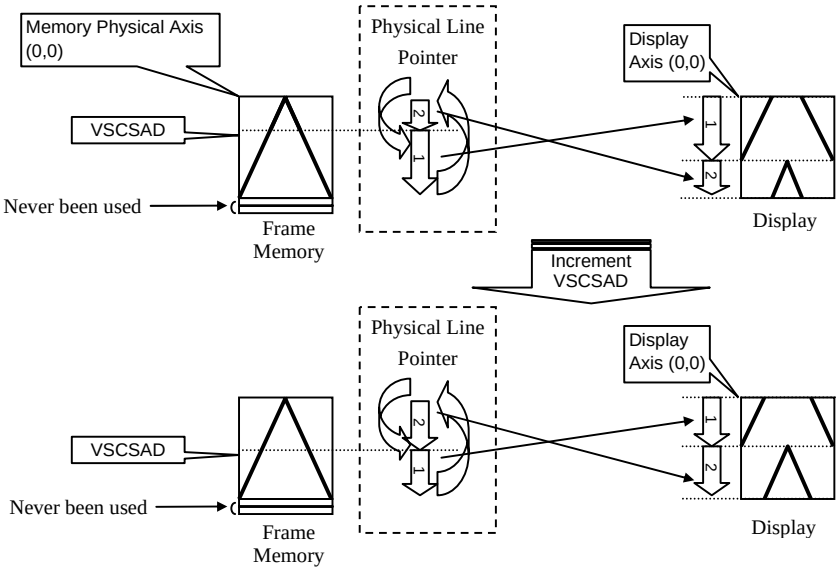
There are 2 types of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA ≠ 208 (when GM1="L", GM0="L": 208-Gate mode),

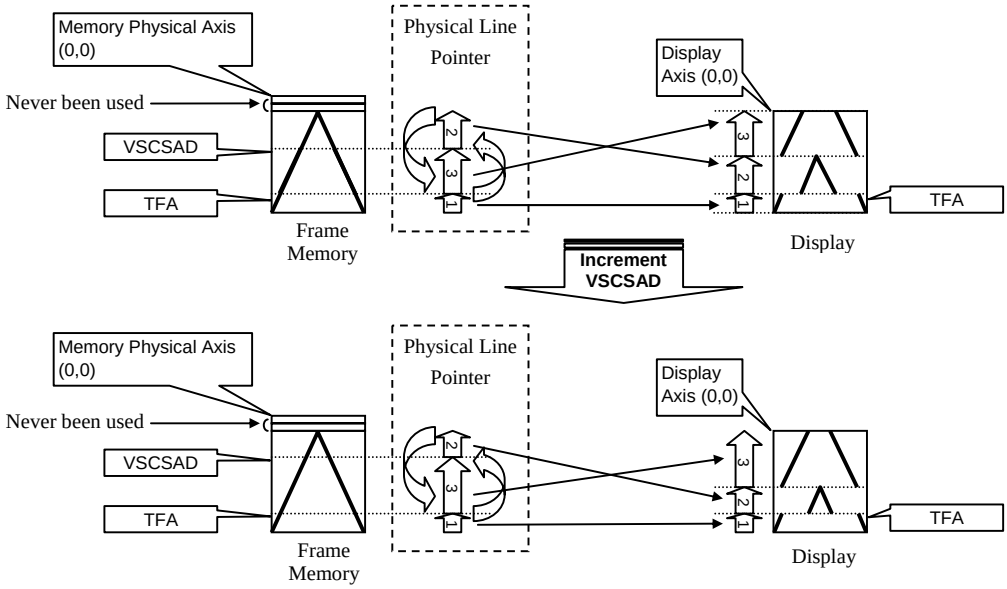
N/A. Do not set TFA + VSA + BFA ≠ 208 (when GM[1:0]= 00). In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA = 208 (when GM1="L", GM0="L": 208-Gate mode)

Example1) When MADCTR parameter ML="0", TFA=0, VSA=208, BFA=0 and VSCSAD=40.



Example2) When MADCTR parameter ML="1", TFA=30, VSA=178, BFA=0 and VSCSAD=80.

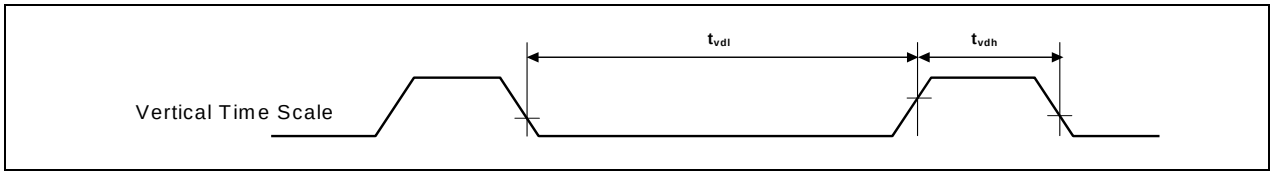


5.2.7 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

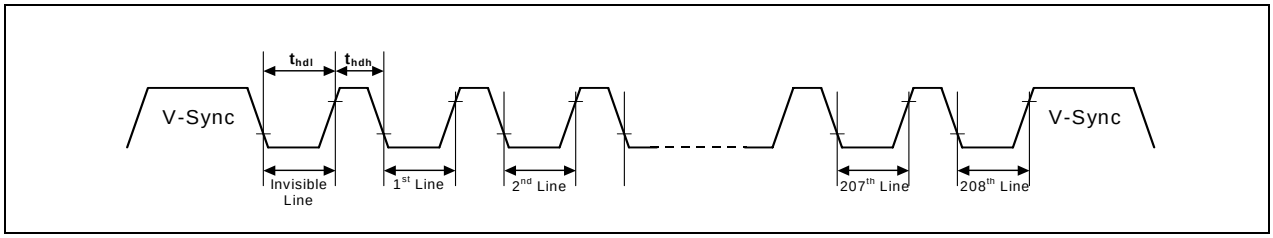
5.2.7.1 Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

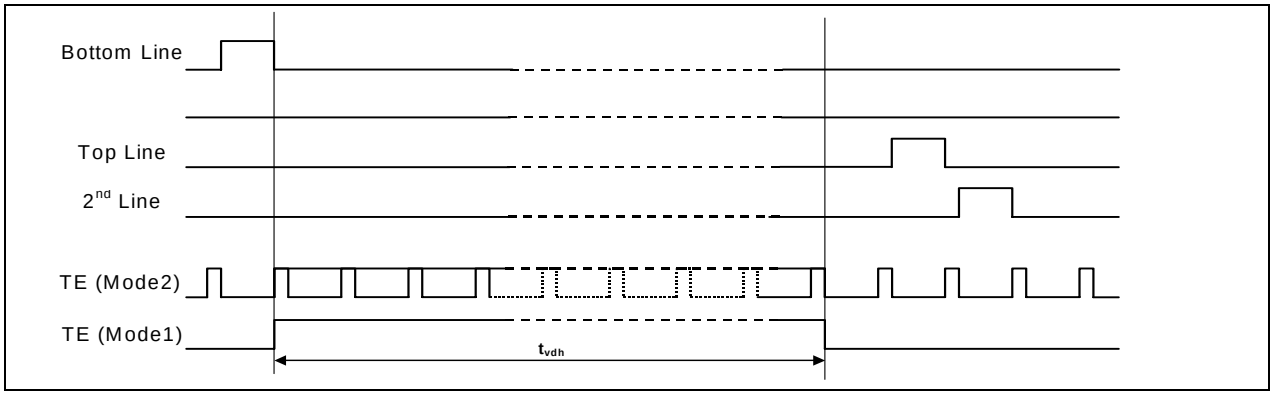


t_{vdh}= The LCD display is not updated from the Frame Memory
t_{vdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 208 H-sync pulses per field.



t_{hdh}= The LCD display is not updated from the Frame Memory
t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low

5.2.7.2 Tearing Effect Line Timing

The Tearing Effect signal is described below:

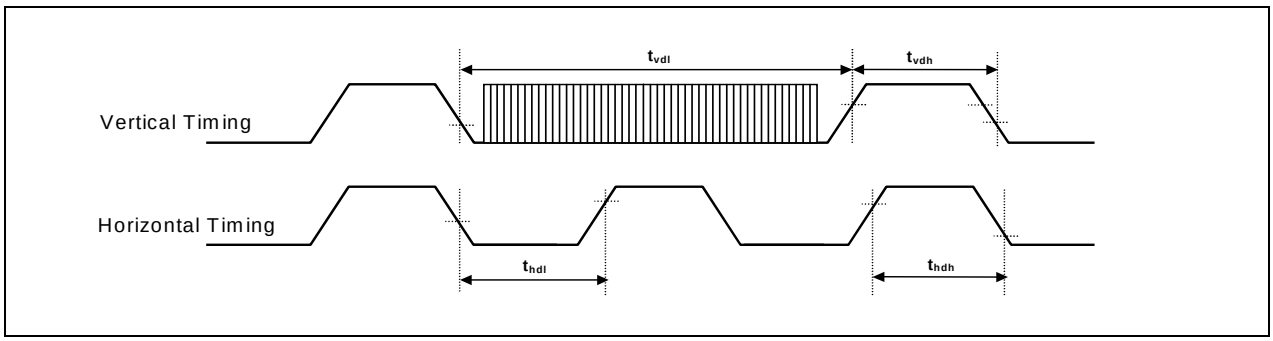


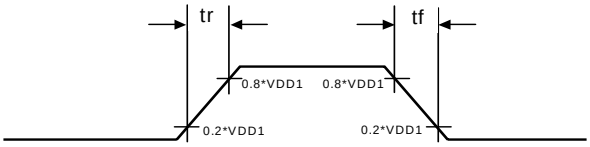
Table 5.2.12 AC characteristics of Tearing Effect Signal

Idle Mode Off (Frame Rate = 58Hz)

Symbol	Parameter	min	max	unit	description
t_{vdl}	Vertical Timing Low Duration	13	-	ms	
t_{vdh}	Vertical Timing High Duration	1000	-	μs	
t_{hdl}	Horizontal Timing Low Duration	33	-	μs	
t_{hdh}	Horizontal Timing High Duration	25	500	μs	

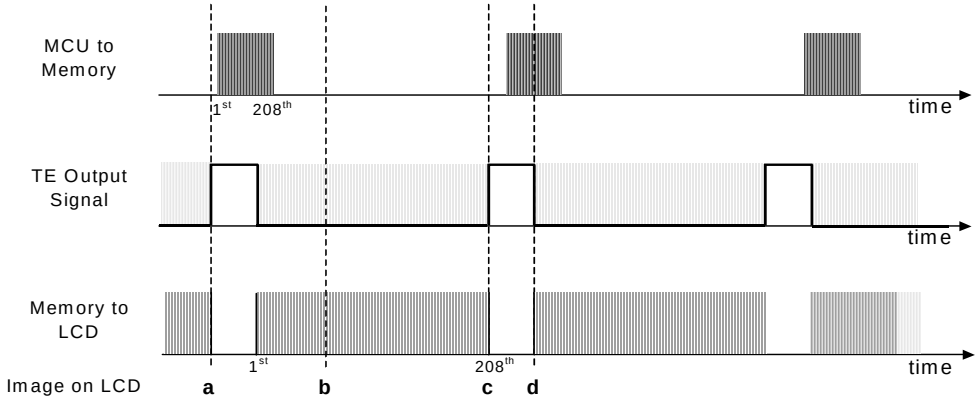
NOTE: The timings in Table 5.2.12 apply when MADCTL ML=0 and ML=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

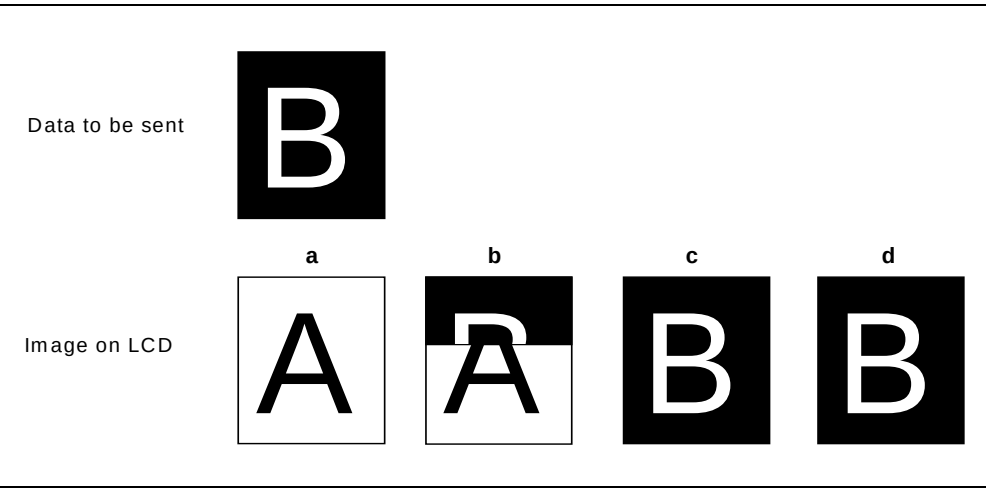


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

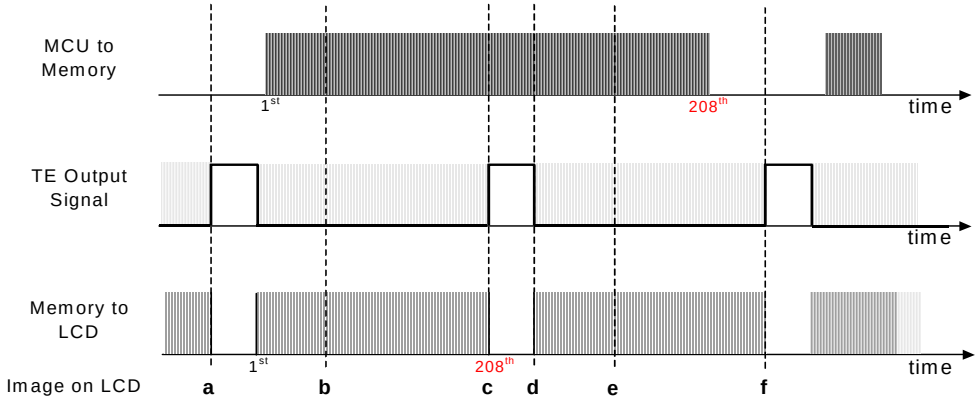
5.2.7.3 Example 1: MPU Write is Faster than Panel Read.



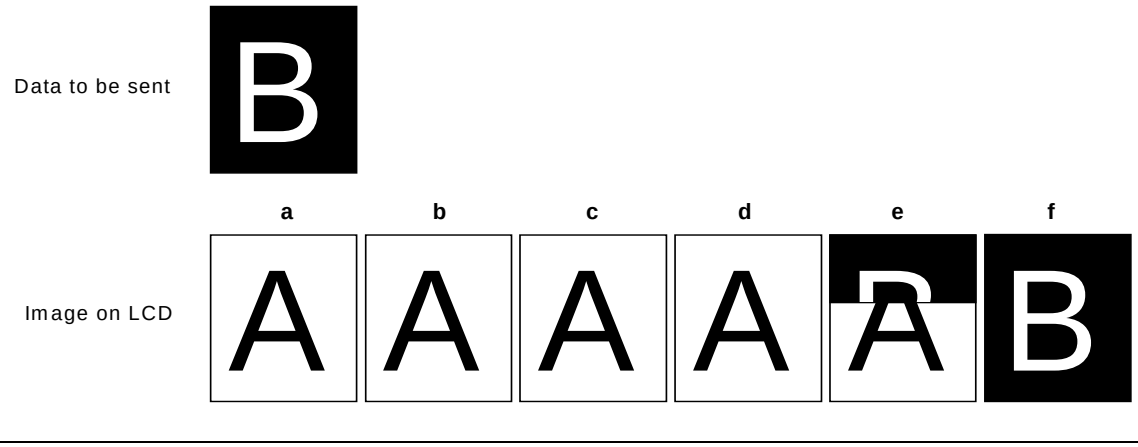
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



5.2.7.4 Example 2: MPU Write is Slower than Panel Read.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.



5.2.8 Colour Depth Conversion Look Up Tables

Color	Look Up Table Outputs Frame Memory Data (5 or 6-bit)	Default value after hardware reset		RGBSET parameter	Look Up Table Input Data	
		256 Color	4096 Color		256 Color	4096 Color
RED	R_{004} R_{003} R_{002} R_{001} R_{000}	00000	00000	1	000	0000
	R_{014} R_{013} R_{012} R_{011} R_{010}	00011	00011	2	001	0001
	R_{024} R_{023} R_{022} R_{021} R_{020}	00101	00101	3	010	0010
	R_{034} R_{033} R_{032} R_{031} R_{030}	00111	00111	4	011	0011
	R_{044} R_{043} R_{042} R_{041} R_{040}	01001	01001	5	100	0100
	R_{054} R_{053} R_{052} R_{051} R_{050}	01011	01011	6	101	0101
	R_{064} R_{063} R_{062} R_{061} R_{060}	01101	01101	7	110	0110
	R_{074} R_{073} R_{072} R_{071} R_{070}	01111	01111	8	111	0111
	R_{084} R_{083} R_{082} R_{081} R_{080}	Not Used	10001	9	Not Used	1000
	R_{094} R_{093} R_{092} R_{091} R_{090}		10011	10		1001
	R_{104} R_{103} R_{102} R_{101} R_{100}		10101	11		1010
	R_{114} R_{113} R_{112} R_{111} R_{110}		10111	12		1011
	R_{124} R_{123} R_{122} R_{121} R_{120}		11001	13		1100
	R_{134} R_{133} R_{132} R_{131} R_{130}		11011	14		1101
	R_{144} R_{143} R_{142} R_{141} R_{140}		11101	15		1110
	R_{154} R_{153} R_{152} R_{151} R_{150}		11111	16		1111
GREEN	G_{005} G_{004} G_{003} G_{002} G_{001} G_{000}	000000	000000	17	000	0000
	G_{015} G_{014} G_{013} G_{012} G_{011} G_{010}	000111	000111	18	001	0001
	G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}	001011	001011	19	010	0010
	G_{035} G_{034} G_{033} G_{032} G_{031} G_{030}	001111	001111	20	011	0011
	G_{045} G_{044} G_{043} G_{042} G_{041} G_{040}	010011	010011	21	100	0100
	G_{055} G_{054} G_{053} G_{052} G_{051} G_{050}	010111	010111	22	101	0101
	G_{065} G_{064} G_{063} G_{062} G_{061} G_{060}	011011	011011	23	110	0110
	G_{075} G_{074} G_{073} G_{072} G_{071} G_{070}	011111	011111	24	111	0111
	G_{085} G_{084} G_{083} G_{082} G_{081} G_{080}	Not Used	100011	25	Not Used	1000
	G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}		100111	26		1001
	G_{105} G_{104} G_{103} G_{102} G_{101} G_{100}		101011	27		1010
	G_{115} G_{114} G_{113} G_{112} G_{111} G_{110}		101111	28		1011
	G_{125} G_{124} G_{123} G_{122} G_{121} G_{120}		110011	29		1100
	G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}		110111	30		1101
	G_{145} G_{144} G_{143} G_{142} G_{141} G_{140}		111011	31		1110
	G_{155} G_{154} G_{153} G_{152} G_{151} G_{150}		111111	32		1111
BLUE	B_{004} B_{003} B_{002} B_{001} B_{000}	00000	00000	33	00	0000
	B_{014} B_{013} B_{012} B_{011} B_{010}	00011	00011	34	01	0001
	B_{024} B_{023} B_{022} B_{021} B_{020}	00101	00101	35	10	0010
	B_{034} B_{033} B_{032} B_{031} B_{030}	00111	00111	36	11	0011
	B_{044} B_{043} B_{042} B_{041} B_{040}	Not Used	01001	37	Not Used	0100
	B_{054} B_{053} B_{052} B_{051} B_{050}		01011	38		0101
	B_{064} B_{063} B_{062} B_{061} B_{060}		01101	39		0110
	B_{074} B_{073} B_{072} B_{071} B_{070}		01111	40		0111
	B_{084} B_{083} B_{082} B_{081} B_{080}		10001	41		1000
	B_{094} B_{093} B_{092} B_{091} B_{090}		10011	42		1001
	B_{104} B_{103} B_{102} B_{101} B_{100}		10101	43		1010
	B_{114} B_{113} B_{112} B_{111} B_{110}		10111	44		1011
	B_{124} B_{123} B_{122} B_{121} B_{120}		11001	45		1100
	B_{134} B_{133} B_{132} B_{131} B_{130}		11011	46		1101
	B_{144} B_{143} B_{142} B_{141} B_{140}		11101	47		1110
	B_{154} B_{153} B_{152} B_{151} B_{150}		11111	48		1111

5.3 INSTRUCTION DECODER & REGISTER

The instruction decoder identifies command words arriving at the interface and routes the following data type bytes to their destination. The command set can be found in “6 INSTRUCTION DESCRIPTION” section.

5.4 SYSTEM CLOCK GENERATOR

The timing generator produces the various signals to drive the internal circuitry. Internal chip operation is not affected by operations on the data bus.

5.5 OSCILLATOR

LDS274 has on-chip oscillator which does not require external components. This oscillator output signal is used for system clock generation for internal display operation

5.6 SOURCE DRIVER

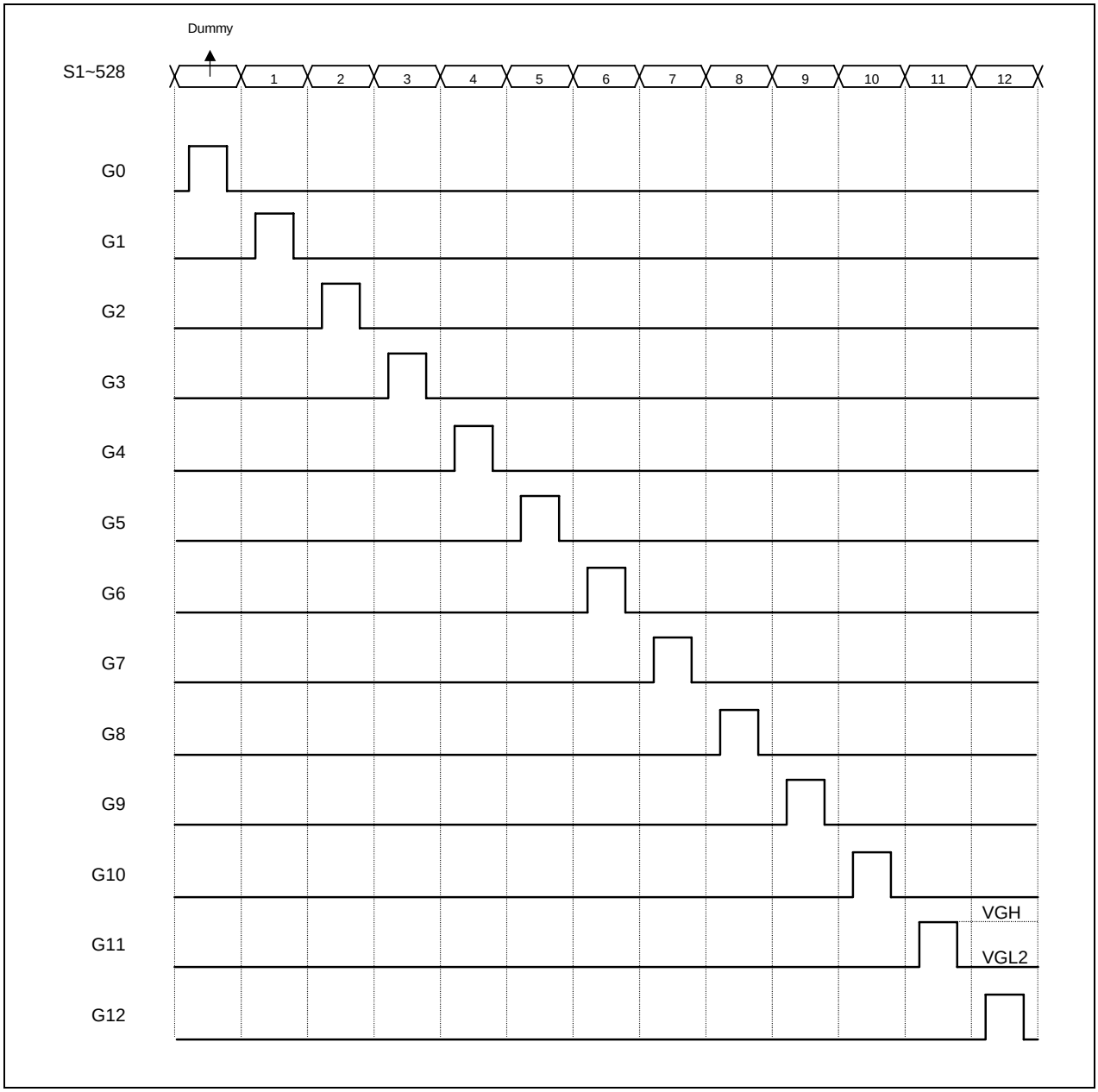
The source driver block includes 176x3 source outputs (S1 to S528), which should be connected directly to the TFT-LCD. The source output signals are generated in the data processing block after the data is read out of the RAM and latched, which represent the simultaneous selected rows. When less then 528 sources are required the unused source outputs should be left open-circuit.

5.7 GATE DRIVER

The gate driver block includes 240 gate outputs + 1 dummy gate output (G0 to G240) which should be connected directly to the TFT-LCD. According to the GM1 and GM0 bit, total gate output number can be selectable from 240, 220 and 208.

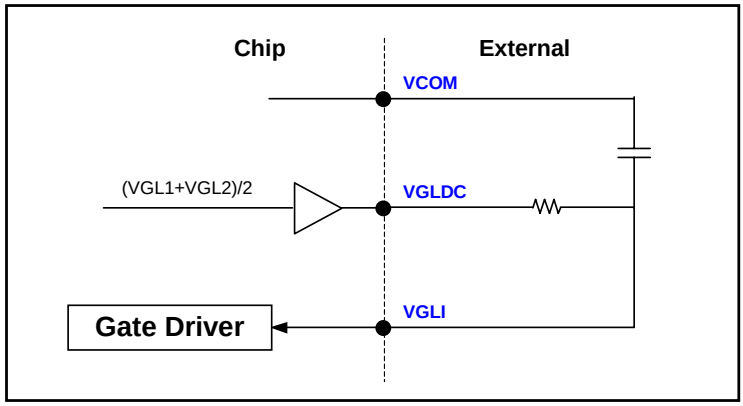
There are all 3-linds of gate driver option which can be controlled by command (GOPSEL)

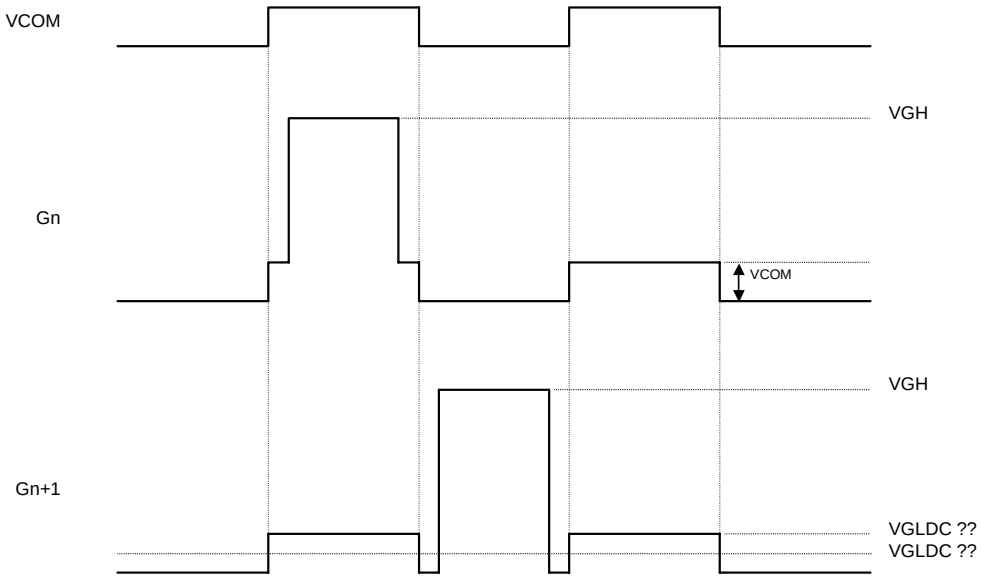
5.7.1 Gate Drive Option1 (2-Level Gate Drive)



5.7.2 Gate Drive Option2 (3-Level Gate Drive)

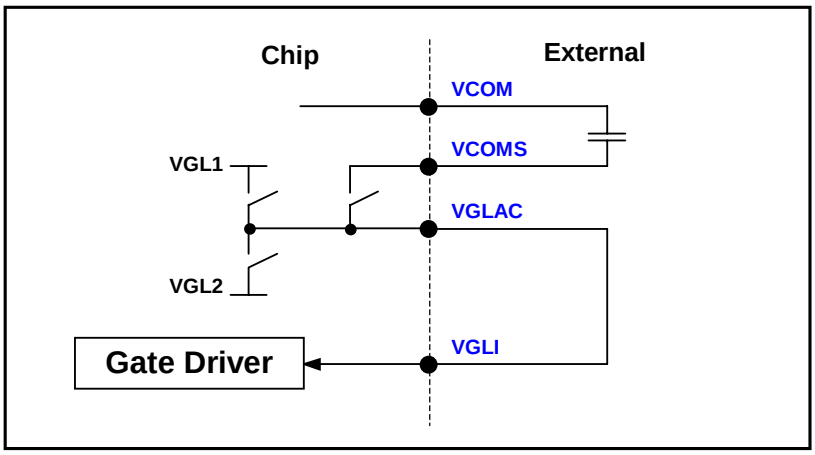
Example of external application for gate drive option 2

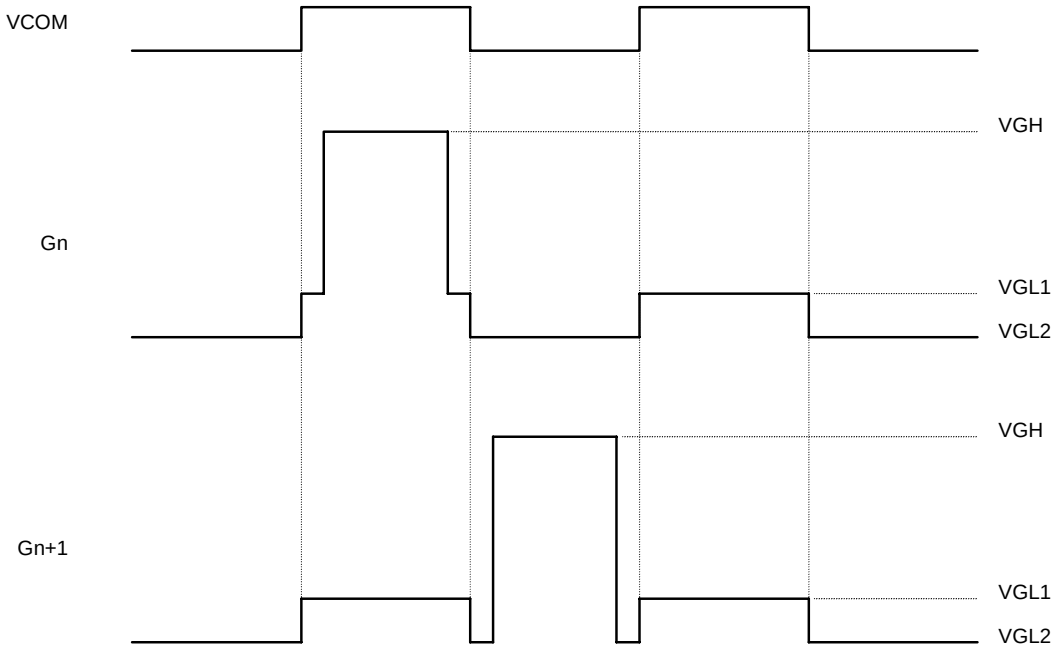




5.7.3 Gate Drive Option3 (3-Level Gate Drive)

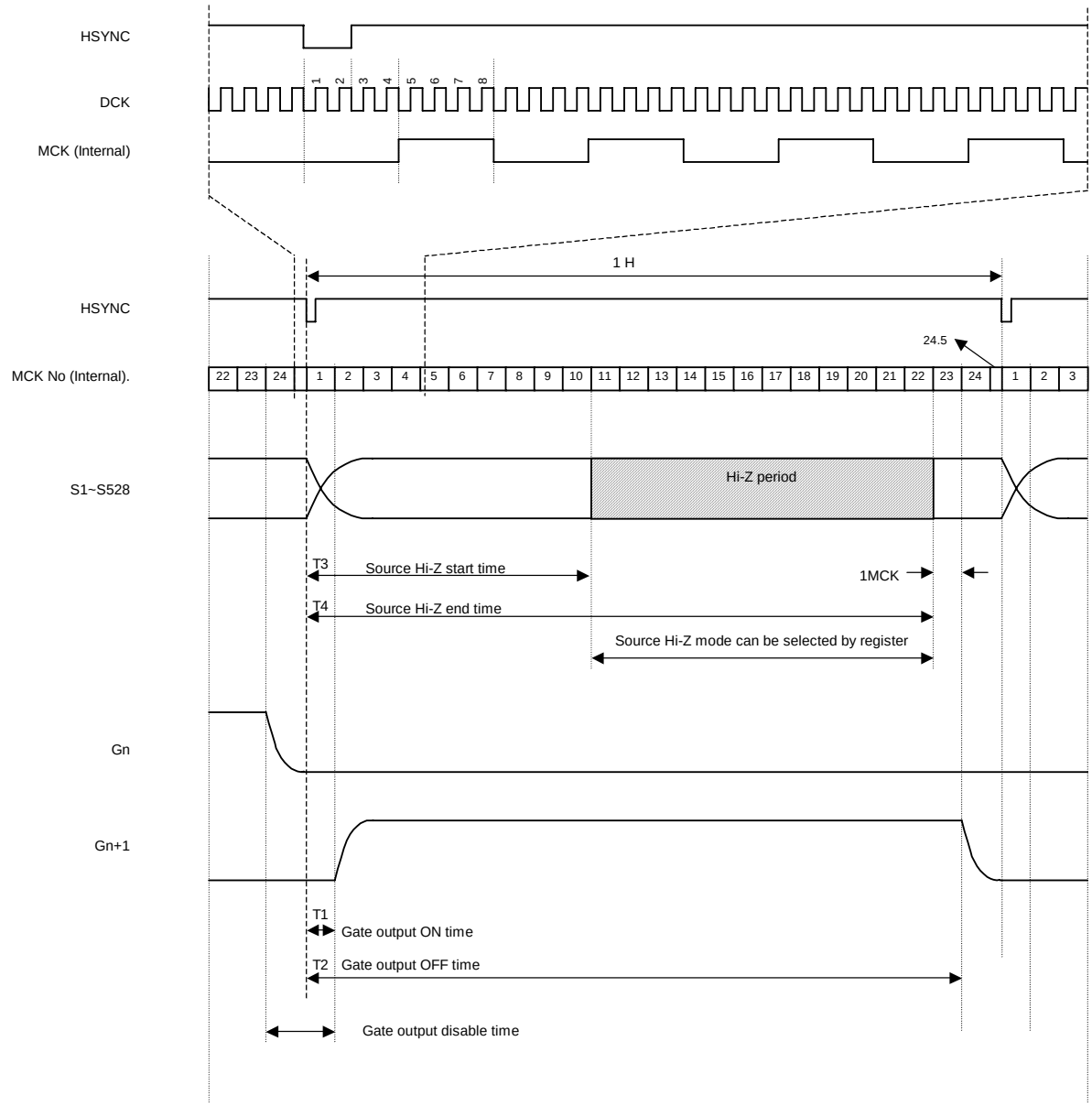
Example of external application for gate drive option 3





5.8 RGB INTERFACE TIMING DIAGRAM

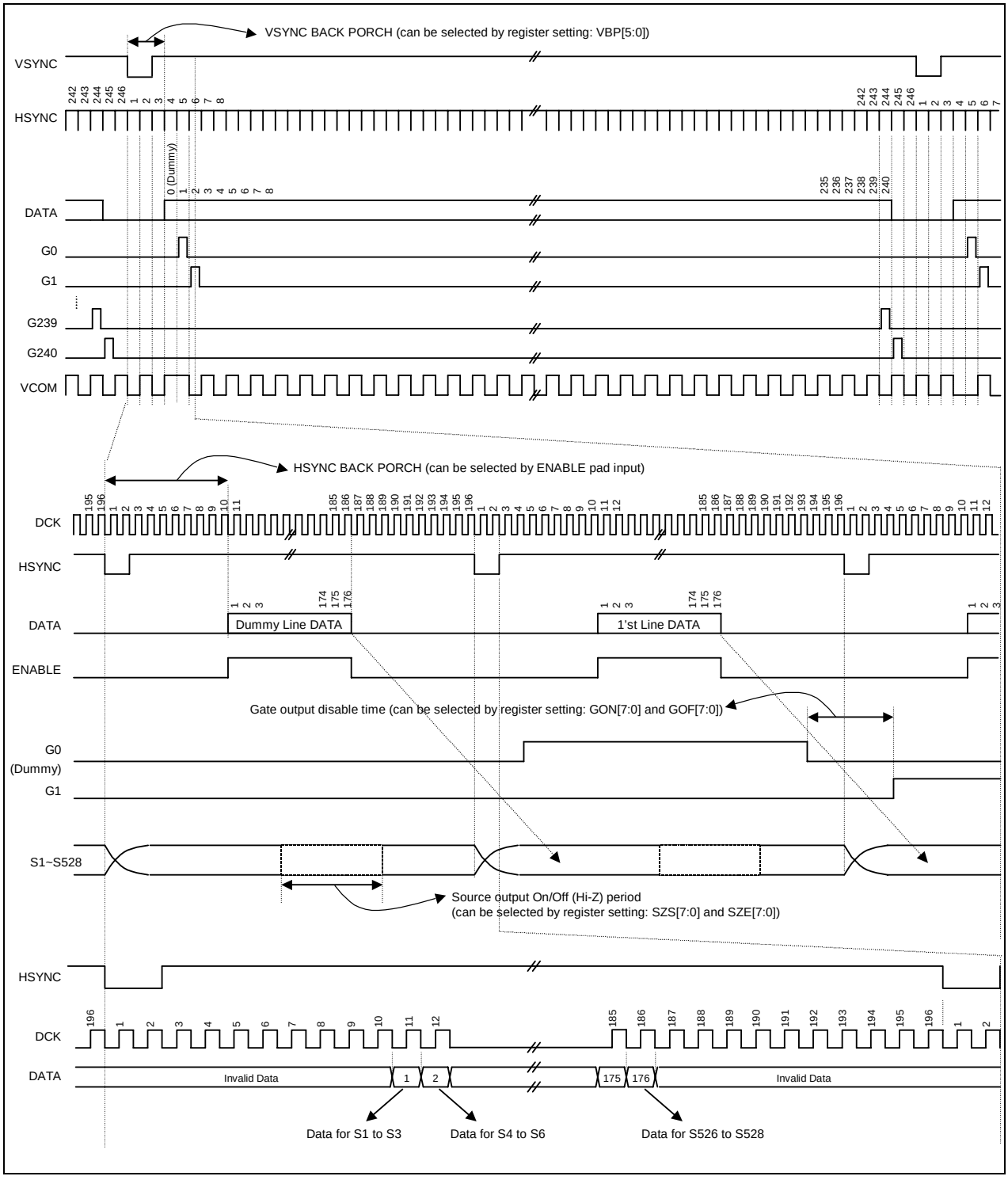
5.8.1 Relationship between Input Signal and Output Signal (RGB I/F Mode 3)



Note. T1, T2, T3 and T4 can be selected by register setting

5.8.2 Input / Output Timing Chart (G0->G240, S1->S528)

Horizontal valid data start time=10DCK, Vertical valid data start time=3HSYNC, 1 Line scan, Line inversion)



5.9 LCD POWER GENERATION CIRCUIT

5.9.1 LCD Power Generation Scheme

The boost voltage generated in LDS274 is shown as below. (In case of AVDD=2 times boosting and VR/VS/VG=4V)

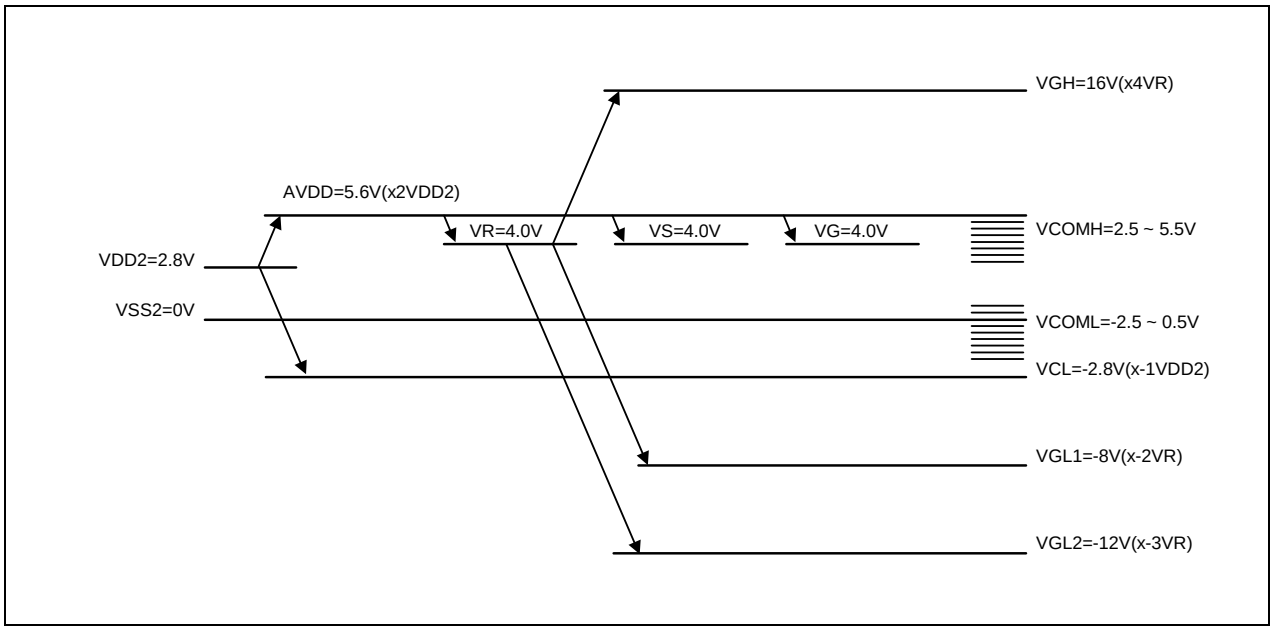


Fig. 5.9.1 LCD power generation scheme

5.9.2 VS/VG AMP Circuit

Booster1 circuit triples the voltage of VDD2-VSS and the boosted voltage is output at VOUT pin.

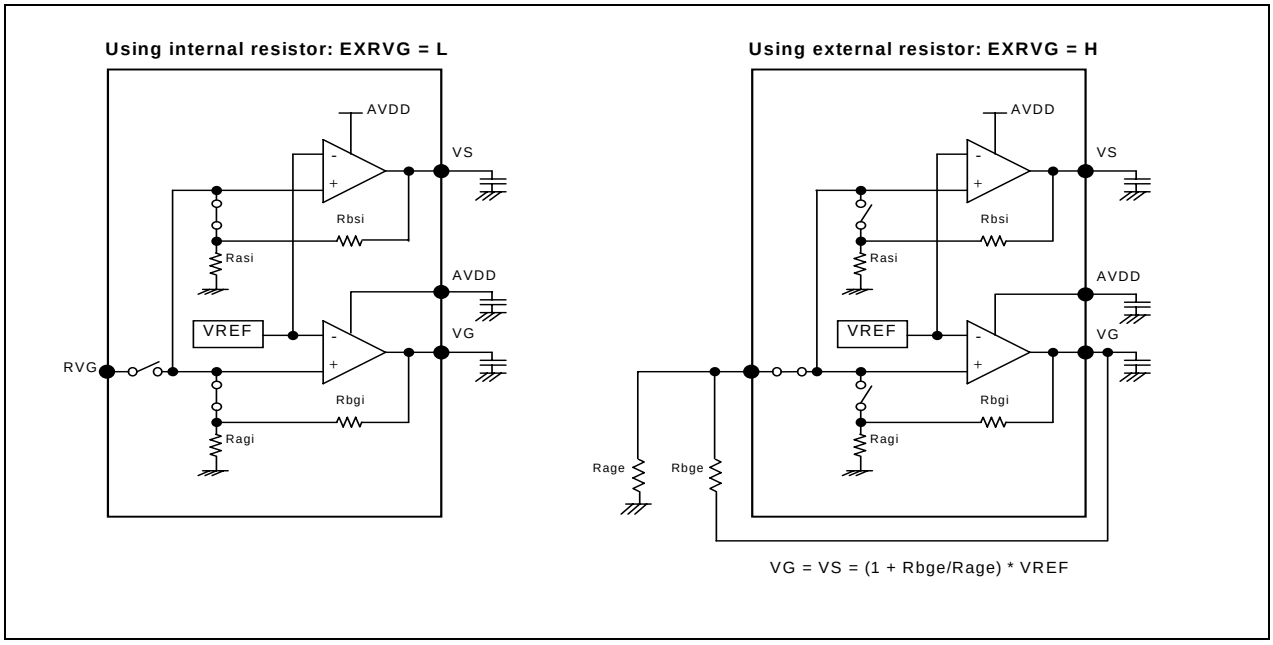


Fig. 5.9.2 LCD power generation scheme

5.9.3 Various Boosting Steps

The boost steps of each boosting voltage are selected according to how the external capacitors are connected. Different booster applications are shown as below.

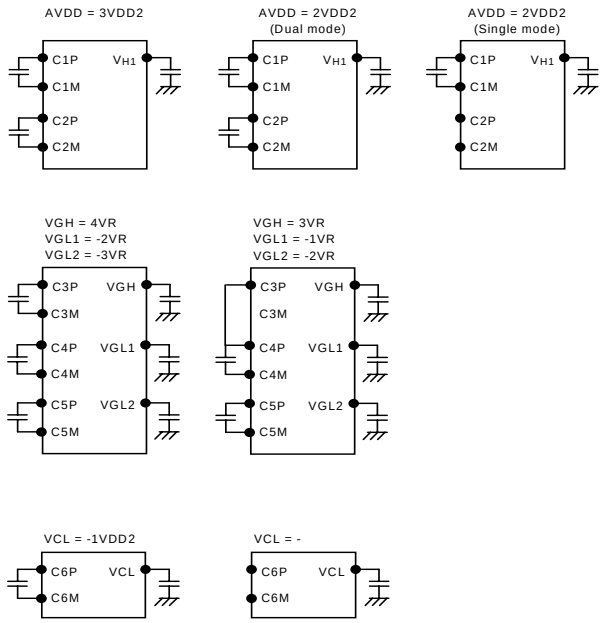
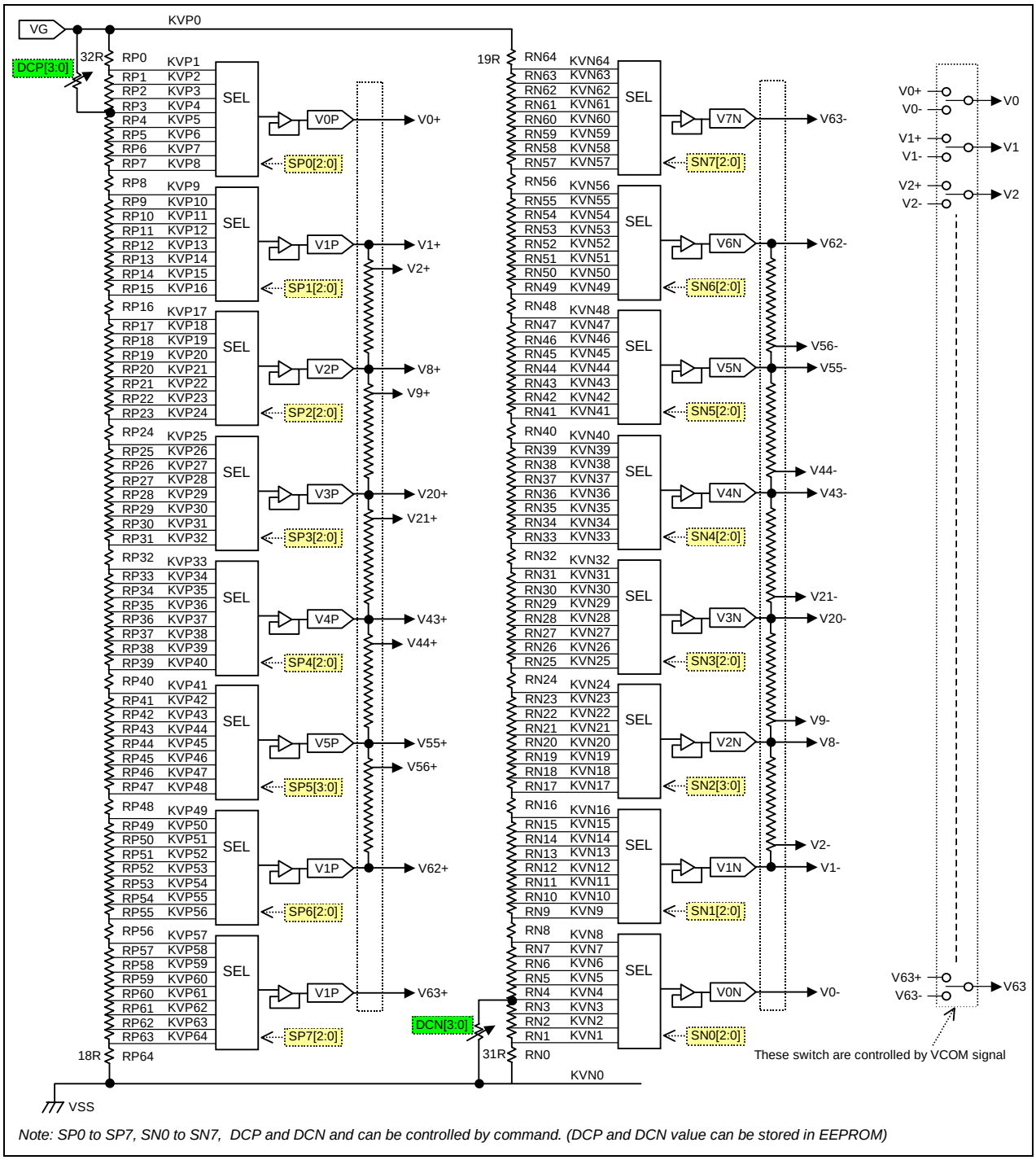


Fig. 5.9.3 Various boosting steps

5.9.4 Gray Voltage Generator for Source Driver

5.9.4.1 Gamma Correction Curve Circuit



Note: SP0 to SP7, SN0 to SN7, DCP and DCN and can be controlled by command. (DCP and DCN value can be stored in EEPROM)

5.9.4.2 Relationship between RAM Data and Output Voltages

Data (Hex)	Output Voltage When VG=4.2V									
	VCOM = Low					VCOM = High				
	Gamma	1.0	2.5	2.2	1.8	Gamma	1.0	2.5	2.2	1.8
3F	V0+	3.896	3.896	3.896	3.896	V0-	0.204	0.204	0.204	0.204
3E	V1+	3.365	3.754	3.795	3.834	V1-	0.735	0.346	0.305	0.266
3D	V2+	3.206	3.657	3.761	3.789	V2-	0.894	0.443	0.339	0.311
3C	V3+	3.103	3.579	3.682	3.761	V3-	0.997	0.521	0.418	0.339
3B	V4+	3.014	3.500	3.647	3.689	V4-	1.086	0.600	0.453	0.411
3A	V5+	2.945	3.438	3.589	3.664	V5-	1.155	0.662	0.511	0.436
39	V6+	2.888	3.381	3.540	3.626	V6-	1.212	0.719	0.560	0.474
38	V7+	2.833	3.330	3.482	3.581	V7-	1.267	0.770	0.618	0.519
37	V8+	2.786	3.276	3.435	3.537	V8-	1.314	0.824	0.665	0.563
36	V9+	2.743	3.220	3.389	3.486	V9-	1.357	0.880	0.711	0.614
35	V10+	2.703	3.175	3.347	3.444	V10-	1.397	0.925	0.753	0.656
34	V11+	2.664	3.131	3.306	3.402	V11-	1.436	0.969	0.794	0.698
33	V12+	2.629	3.087	3.258	3.365	V12-	1.471	1.013	0.842	0.735
32	V13+	2.596	3.043	3.212	3.328	V13-	1.504	1.057	0.888	0.772
31	V14+	2.563	2.998	3.174	3.287	V14-	1.537	1.102	0.926	0.813
30	V15+	2.534	2.959	3.135	3.242	V15-	1.566	1.141	0.965	0.858
2F	V16+	2.506	2.926	3.095	3.200	V16-	1.594	1.174	1.005	0.900
2E	V17+	2.474	2.891	3.056	3.165	V17-	1.626	1.209	1.044	0.935
2D	V18+	2.447	2.852	3.014	3.128	V18-	1.653	1.248	1.086	0.972
2C	V19+	2.424	2.819	2.977	3.090	V19-	1.676	1.281	1.123	1.010
2B	V20+	2.400	2.786	2.942	3.052	V20-	1.700	1.314	1.158	1.048
2A	V21+	2.375	2.754	2.911	3.011	V21-	1.725	1.346	1.189	1.089
29	V22+	2.351	2.724	2.875	2.974	V22-	1.749	1.376	1.225	1.126
28	V23+	2.329	2.693	2.839	2.941	V23-	1.771	1.407	1.261	1.159
27	V24+	2.306	2.660	2.806	2.909	V24-	1.794	1.440	1.294	1.191
26	V25+	2.283	2.631	2.775	2.873	V25-	1.817	1.469	1.325	1.227
25	V26+	2.260	2.602	2.744	2.838	V26-	1.840	1.498	1.356	1.262
24	V27+	2.240	2.572	2.713	2.804	V27-	1.860	1.528	1.387	1.296
23	V28+	2.219	2.544	2.680	2.773	V28-	1.881	1.556	1.420	1.327
22	V29+	2.199	2.517	2.648	2.741	V29-	1.901	1.583	1.452	1.359
21	V30+	2.179	2.488	2.618	2.709	V30-	1.921	1.612	1.482	1.391
20	V31+	2.160	2.457	2.588	2.676	V31-	1.940	1.643	1.512	1.424
1F	V32+	2.138	2.433	2.556	2.643	V32-	1.962	1.667	1.544	1.457
1E	V33+	2.116	2.408	2.529	2.612	V33-	1.984	1.692	1.571	1.488
1D	V34+	2.098	2.381	2.499	2.580	V34-	2.002	1.719	1.601	1.520
1C	V35+	2.079	2.354	2.465	2.548	V35-	2.021	1.746	1.635	1.552
1B	V36+	2.061	2.328	2.438	2.519	V36-	2.039	1.772	1.662	1.581
1A	V37+	2.040	2.302	2.411	2.485	V37-	2.060	1.798	1.689	1.615
19	V38+	2.018	2.275	2.382	2.452	V38-	2.082	1.825	1.718	1.648
18	V39+	1.998	2.248	2.352	2.424	V39-	2.102	1.852	1.748	1.676
17	V40+	1.979	2.223	2.324	2.394	V40-	2.121	1.877	1.776	1.706
16	V41+	1.960	2.197	2.295	2.362	V41-	2.140	1.903	1.805	1.738
15	V42+	1.937	2.172	2.264	2.332	V42-	2.163	1.928	1.836	1.768
14	V43+	1.914	2.145	2.236	2.300	V43-	2.186	1.955	1.864	1.800
13	V44+	1.892	2.116	2.207	2.267	V44-	2.208	1.984	1.893	1.833
12	V45+	1.870	2.091	2.178	2.236	V45-	2.230	2.009	1.922	1.864
11	V46+	1.849	2.066	2.148	2.205	V46-	2.251	2.034	1.952	1.895
10	V47+	1.828	2.036	2.115	2.174	V47-	2.272	2.064	1.985	1.926
0F	V48+	1.806	2.005	2.086	2.140	V48-	2.294	2.095	2.014	1.960
0E	V49+	1.778	1.978	2.056	2.105	V49-	2.322	2.122	2.044	1.995
0D	V50+	1.752	1.947	2.020	2.073	V50-	2.348	2.153	2.080	2.027
0C	V51+	1.728	1.913	1.987	2.036	V51-	2.372	2.187	2.113	2.064
0B	V52+	1.702	1.879	1.953	1.998	V52-	2.398	2.221	2.147	2.102
0A	V53+	1.672	1.846	1.913	1.962	V53-	2.428	2.254	2.187	2.138
09	V54+	1.634	1.813	1.872	1.918	V54-	2.466	2.287	2.228	2.182
08	V55+	1.600	1.768	1.834	1.873	V55-	2.500	2.332	2.266	2.227
07	V56+	1.571	1.729	1.788	1.830	V56-	2.529	2.371	2.312	2.270
06	V57+	1.529	1.684	1.739	1.776	V57-	2.571	2.416	2.361	2.324
05	V58+	1.466	1.622	1.686	1.722	V58-	2.634	2.478	2.414	2.378
04	V59+	1.399	1.572	1.613	1.656	V59-	2.701	2.528	2.487	2.444
03	V60+	1.334	1.487	1.548	1.578	V60-	2.766	2.613	2.552	2.522
02	V61+	1.198	1.370	1.419	1.458	V61-	2.902	2.730	2.681	2.642
01	V62+	0.867	1.172	1.220	1.269	V62-	3.233	2.928	2.880	2.831
00	V63+	0.200	0.200	0.200	0.200	V63-	3.900	3.900	3.900	3.900

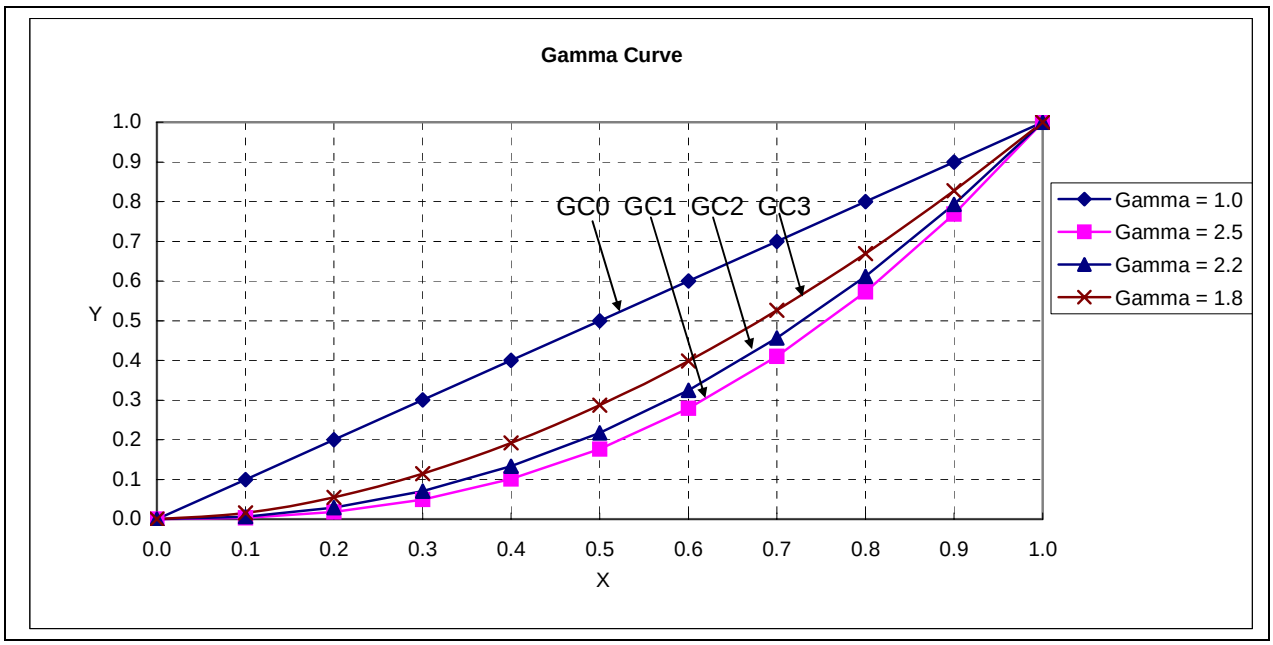


Fig. 5.9.4 Gamma Curve according to the GC0 to GC3 bit

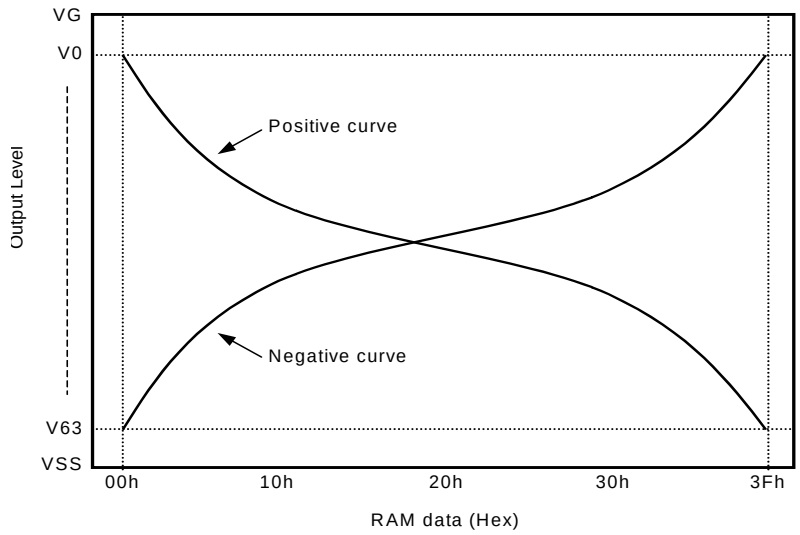


Fig. 5.9.5 Relationship between RAM data and output level

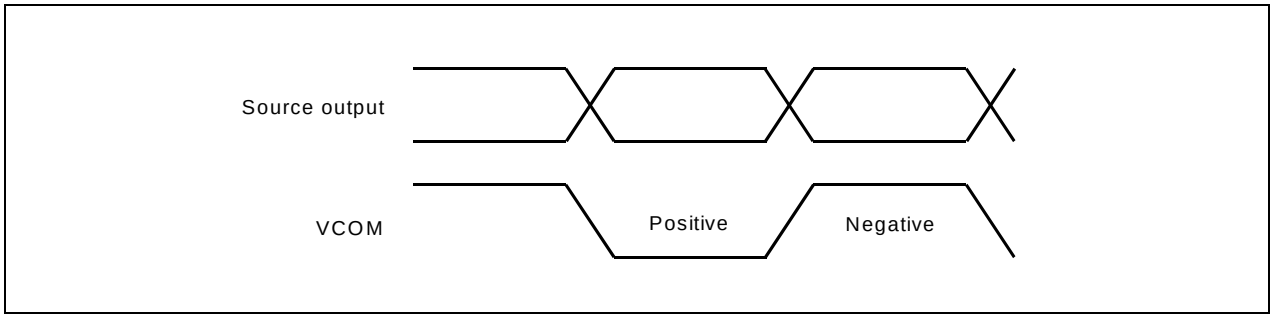


Fig. 5.9.6 Relationship between source output and VCOM

5.10 POWER ON/OFF SEQUENCE

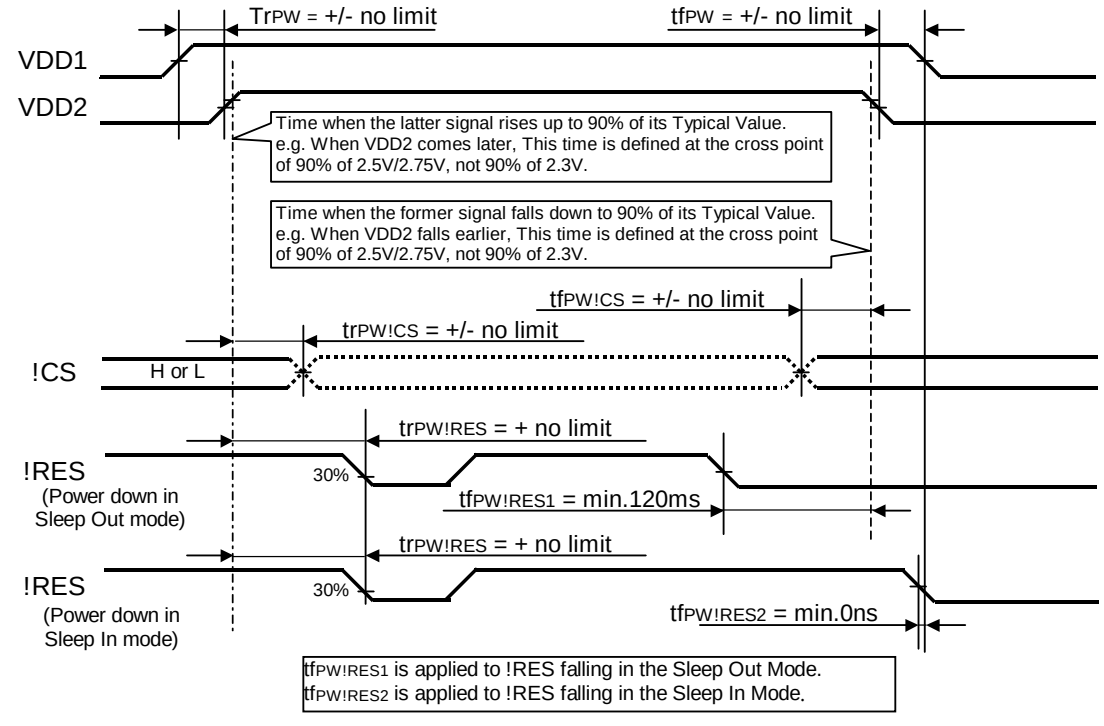
VDD1 and VDD2 can be applied in any order.
VDD2 and VDD1 can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, VDD2 and VDD1 must be powered down minimum 120msec after !RES has been released.
During power off, if LCD is in the Sleep In mode, VDD1 or VDD2 can be powered down minimum 0msec after !RES has been released.
!SCE can be applied at any timing or can be permanently grounded. !RES has priority over !SCE.

There will be no damage to the display module if the power sequences are not met.
There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
If !RES line is not held stable by host during Power On Sequence as defined in Sections 5.10.1 and 5.10.2, then it will be necessary to apply a Hardware Reset (!RES) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

5.10.1 Case 1 – !RES line is held High or Unstable by Host at Power On

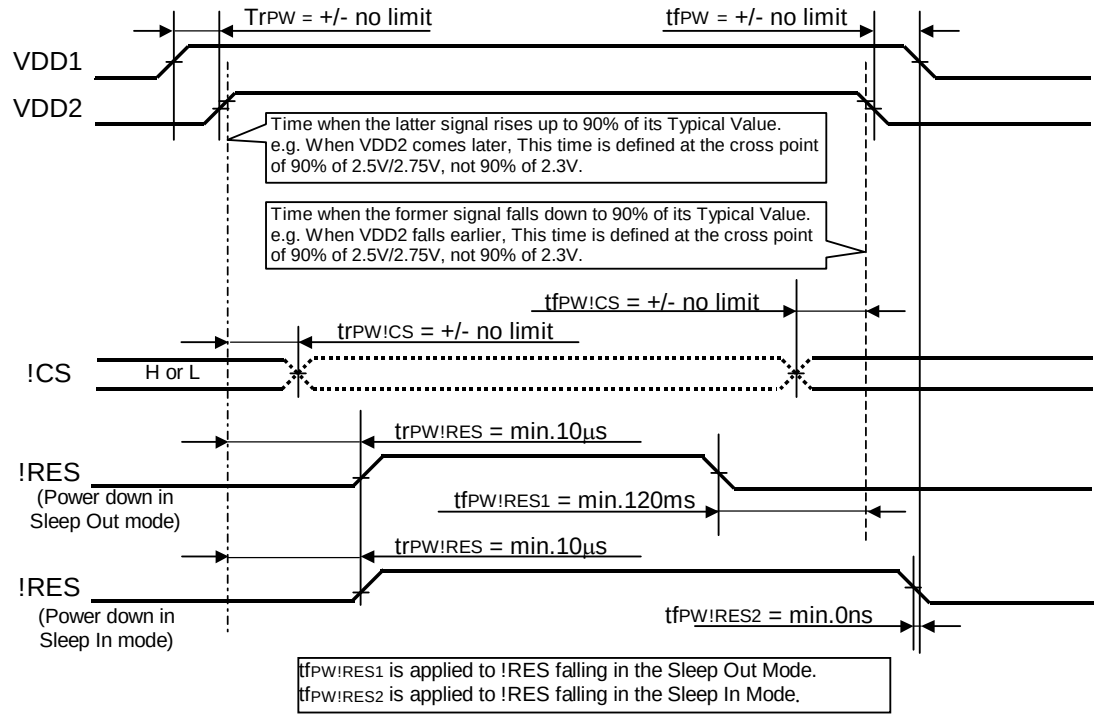
If !RES line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD2 and VDD1 have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

5.10.2 Case 2 – !RES line is held Low by host at Power On

If !RES line is held Low (and stable) by the host during Power On, then the !RES must be held low for minimum 10μsec after both VDD2 and VDD1 have been applied.

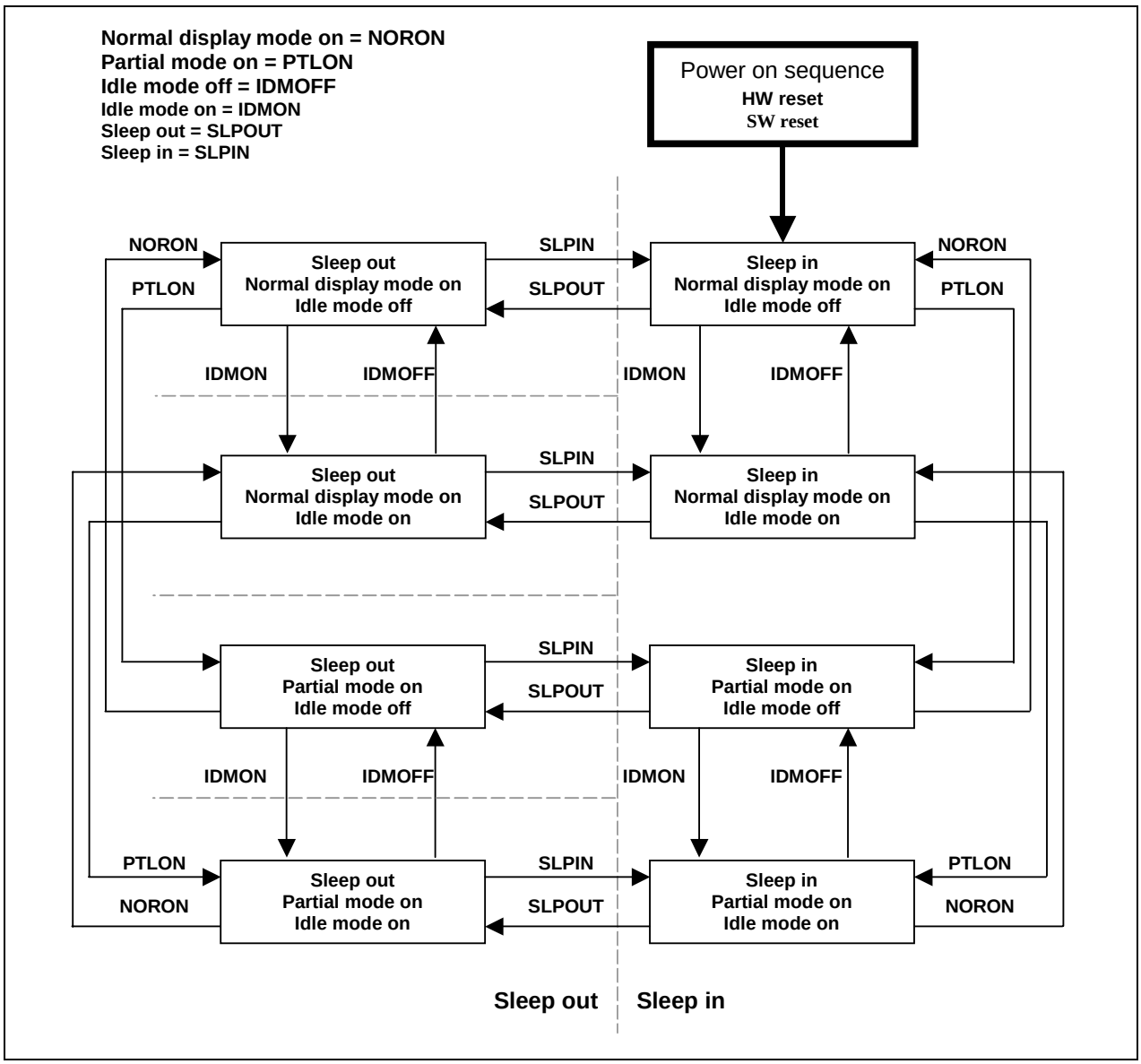


Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

5.11 UNCONTROLLED POWER OFF

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects on the display.

5.12 POWER FLOW CHART FOR DIFFERENT POWER MODES



5.13 INPUT / OUTPUT PIN STATE

5.13.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D17 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
VSYNCO	Low	Low	Low
TEST1	Low	Low	Low

Note: There will be no output from D17-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

5.13.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
!RES	See Section 5.10	Input valid	Input valid	Input valid	See Section 5.10
!CS	Input valid	Input valid	Input valid	Input valid	Input invalid
D/!C	Input valid	Input valid	Input valid	Input valid	Input invalid
!WR	Input valid	Input valid	Input valid	Input valid	Input invalid
!RD	Input valid	Input valid	Input valid	Input valid	Input invalid
D17 to D0	Input valid	Input valid	Input valid	Input valid	Input invalid
HSYNC	Input valid	Input valid	Input valid	Input valid	Input invalid
VSYNC	Input valid	Input valid	Input valid	Input valid	Input invalid
DCK	Input valid	Input valid	Input valid	Input valid	Input invalid
ENABLE	Input valid	Input valid	Input valid	Input valid	Input invalid
VD17 to VD0	Input valid	Input valid	Input valid	Input valid	Input invalid
OSC, CM, GM0, GM1, SRGB, SMX, SMY, P68, BS1, BS0, FRM, EXTC	Input valid	Input valid	Input valid	Input valid	Input invalid

6 INSTRUCTION DESCRIPTION

6.1 INSTRUCTION CODE

6.1.1 Instruction Code Table

Table 6.1.1 Instruction Code

"-": Don't care

Instruction	Refer	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
NOP	6.1.2	0	↑	1	0	0	0	0	0	0	0	0	**(00h)**	No Operation
SWRESET	6.1.3	0	↑	1	0	0	0	0	0	0	0	1	**(01h)**	Software reset
RDDID	6.1.4	0	↑	1	0	0	0	0	0	1	0	0	**(04h)**	Read Display ID
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-	ID1 read
		1	1	↑	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-	ID2 read
		1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-	ID3 read
RDDST	6.1.5	0	↑	1	0	0	0	0	1	0	0	1	**(09h)**	Read Display Status
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	-	-
		1	1	↑	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	-	-
		1	1	↑	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	-	-
		1	1	↑	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	-	-
SLPIN	6.1.6	0	↑	1	0	0	0	1	0	0	0	0	**(10h)**	Sleep in & booster off
SLPOUT	6.1.7	0	↑	1	0	0	0	1	0	0	0	1	**(11h)**	Sleep out & booster on
PTLON	6.1.8	0	↑	1	0	0	0	1	0	0	1	0	**(12h)**	Partial mode on
NORON	6.1.9	0	↑	1	0	0	0	1	0	0	1	1	**(13h)**	Partial off (Normal)
INVOFF	6.1.10	0	↑	1	0	0	1	0	0	0	0	0	**(20h)**	Display inversion off (normal)
INVON	6.1.11	0	↑	1	0	0	1	0	0	0	0	1	**(21h)**	Display inversion on
GAMSET	6.1.12	0	↑	1	0	0	1	0	1	1	1	0	**(26h)**	Gamma set
		1	↑	1	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	**-**	Select desired gamma curve
DISPOFF	6.1.13	0	↑	1	0	0	1	0	1	0	0	0	**(28h)**	Display off
DISPON	6.1.14	0	↑	1	0	0	1	0	1	0	0	1	**(29h)**	Display on
CASET	6.1.15	0	↑	1	0	0	1	0	1	0	1	0	**(2Ah)**	Column address set
		1	↑	1	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	-	X_ADR start: 0 ≤ XS ≤ AFh
		1	↑	1	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-	
		1	↑	1	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	**-**	X_ADR end: XS ≤ XE ≤ AFh
		1	↑	1	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	**-**	
RASET	6.1.16	0	↑	1	0	0	1	0	1	0	1	1	**(2Bh)**	Row address set
		1	↑	1	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	-	Y_ADR start: 0 ≤ YS ≤ CFh / DBh / EFh
		1	↑	1	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-	
		1	↑	1	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	**-**	Y_ADR end: YS ≤ YE ≤ CFh / DBh / EFh
		1	↑	1	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	**-**	
RAMWR	6.1.17	0	↑	1	0	0	1	0	1	1	0	0	**(2Ch)**	Memory write
		1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	-	Write data
RAMRD	6.1.18	0	↑	1	0	0	1	0	1	1	1	0	**(2Eh)**	Memory read
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D7	D6	D5	D4	D3	D2	D1	D0	-	Read data

Table 6.1.2 Instruction Code (Continued)

"-": Don't care

Instruction	Refer	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
RGBSET	6.1.19	0	↑	1	0	0	1	0	1	1	0	1	**(2Dh)**	Color set for 256 or 4k color display
		1	↑	1	-	-	-	R4	R3	R2	R1	R0	-	Red tone (0000)
		1	↑	1	:	:	:	:	:	:	:	:	:	: -
		1	↑	1	-	-	-	R4	R3	R2	R1	R0	-	Red tone (11111)
		1	↑	1	-	-	G5	G4	G3	G2	G1	G0	-	Green tone (0000)
		1	↑	1	:	:	:	:	:	:	:	:	:	: -
		1	↑	1	-	-	G5	G4	G3	G2	G1	G0	-	Green tone (1111)
		1	↑	1	-	-	-	B4	B3	B2	B1	B0	-	Blue tone (0000)
		1	↑	1	:	:	:	:	:	:	:	:	:	: -
		1	↑	1	-	-	-	B4	B3	B2	B1	B0	-	Blue tone (1111)
PTLAR	6.1.20	0	↑	1	0	0	1	1	0	0	0	0	**(30h)**	Partial start/end address set
		1	↑	1	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	-	Partial start address (0,1,2, …, 207/219/239)
		1	↑	1	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-	
		1	↑	1	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	**-**	Partial end address (0,1,2, …, 207/219/239)
		1	↑	1	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	**-**	
SCRLAR	6.1.21	0	↑	1	0	0	1	1	0	0	1	1	**(33h)**	Scroll area set
		1	↑	1	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	-	Top fixed area TFA = 0,1,2, … , 208/220/240
		1	↑	1	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-	
		1	↑	1	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	-	Vertical scroll area VSA = 0,1,2, … , 208/220/240
		1	↑	1	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	**-**	
		1	↑	1	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	**-**	Bottom fixed area BFA = 0,1,2, … , 208/220/240
		1	↑	1	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	**-**	
TEOFF	6.1.22	0	↑	1	0	0	1	1	0	1	0	0	**(34h)**	Tearing effect line off
TEON	6.1.23	0	↑	1	0	0	1	1	0	1	0	1	**(35h)**	Tearing effect mode set & on
		1	↑	1	-	-	-	-	-	-	-	M	**-**	M="0": Mode1, M="1": Mode2
MADCTR	6.1.24	0	↑	1	0	0	1	1	0	1	1	0	**(36h)**	Memory data access control
		1	↑	1	MY	MX	MV	ML	RGB	-	-	-	-	-
VSCSAD	6.1.25	0	↑	1	0	0	1	1	0	1	1	1	**(37h)**	Scroll start address of RAM
		1	↑	1	SSA15	SSA14	SSA13	SSA12	SSA11	SSA10	SSA9	SSA8	-	SSA = 0, 1, 2, … , 207/219/239
		1	↑	1	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	**-**	
IDMOFF	6.1.26	0	↑	1	0	0	1	1	1	0	0	0	**(38h)**	Idle mode off
IDMON	6.1.27	0	↑	1	0	0	1	1	1	0	0	1	**(39h)**	Idle mode on
COLMOD	6.1.28	0	↑	1	0	0	1	1	1	0	1	0	**(3Ah)**	Interface pixel format
		1	↑	1	-	-	-	-	-	P2	P1	P0	-	Interface format
RDID1	6.1.29	0	↑	1	1	1	0	1	1	0	1	0	**(DAh)**	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-	Read parameter
RDID2	6.1.30	0	↑	1	1	1	0	1	1	0	1	1	**(DBh)**	Read ID2
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-	Read parameter
RDID3	6.1.31	0	↑	1	1	1	0	1	1	1	0	0	**(DCh)**	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-	Read parameter

Table 6.1.3 Instruction Code (Extended code set)

"-": Don't care

Instruction	Refer	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
CLKINT	6.1.32	0	↑	1	1	0	1	1	0	0	0	0	**(B0h)**	Internal oscillator select
CLKEXT	6.1.33	0	↑	1	1	0	1	1	0	0	0	1	**(B1h)**	External oscillator select
INVCTR	6.1.34	0	↑	1	1	0	1	1	0	0	1	0	**(B2h)**	Display inversion control
		1	↑	1	DANA	TWIA	INVA	FR2A	-	NLA2	NLA1	NLA0	-	Line inversion (full color)
		1	↑	1	DANB	TWIB	INVB	FR2B	-	NLB2	NLB1	NLB0	-	Line inversion (8-color)
PATCTR	6.1.35	0	↑	1	1	0	1	1	0	0	1	1	**(B3h)**	Partial display off area control
		1	↑	1	-	-	-	-	-	PF2	PF1	PF0	**-**	Source / gate driving cycle set
GAMCTR	6.1.36	0	↑	1	1	0	1	1	0	1	0	0	**(B4h)**	Set gamma correction characteristics
		1	↑	1	-	-	-	-	DCP13	DCP12	DCP11	DCP10	-	Gamma adjustment (+ polarity)
		1	↑	1	-	SP12	SP11	SP10	-	SP02	SP01	SP00	-	Gamma adjustment (+ polarity)
		1	↑	1	-				DCN13	DCN12	DCN11	DCN10	-	Gamma adjustment (- polarity)
		1	↑	1	-	SN12	SN11	SN10	-	SN02	SN01	SN00	-	Gamma adjustment (- polarity)
		1	↑	1	-	SP32	SP31	SP30	-	SP22	SP21	SP20	-	Gamma adjustment (+ polarity)
		1	↑	1	-	SP52	SP51	SP50	-	SP42	SP41	SP40	-	Gamma adjustment (+ polarity)
		1	↑	1	-	SP72	SP71	SP70	-	SP62	SP61	SP60	-	Gamma adjustment (+ polarity)
		1	↑	1	-	SN32	SN31	SN30	-	SN22	SN21	SN20	-	Gamma adjustment (- polarity)
		1	↑	1	-	SN52	SN51	SN50	-	SN42	SN41	SN40	-	Gamma adjustment (- polarity)
		1	↑	1	-	SN72	SN71	SN70	-	SN62	SN61	SN60	-	Gamma adjustment (- polarity)
IFMODE	6.1.37	0	↑	1	1	0	1	1	0	1	0	1	**(B5h)**	Set display interface mode
		1	↑	1	-	-	-	-	-	-	IF1	IF0	-	Data transfer mode set
		1	↑	1	-	-	DW1	DW0	DP	EP	HSP	VSP	-	RGB I/F data width & Clock polarity set
EPWRIN	6.1.38	0	↑	1	1	0	1	1	0	1	1	0	**(B6h)**	EEPROM write start
EPWROUT	6.1.39	0	↑	1	1	0	1	1	0	1	1	1	**(B7h)**	EEPROM write end
DISCLK	6.1.40	0	↑	1	1	0	1	1	1	0	0	0	**(B8h)**	Display clock set
		1	↑	1	-	-	-	-	-	-	-	HA8		MSB of 1H (full-color)
		1	↑	1	HA7	HA 6	HA 5	HA 4	HA 3	HA 2	HA 1	HA 0	-	Number of clocks during 1H (full-color)
		1	↑	1	-	-	BPA5	BPA4	BPA3	BPA2	BPA1	BPA0	-	Number of vertical back porches (full-color)
		1	↑	1	-	-	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0	-	Number of vertical front porches (full-color)
		1	↑	1	-	-	-	-	-	-	-	HB8		MSB of 1H (8-color)
		1	↑	1	HB7	HB 6	HB 5	HB 4	HB 3	HB 2	HB 1	HB 0	-	Number of clocks during 1H (8-color)
		1	↑	1	-	-	BPB5	BPB4	BPB3	BPB2	BPB1	BPB0	-	Number of vertical back porches (8-color)
		1	↑	1	-	-	FPB5	FPB4	FPB3	FPB2	FPB1	FPB0	-	Number of vertical front porches (8-color)
WRID2	6.1.41	0	↑	1	1	1	0	1	1	0	0	1	**(D9h)**	Write ID2 for EEPROM program
		1	↑	1	1	-	-	-	ID23	ID22	ID21	ID20	-	Just ID2 [3:0] are stored in EEPROM
VCOMOFS	6.1.42	0	↑	1	1	0	1	1	1	0	0	1	**(B9h)**	VCOM Offset control
		1	↑	1	-	-	VCOF5	VCOF4	VCOF3	VCOF2	VCOF1	VCOF0	**-**	VCOM middle voltage trimming
VCOMCTR	6.1.43	0	↑	1	1	0	1	1	1	0	1	0	**(BAh)**	VCOML/VCOMH voltage control
		1	↑	1	-	-	VCLC5	VCLC4	VCLC3	VCLC2	VCLC1	VCLC0	**-**	-2.5V ~ +0.5V (50mV step)
		1	↑	1	-	-	VCHC5	VCHC4	VCHC3	VCHC2	VCHC1	VCHC0	**-**	+2.5V ~ +5.5V (50mV step)
PWRCTR	6.1.44	0	↑	1	1	0	1	1	1	0	1	0	**(BBh)**	Booster On/Off Control
		1	↑	1	VCREG	VCL	VGHL	VG	VS	VR	AVD	OSC	-	On/Off control
OUTCTR	6.1.45	0	↑	1	1	0	1	1	1	0	1	1	**(BCh)**	Output on/off control
		1	↑	1	-	-	-	-	-	VCOM	GATE	SRC	-	On/Off control
REGCTR	6.1.46	0	↑	1	1	0	1	1	1	1	0	0	**(BDh)**	Regulator control
		1	↑	1	-	VRS2	VRS1	VRS0	-	VSG2	VSG1	VSG0	-	VR/VS/VG regulator output voltage control

Table 6.1.4 Instruction Code (Extended code set, continued)

"-": Don't care

Instruction	Refer	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)	Function
AMPCTR	6.1.47	0	↑	1	1	0	1	1	1	1	0	1	**(BEh)**	OP-amp current control
		1	↑	1	0	0	0-	0	0	0	0	0	-	-
		1	↑	1	-	-	-	-	SACS3	SACS2	SACS1	SACS0		Source amp current control
		1	↑	1	-	-	-	-	GACS3	GACS2	GACS1	GACS0		Gamma amp current control
BSTCLK	6.1.48	0	↑	1	1	0	1	1	1	1	1	1	**(BFh)**	Booster clock select
		1	↑	1	-	-	-	-	FGA3	FGA2	FGA1	FGA0	-	Booster clock 1 for full-color mode
		1	↑	1	-	-	-	-	FCA3	FCA2	FCA1	FCA0	-	Booster clock 2 for full-color mode
		1	↑	1	-	-	-	-	FAA3	FAA2	FAA1	FAA0	-	Booster clock 3 for full-color mode
		1	↑	1	-	-	-	-	FGB3	FGB2	FGB1	FGB0	-	Booster clock 1 for 8-color mode
		1	↑	1	-	-	-	-	FCB3	FCB2	FCB1	FCB0	-	Booster clock 2 for 8-color mode
		1	↑	1	-	-	-	-	FAB3	FAB2	FAB1	FAB0	-	Booster clock 3 for 8-color mode
		1	↑	1	-	-	-	-	-	-	VMS	VCD	-	Boosting method & ratio select for AVDD
VGLCTR	6.1.49	0	↑	1	1	1	0	0	0	0	0	0	**(C0h)**	Gate low level control
		1	↑	1	-	-	-	-	-	-	VGLS1	VGLS0	**-**	
SGTCTR	6.1.50	0	↑	1	1	1	0	0	0	0	0	1	**(C1h)**	Source/Gate on/off time control
		1	↑	1	0	0	0	0	0	0	0	0	**-**	-
		1	↑	1	0	0	0	0	0	0	0	0	**-**	-
		1	↑	1	GON7	GON6	GON5	GON4	GON3	GON2	GON1	GON0	**-**	Gate output ON timing
		1	↑	1	GOF7	GOF6	GOF5	GOF4	GOF3	GOF2	GOF1	GOF0	**-**	Gate output OFF time
IFMPU	6.1.51	0	↑	1	1	1	0	0	0	0	1	0	**(C2h)**	MPU Interface mode select (Test mode)
		1	↑	1	-	-	-	-	-	PP68	PBS1	PBS0	**-**	-
REGAPP	6.1.52	0	↑	1	1	1	1	1	1	0	0	0	**(F8h)**	Register direct access (Just for TEST)
		1	↑	1	0	0	0	0	0	0	0	RAPP	**-**	-
REGAPP1	5.1.53	0	↑	1	1	1	1	1	0	0	1	0	**(F2h)**	VCOMH register value access control
		1	↑	1	0	0	**1**	0	0	0	0	RAPP1	**-**	(Just for TEST)
TEST1	6.1.54	0	↑	1	1	1	1	0	-	-	-	-	**(E-h)**	Test command1.
TEST2	6.1.55	0	↑	1	1	1	1	1	-	-	-	-	**(F-h)**	Test command2.

NOTE:

1) After the H/W reset by !RES pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

2) To use extended code set, EXTC pad should be connected to VDD1 and expended code set is just used for module test and if EXTC is not connected to VDD1, all the extended code set will be ignored and regarded as NOP (00h) command.

3) Undefined commands are treated as NOP (00 h) command.

4) Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

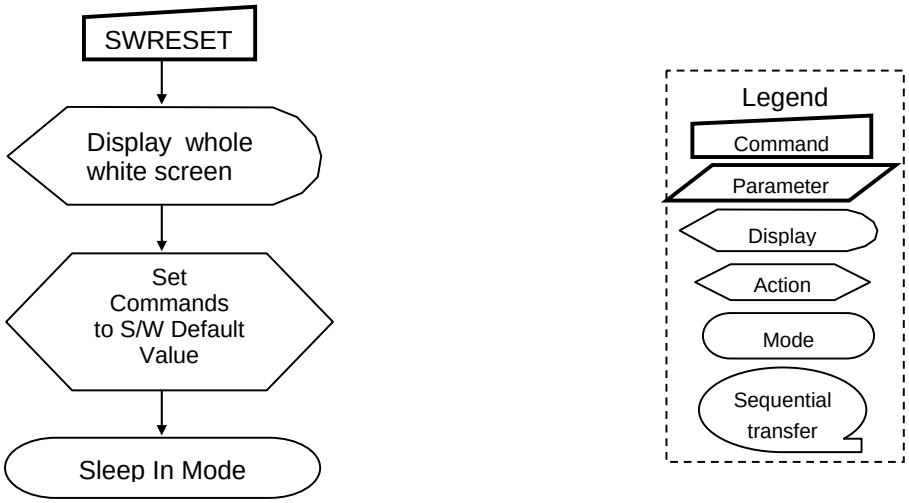
6.1.2 NOP (00h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NOP	0	↑	1	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter											

Description	This command is empty command. It does not have effect on the display module. However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write), RAMRD (Memory Read) and parameter write commands.
Restriction	-
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes
Default	Status / Default Value Power On Sequence / N/A S/W Reset / N/A H/W Reset / N/A
Flow Chart	-

6.1.3 SWRESET: Software Reset (01h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SWRESET	0	↑	1	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter											

Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to VSS (display off). (See default tables in each command description) *Note: The Frame Memory contents are not affected by this command.*
Restriction	It will be necessary to wait 5msec before sending new command following software reset
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: N/A Status: S/W Reset — Default Value: N/A Status: H/W Reset — Default Value: N/A
Flow Chart	

6.1.4 RDDID: Read Display ID (04h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDID	0	↑	1	0	0	0	0	0	1	0	0	(04h)
Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
3rd parameter	1	1	↑	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
4th parameter	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

Description

This read byte returns 24-bit display identification information.

The 1st parameter is dummy data

The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

The 3rd parameter (ID26 to ID20): LCD module/driver version ID

The 4th parameter (ID37 to UD30): LCD module/driver ID.

NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.

Restriction

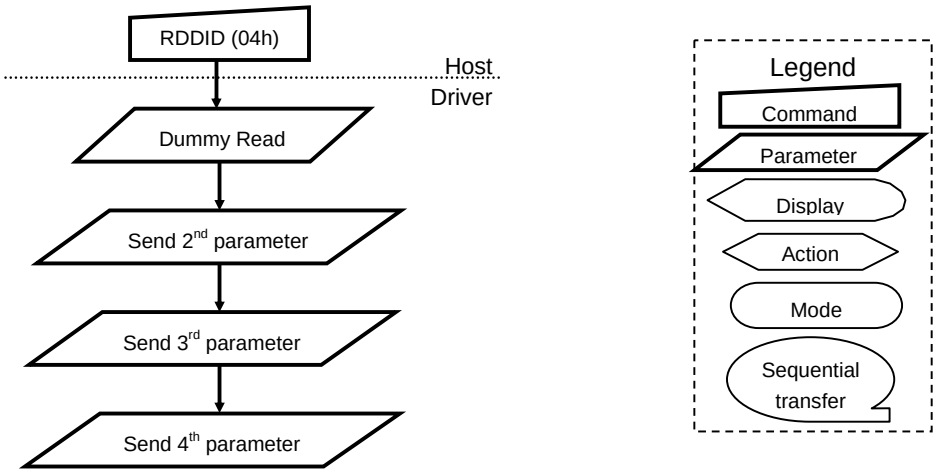
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	45h	80~FFh (Not Fixed)	14h
S/W Reset	45h	80~FFh (Not Fixed)	14h
H/W Reset	45h	80~FFh (Not Fixed)	14h

Flow Chart



6.1.5 RDDST: Read Display Status (09h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDST	0	↑	1	0	0	0	0	1	0	0	1	(09h)
Dummy Read	1	1	↑	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	-
3rd parameter	1	1	↑	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	-
4th parameter	1	1	↑	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	-
5th parameter	1	1	↑	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
ST31	Booster Voltage Status	"1"=Booster on, "0"=off
ST30	Row Address Order (MY)	"1"=Decrement, "0"=Increment
ST29	Column Address Order (MX)	"1"=Decrement, "0"=Increment
ST28	Row/Column Exchange (MV)	"1"= Row/column exchange (MV=1) "0"= Normal (MV=0)
ST27	Scan Address Order (ML)	"1"=Decrement, "0"=Increment
ST26	RGB/BGR Order (RGB)	"1"=BGR, "0"=RGB
ST25	Not Used	"0"
ST24	Not Used	"0"
ST23	Not Used	"0"
ST22 ST21 ST20	Interface Colour Pixel Format Definition	"010" = 8-bit / pixel, "011" = 12-bit / pixel "101" = 16-bit / pixel, "110" = 18-bit / pixel
ST19	Idle Mode On/Off	"1" = On, "0" = Off
ST18	Partial Mode On/Off	"1" = On, "0" = Off
ST17	Sleep In/Out	"1" = Out, "0" = In
ST16	Display Normal Mode On/Off	"1" = Normal Display, "0" = Partial Display
ST15	Vertical Scrolling Status	"1" = Scroll on, "0" = Scroll off
ST14	Not Used	"0"
ST13	Inversion Status	"1" = On, "0" = Off
ST12	All Pixels On (Not Used)	"0"
ST11	All Pixels Off (Not Used)	"0"
ST10	Display On/Off	"1" = On, "0" = Off
ST9	Tearing effect line on/off	"1" = On, "0" = Off
ST8 ST7 ST6	Gamma curve selection	ST.[8:6] = "000" = Gamma curve 1 (GC0) ST.[8:6] = "001" = Gamma curve 2 (GC1) ST.[8:6] = "010" = Gamma curve 3 (GC2) ST.[8:6] = "011" = Gamma curve 4 (GC2) ST.[8:6] = "1xx" = Not defined ("x"=don't care)
ST5	Tearing effect line mode	"0" = mode1, "1" = mode2
ST4	Not Used	"0"
ST3	Not Used	"0"
ST2	Not Used	"0"
ST1	Not Used	"0"
ST0	Not Used	"0"

Restriction

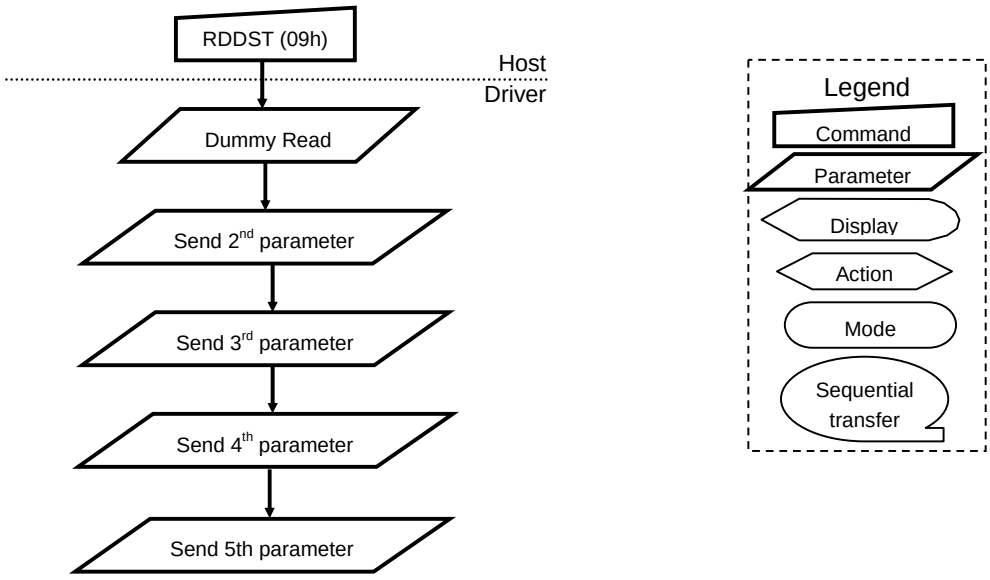
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

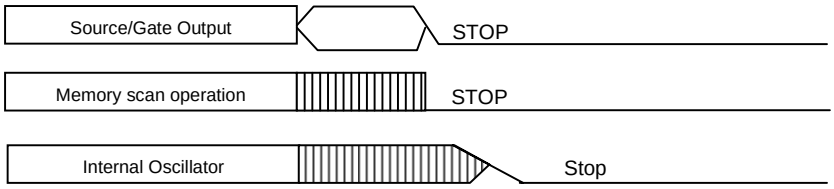
Status	Default Value (ST31 to ST0)		Default Valu
Power On Sequence	0000 0000_0101 0001_0000 0000_0000 0000		See Descripti
S/W Reset	0XXX XX00_0XXX 0001_0000 0000_0000 0000		See Descripti
H/W Reset	0000 0000_0101 0001_0000 0000_0000 0000		See Descripti

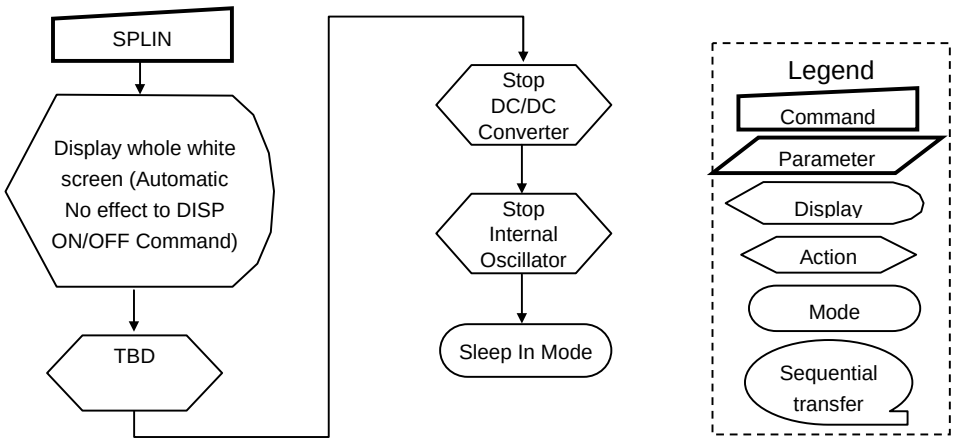
Flow Chart



6.1.6 SLPIN: Sleep In (10h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPIN	0	↑	1	0	0	0	1	0	0	0	0	(10h)
Parameter	No Parameter											

Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.  MCU interface and memory are still working and the memory keeps its contents It will take about 120 msec for the supply voltages to stabilise to 0V. But there is no wait time limitation for the next command.
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: Sleep in mode Status: S/W Reset — Default Value: Sleep in mode Status: H/W Reset — Default Value: Sleep in mode

Flow Chart	It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued. The results of booster off can be check by RDDST (09h) command Bit31. 

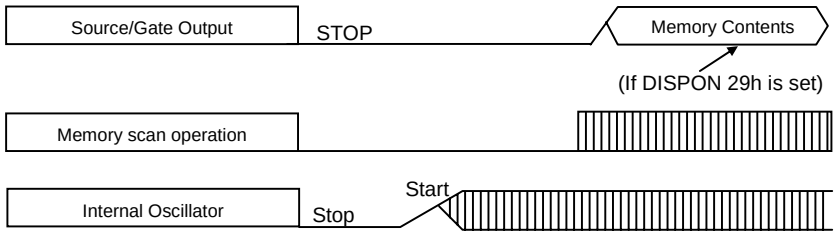
6.1.7 SLPOUT: Sleep Out (11h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPOUT	0	↑	1	0	0	0	1	0	0	0	1	(11h)
Parameter	No Parameter											

Description

This command turns off sleep mode.

In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.



Restriction

This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).

It will be necessary to wait 120msec for the supply voltages and clock circuits to stabilize.

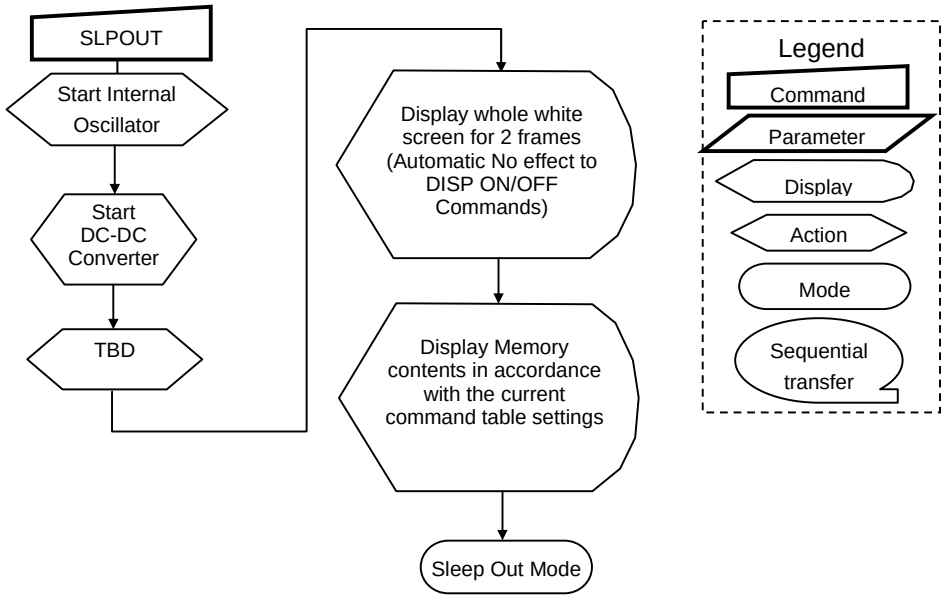
But there is no wait time limitation for the next command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart	It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued. The results of booster on can be checked by RDDST (09h) command Bit31. 

6.1.8 PTLON: Partial Display Mode On (12h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLON	0	↑	1	0	0	0	1	0	0	1	0	(12h)
Parameter	No Parameter											

Description	This command turns on Partial mode. The partial mode window is described by the Partial Area command (30_H) Exit from PTLON by Normal Display Mode On command (13_H) There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.
Restriction	This command has no effect when Partial mode is active.
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: Partial mode off Status: S/W Reset — Default Value: Partial mode off Status: H/W Reset — Default Value: Partial mode off
Flow Chart	See Partial Area (30h)

6.1.9 NORON: Normal Display Mode On (13h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NORON	0	↑	1	0	0	0	1	0	0	1	1	(13h)
Parameter	No Parameter											

Description	This command returns the display to normal mode. Normal display mode on means Partial mode off, Scroll mode Off. Exit from NORON by the Partial mode On command (12h) There is no abnormal visual effect during mode change from Normal mode On to Partial mode On.
Restriction	This command has no effect when Normal Display mode is active.
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status: Default Value Power On Sequence: Normal Mode On S/W Reset: Normal Mode On H/W Reset: Normal Mode On
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command

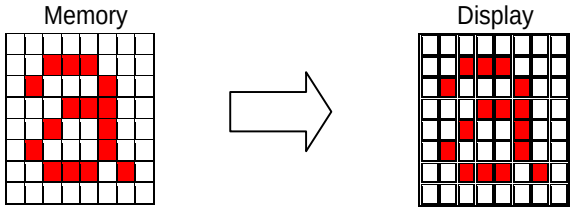
6.1.10 INVOFF: Display Inversion Off (20h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVOFF	0	↑	1	0	0	1	0	0	0	0	0	(20h)
Parameter	No parameter											

Description

This command is used to recover from display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.

(Example)



Restriction

This command has no effect when module is already inversion off mode.

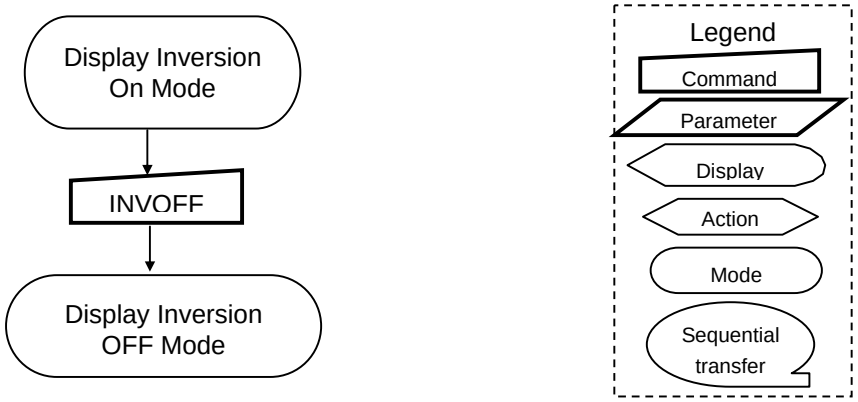
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



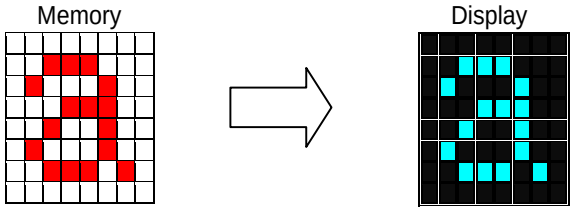
6.1.11 INVON: Display Inversion On (21h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVON	0	↑	1	0	0	1	0	0	0	0	1	(21h)
Parameter	No Parameter											

Description

This command is used to enter into display inversion mode
This command makes no change of contents of frame memory.
This command does not change any other status.
To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

(Example)



Restriction

This command has no effect when module is already Inversion On mode.

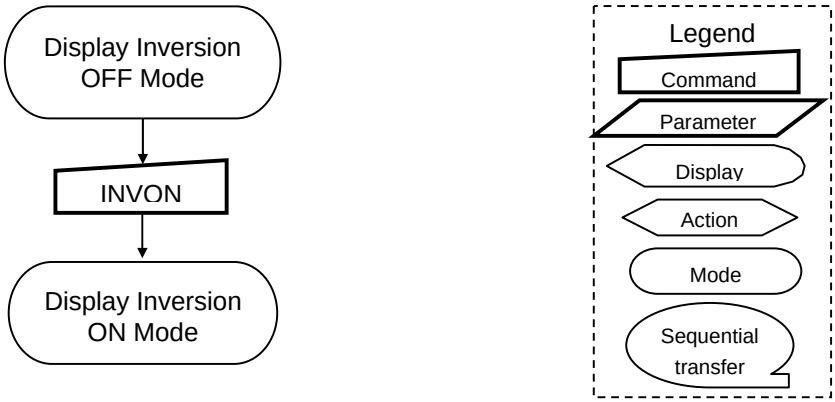
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



6.1.12 GAMSET: Gamma Set (26h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRCNTR	0	↑	1	0	0	1	0	0	1	0	1	(26h)
Parameter	1	↑	1	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	-

NOTE: "-" Don't care

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curves are defined in Fig 5.9.5 The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC [7:0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1
02h	GC1	Gamma Curve 2
04h	GC2	Gamma Curve 3
08h	GC3	Gamma Curve 4

Note: All other values are undefined.

Restriction

Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid is received.

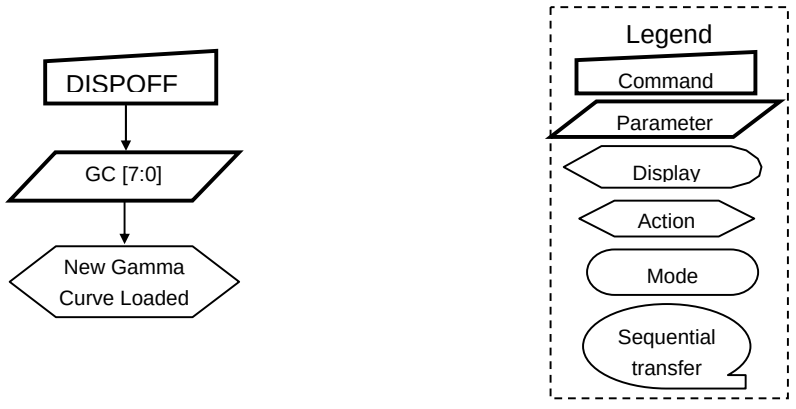
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



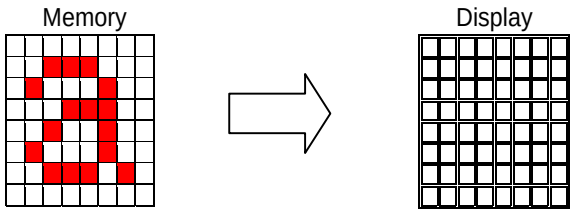
6.1.13 DISPOFF: Display Off (28h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPOFF	0	↑	1	0	0	1	0	1	0	0	0	(28h)
Parameter	No Parameter											

Description

This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disables and white page inserted.
This command makes no change of contents of frame memory.
This command does not change any other status.
There will be no abnormal visible effect on the display.
Exit from this command by Display On (29h)

(Example)



Restriction

This command has no effect when module is already in Display Off mode.

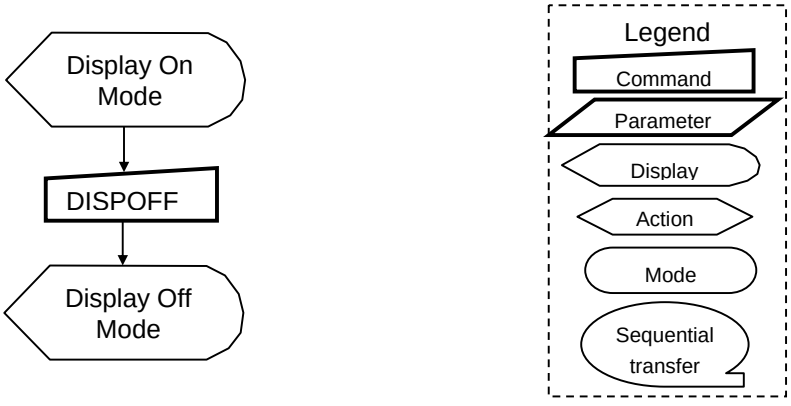
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



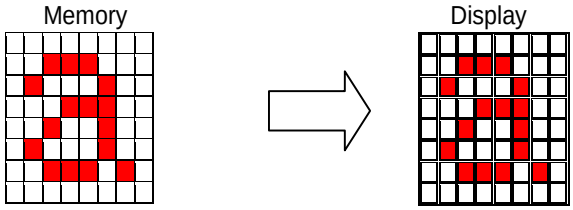
6.1.14 DISPON: Display On (29h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPON	0	↑	1	0	0	1	0	1	0	0	1	(29h)
Parameter	No Parameter											

Description

This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.

(Example)



Restriction

This command has no effect when module is already in Display On mode.

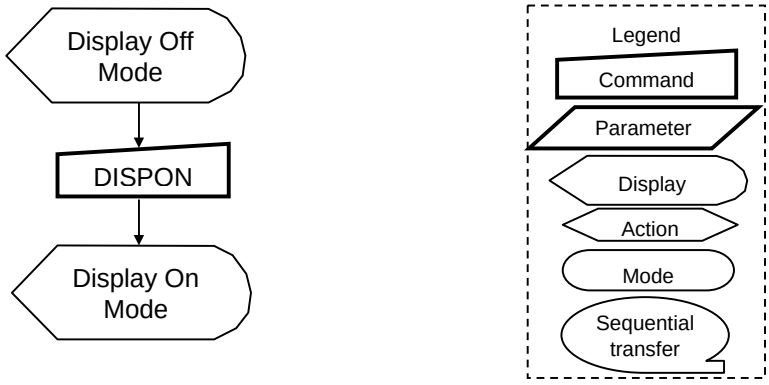
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



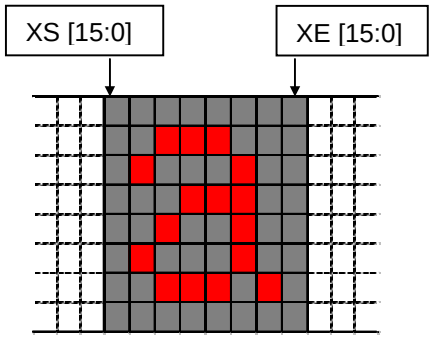
6.1.15 CASET: Column Address Set (2Ah)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CASET	0	↑	1	0	0	1	0	1	0	1	0	(2Ah)
1st Parameter	1	↑	1	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS9	-
2nd Parameter	1	↑	1	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-
3rd Parameter	1	↑	1	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	-
4th Parameter	1	↑	1	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The value of XS [15:0] and XE [15:0] are referred when RAMWR command comes.
Each value represents one column line in the Frame Memory.

(Example)



Restriction

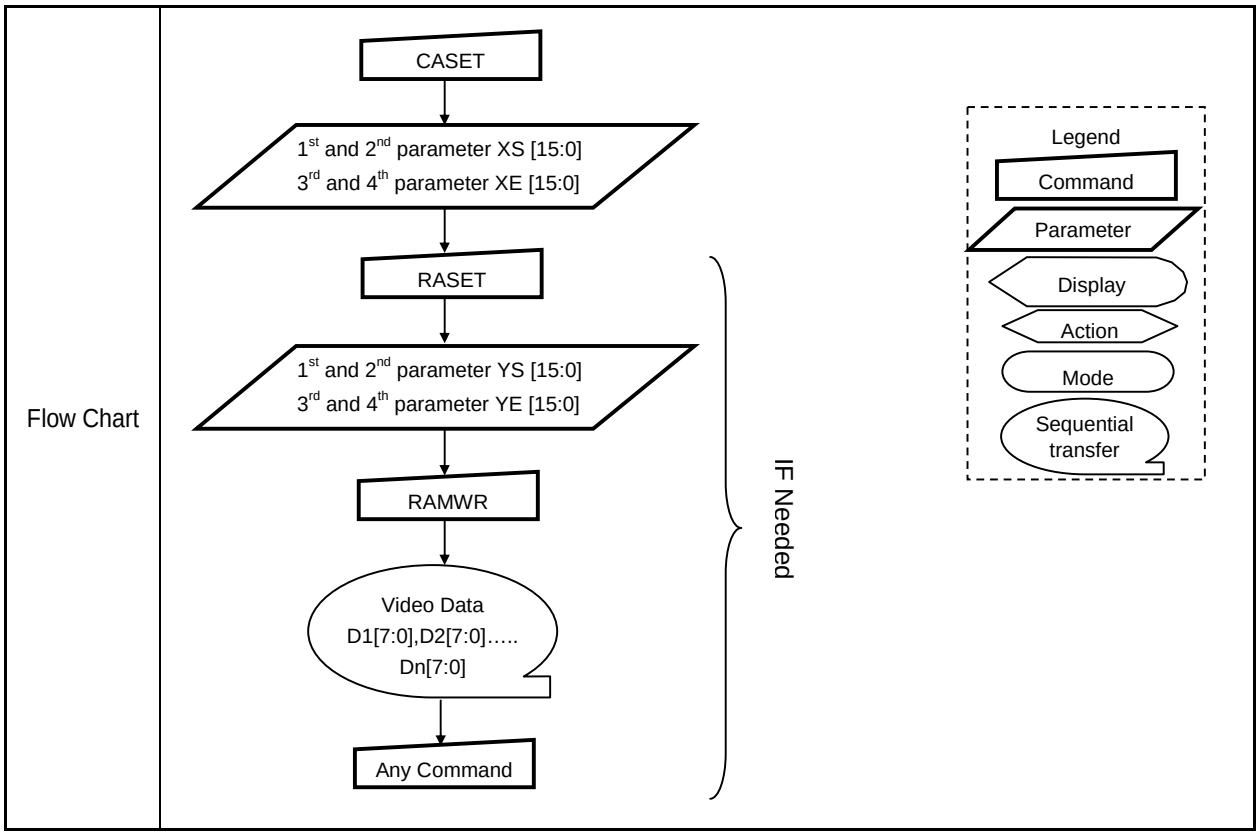
XS [15:0] always must be equal to or less than XE [15:0]
When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.
(Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 175 (AFh), when GM=don't care and MV=0)
(Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 207 (CFh), when GM="00" and MV=1)
(Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 219 (DBh), when GM="01" and MV=1)
(Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 239 (EFh), when GM="10" and MV=1)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	XS [15:0]	XE [15:0]
Power On Sequence	00h	AFh
S/W Reset	00h	AFh
H/W Reset	00h	AFh


Flow Chart
CASET
1st and 2nd parameter XS [15:0]
3rd and 4th parameter XE [15:0]
RASET
1st and 2nd parameter YS [15:0]
3rd and 4th parameter YE [15:0]
RAMWR
Video Data
D1[7:0],D2[7:0].....
Dn[7:0]
Any Command
IF Needed
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

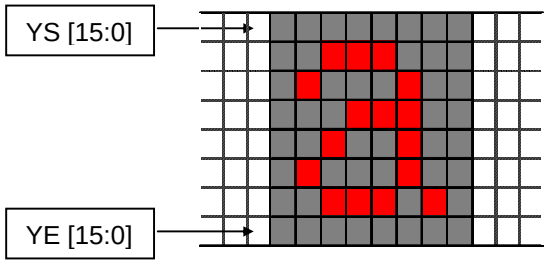
6.1.16 RASET: Row Address Set (2Bh)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RASET	0	↑	1	0	0	1	0	1	0	1	1	(2Bh)
1st parameter	1	↑	1	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	-
2nd parameter	1	↑	1	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-
3rd Parameter	1	↑	1	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	-
4th Parameter	1	↑	1	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes.
Each value represents one column line in the Frame Memory.

(Example)



Restriction

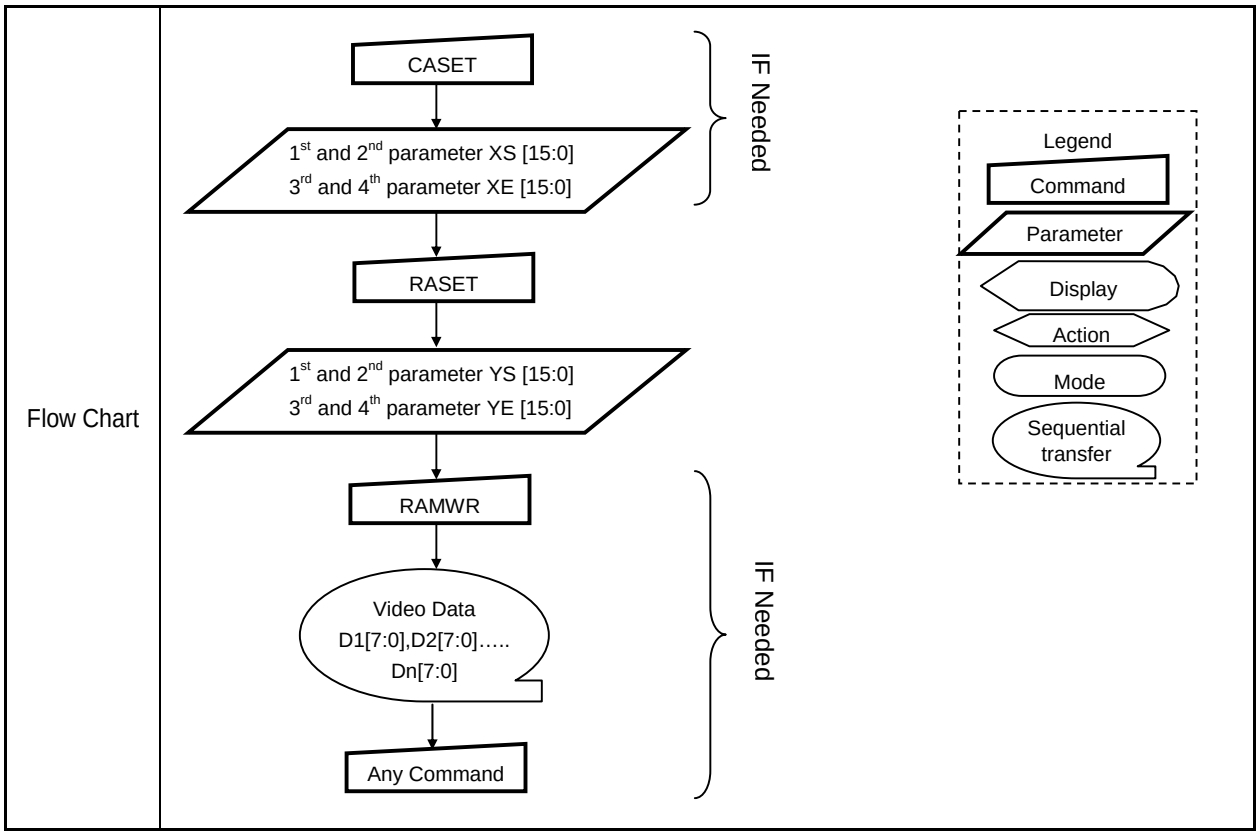
YS [15:0] always must be equal to or less than YE [15:0]
When YS [15:0] or YE [15:0] is greater than maximum row address like below, data of out of range will be ignored.
(Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 207 (CFh), when GM="00" and MV=0)
(Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 219 (DBh), when GM="01" and MV=0)
(Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 239 (EFh), when GM="10" and MV=0)
(Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 175 (AFh), when GM=don't care and MV=1)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	YS [15:0]			YE [15:0]		
	GM=00	GM=01	GM=10	GM=00	GM=01	GM=10
Power On Sequence	00h	00h	00h	CFh	DBh	EFh
S/W Reset	00h	00h	00h	CFh	DBh	EFh
H/W Reset	00h	00h	00h	CFh	DBh	EFh


Flow Chart
CASET
1st and 2nd parameter XS [15:0]
3rd and 4th parameter XE [15:0]
IF Needed
RASET
1st and 2nd parameter YS [15:0]
3rd and 4th parameter YE [15:0]
RAMWR
Video Data
D1[7:0],D2[7:0].....
Dn[7:0]
Any Command
IF Needed
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.1.17 RAMWR: Memory Write (2Ch)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMWR	0	↑	1	0	0	1	0	1	1	0	0	(2Ch)
Data write	1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	-
:	:	:	:	:	:	:	:	:	:	:	:	:
Data write	1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	-

Description

This command is used to transfer data MCU to frame memory.
This command makes no change to the other driver status.
When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.
The Start Column/Start Page positions are different in accordance with MADCTL setting. (See 5.2.3)
Then D [7:0] is stored in frame memory and the column register and the page register incremented as in ***Fig 5.2.4***.
Sending any other command can stop Frame Write.

Restriction

In all color modes, there is no restriction on length of parameters.

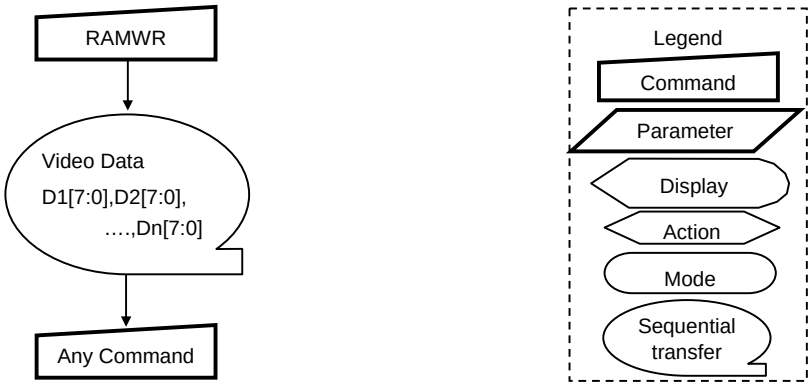
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



6.1.18 RAMRD: Memory Read (2Eh)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMRD	0	↑	1	0	0	1	0	1	1	1	0	(2Eh)
Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
Data read	1	1	↑	D7	D6	D5	D4	D3	D2	D1	D0	-
:	:	:	:	:	:	:	:	:	:	:	:	:
Data read	1	1	↑	D7	D6	D5	D4	D3	D2	D1	D0	-

Description

This command is used to transfer data from frame memory to MCU.
This command makes no change to the other driver status.
When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.
The Start Column/Start Page positions are different in accordance with MADCTL setting. (See 5.2.3)
Then D [7:0] is read back from the frame memory and the column register and the row register incremented as in ***Fig. 5.2.4***.
Sending any other command can stop Frame Read.

Restriction

In all color modes, the Frame Read is always 16-bit (when CM=0) or 18-bit (when CM=1) so there is no restriction on length of parameters.

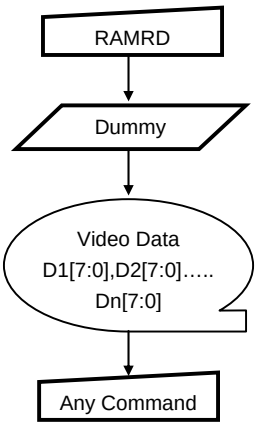
Register Availability

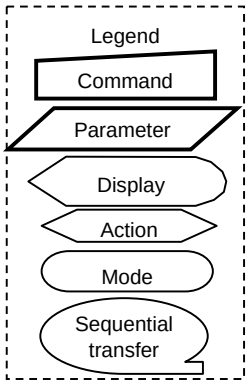
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart





6.1.19 RGBSET: Colour Set for 4k or 256-Color Display (2Dh)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RGBSET	0	↑	1	0	0	1	0	1	1	0	1	(2Dh)
1st parameter	1	↑	1	-	-	-	R004	R003	R002	R001	R000	-
:	1	↑	1	-	-	-	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	-
16th parameter	1	↑	1	-	-	-	R154	R153	R152	R151	R150	-
17th parameter	1	↑	1	-	-	G005	G004	G003	G002	G001	G000	-
:	1	↑	1	-	-	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	-
32nd parameter	1	↑	1	-	-	G155	G154	G153	G152	G151	G150	-
33rd parameter	1	↑	1	-	-	-	B004	B003	B002	B001	B000	-
:	1	↑	1	-	-	-	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	-
48th parameter	1	↑	1	-	-	-	B154	B153	B152	B151	B150	-

Description

This command is used to define the LUT for 8bit-to-16bit / 12-bit-to-16bit color depth conversations.
48 Bytes must be written to the LUT regardless of the color mode. Only the values in Section 5.2.8 are referred.
This command has no effect on other commands/parameters and Contents of frame memory.
Visible change takes effect next time the Frame Memory is written to.

Restriction

Do not send any command before the last data is sent or LUT is not defined correctly.

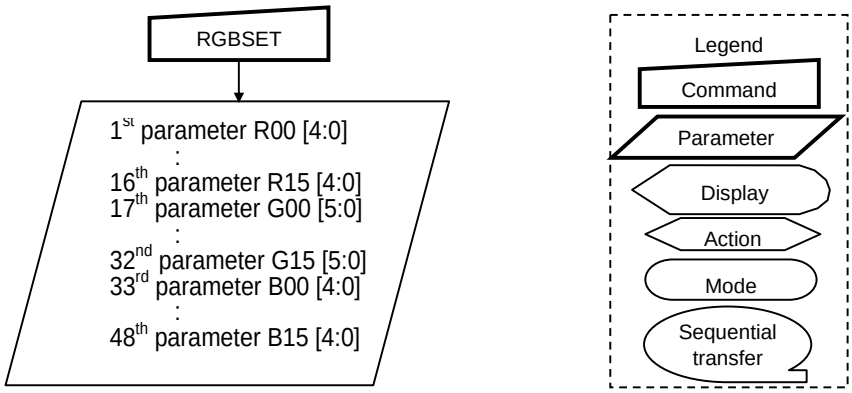
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See Section 5.2.8
S/W Reset	Contents of the look-up table protected
H/W Reset	See Section 5.2.8

Flow Chart



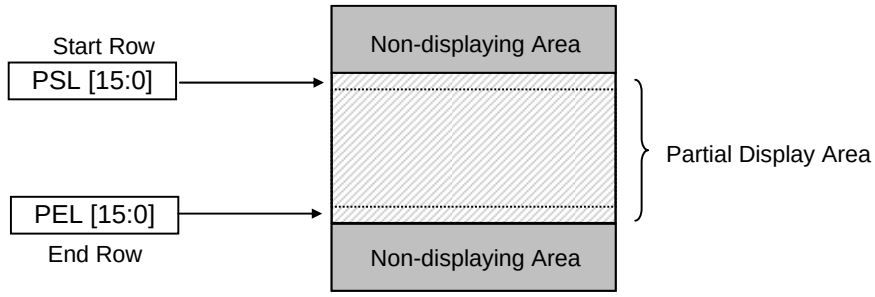
6.1.20 PTLAR: Partial Area (30h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLAR	0	↑	1	0	0	1	1	0	0	0	0	(30h)
1st parameter	1	↑	1	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	-
2nd parameter	1	↑	1	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-
3rd parameter	1	↑	1	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	-
4th parameter	1	↑	1	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-

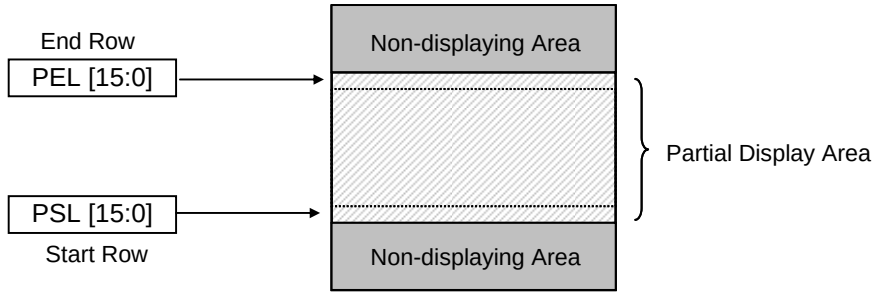
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

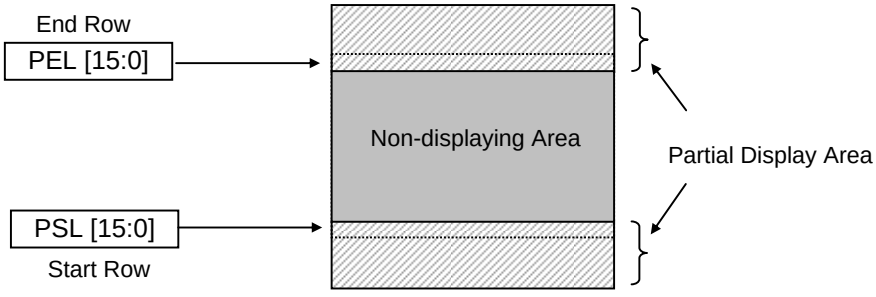
If End Row > Start Row when MADCTL ML=0:



If End Row > Start Row when MADCTL ML=1:



If End Row < Start Row when MADCTL ML=0:



If End Row = Start Row then the Partial Area will be one row deep.

Restriction

PSL[15:0] and PEL[15:0] should have below range
(Parameter range: 0 ≤ PSL[15:0], PEL[15:0] ≤ 207 (CFh), when GM="00")
(Parameter range: 0 ≤ PSL[15:0], PEL[15:0] ≤ 219 (DBh), when GM="01")
(Parameter range: 0 ≤ PSL[15:0], PEL[15:0] ≤ 239 (EFh), when GM="10")

Register Availability

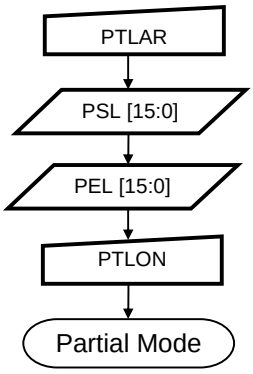
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

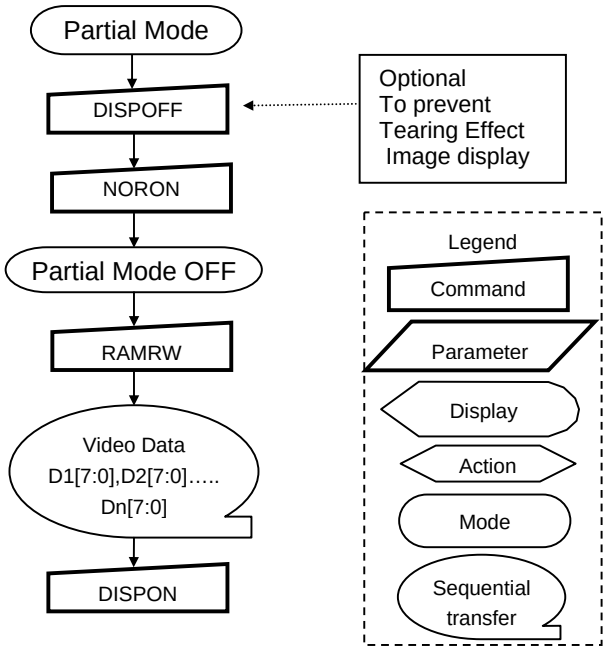
Status	Default Value			
	PSL [15:0]	PEL [15:0]		
		GM=00	GM=01	GM=10
Power On Sequence	00h	CFh	DBh	EFh
S/W Reset	00h	CFh	DBh	EFh
H/W Reset	00h	CFh	DBh	EFh

Flow Chart

1. To Enter Partial Mode



2. To Exit Partial Mode



6.1.21 SCRLAR: Scroll Area (33h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SCRLAR	0	↑	1	0	0	1	1	0	0	1	1	(33h)
1st parameter	1	↑	1	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	-
2nd parameter	1	↑	1	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-
3rd parameter	1	↑	1	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	-
4th parameter	1	↑	1	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-
5th parameter	1	↑	1	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	-
6th parameter	1	↑	1	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-

Description

This command defines the Vertical Scrolling Area of the display.

When MADCTL ML=0

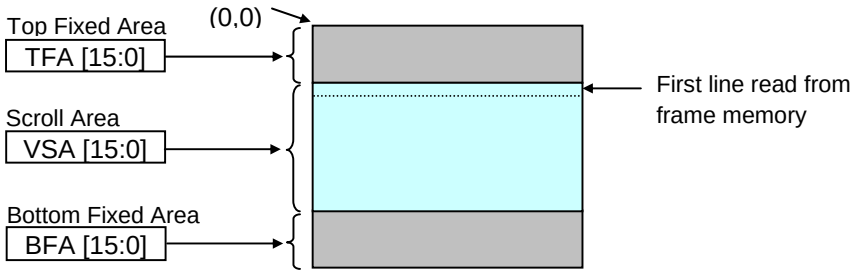
The 1st parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 2nd parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)

The first line appears immediately after the bottom most line of the Top Fixed Area.

The 3rd parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory row address.



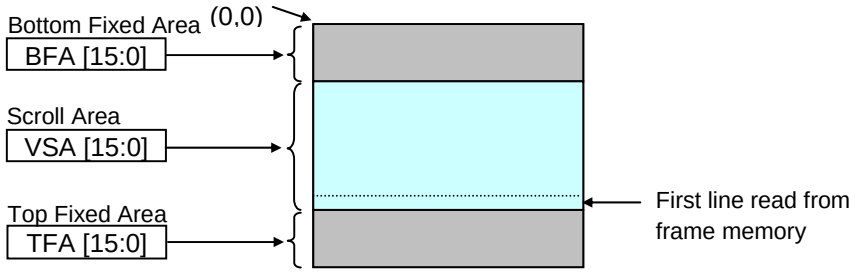
When MADCTL ML=1

The 1st parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 2nd parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)

The first line appears immediately after the top most line of the Top Fixed Area.

The 3rd parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).

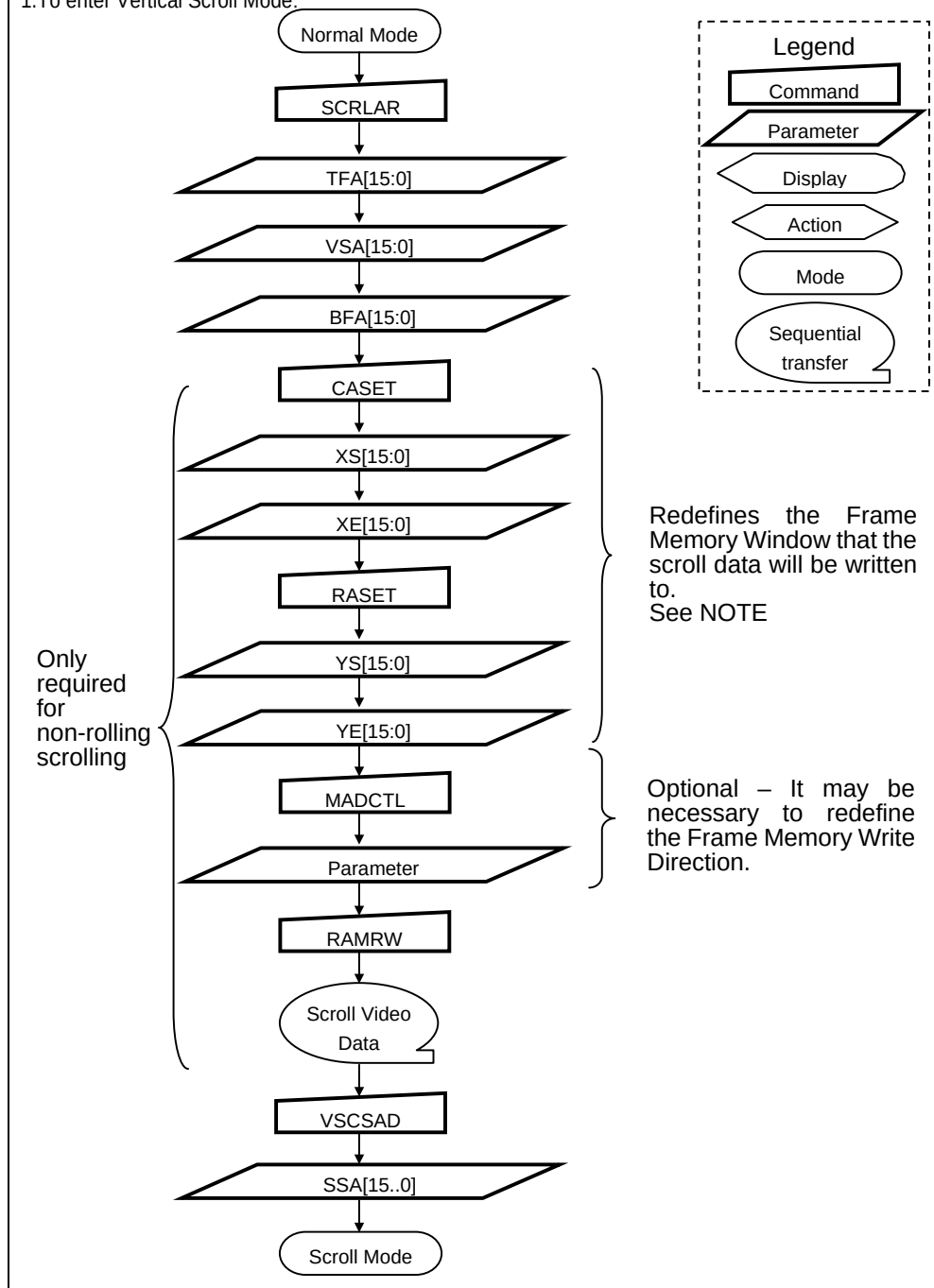


See Section 5.2.6 for details of the Memory to Display Mapping.

<table>
<tr><td>Restriction</td><td>The condition is (TFA+VSA+BFA) =208 (GM=”00”) / 220 (GM=”01”) / 240 (GM=”10”), otherwise Scrolling mode is undefined.
In Vertical Scroll Mode, MADCTL parameter MV should be set to ‘0’-this only affects the Frame Memory Write.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="5">Default Value</th></tr>
<tr><th>TFA [15:0]</th><th colspan="3">VSA [15:0]</th><th>BFA [15:0]</th></tr>
<tr><th></th><th></th><th>GM=00</th><th>GM=01</th><th>GM=10</th><th></th></tr>
<tr><td>Power On Sequence</td><td>00h</td><td>00h</td><td>00h</td><td>00h</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td><td>00h</td><td>00h</td><td>00h</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td><td>00h</td><td>00h</td><td>00h</td><td>00h</td></tr>
</table>
</td></tr>
</table>

Flow Chart

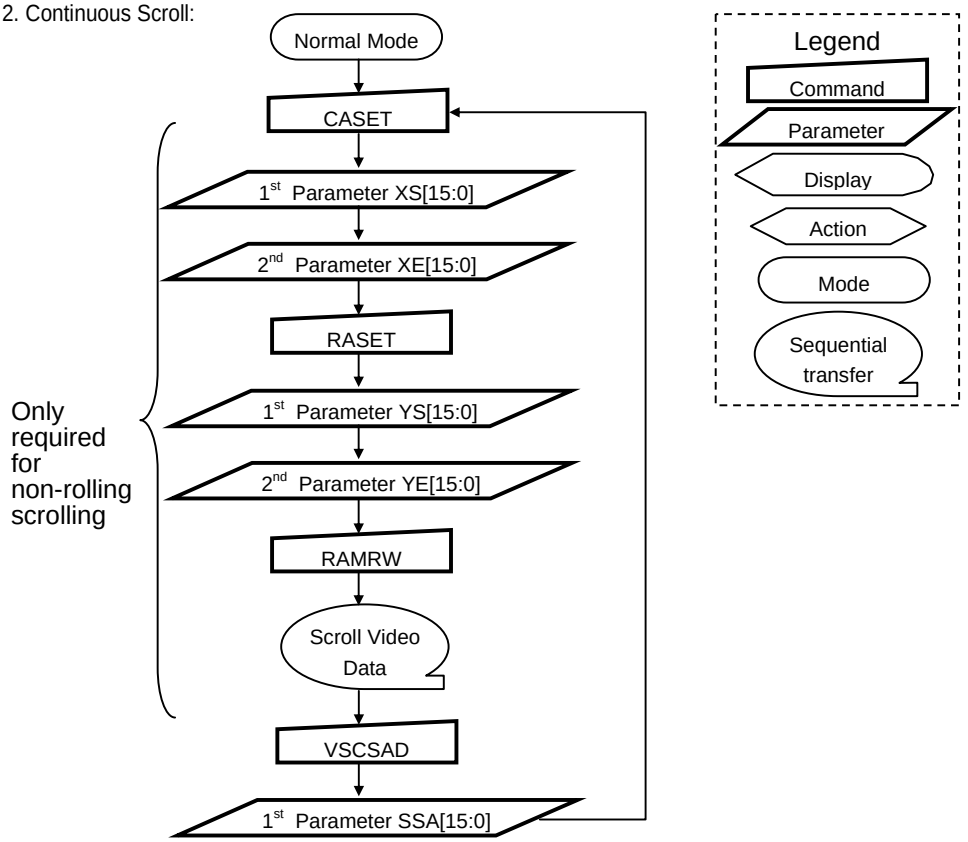
1.To enter Vertical Scroll Mode:



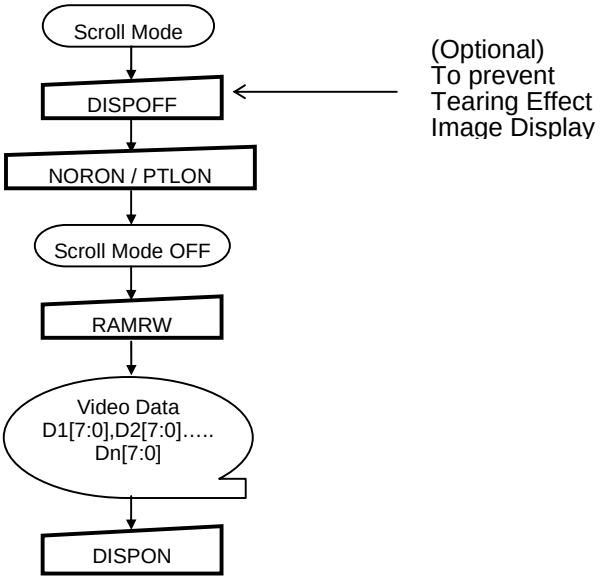
NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

Flow Chart

2. Continuous Scroll:



3. To Exit Vertical Scroll Mode:



NOTE: Scroll Mode can be exit by both the Normal Display Mode On(13h) and Partial Mode On (12h) commands.

6.1.22 TEOFF: Tearing Effect Line OFF (34h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEOFF	0	↑	1	0	0	1	1	0	1	0	0	(34h)
Parameter	No Parameter											

Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	This command has no effect when Tearing Effect output is already OFF.

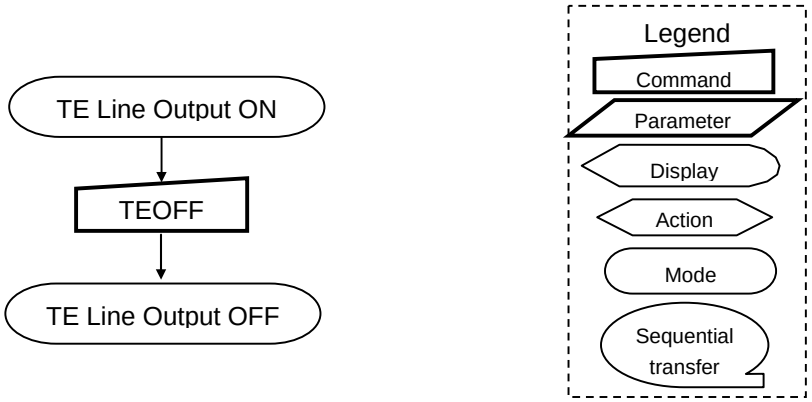
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart

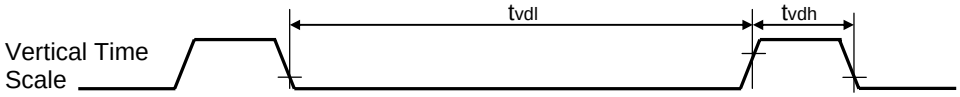


6.1.23 TEON: Tearing Effect Line ON (35h)

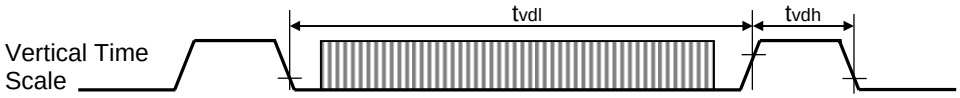
Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEON	0	↑	1	0	0	1	1	0	1	0	1	(35h)
Parameter	1	↑	1	-	-	-	-	-	-	-	M	-

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML.
The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care).
When M=0: The Tearing Effect Output line consists of V-Blanking information only.



When M=1: The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.



See Section 5.2.7 for more information.
Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already OFF.

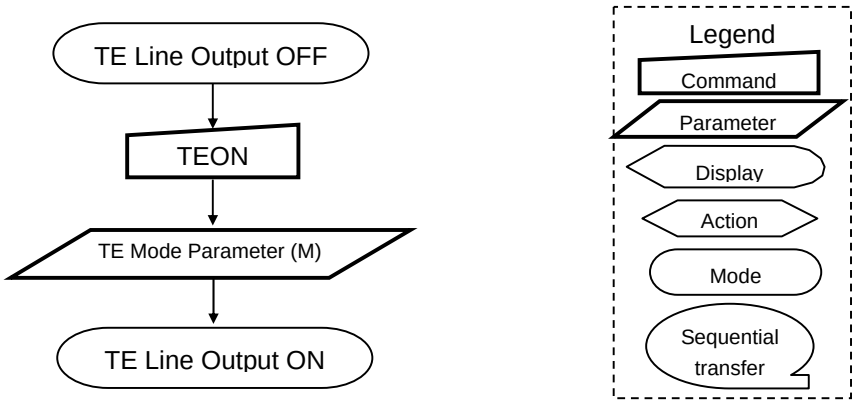
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off & M=0
S/W Reset	Tearing effect off & M=0
H/W Reset	Tearing effect off & M=0

Flow Chart



6.1.24 MADCTR: Memory Data Access Control (36h)

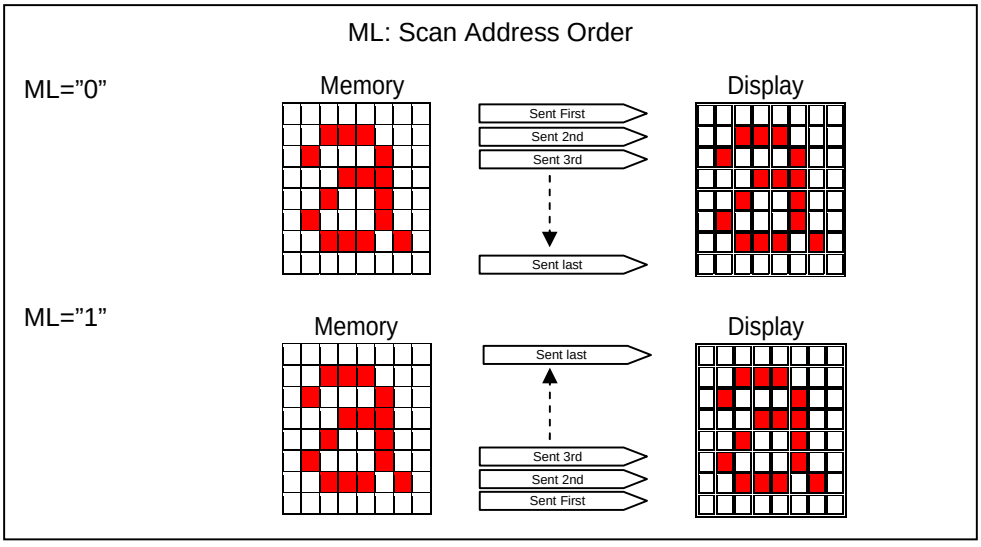
Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
MADCTR	0	↑	1	0	0	1	1	0	1	1	0	(36h)
Parameter	1	↑	1	MY	MX	MV	ML	RGB	-	-	-	-

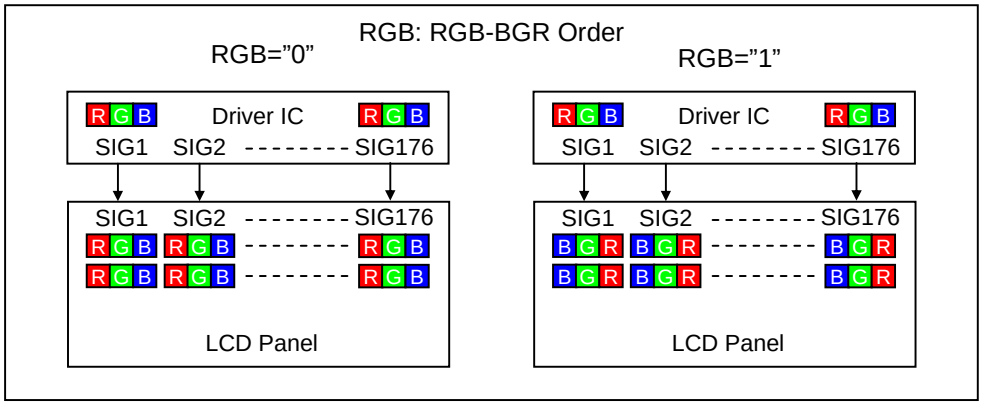
Description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

Bit Assignment

Bit	NAME	DESCRIPTION
MY	ROW ADDRESS ORDER	These 3bits controls MPU to memory write/read direction. (See Section 5.2.3)
MX	COLUMN ADDRESS ORDER	
MV	ROW/COLUMN EXCHANGE	
ML	SCAN ADDRESS ORDER	LCD refresh direction control
RGB	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)





Restriction

D2, D1 and D0 of the 1st parameter are set to '000'internally.

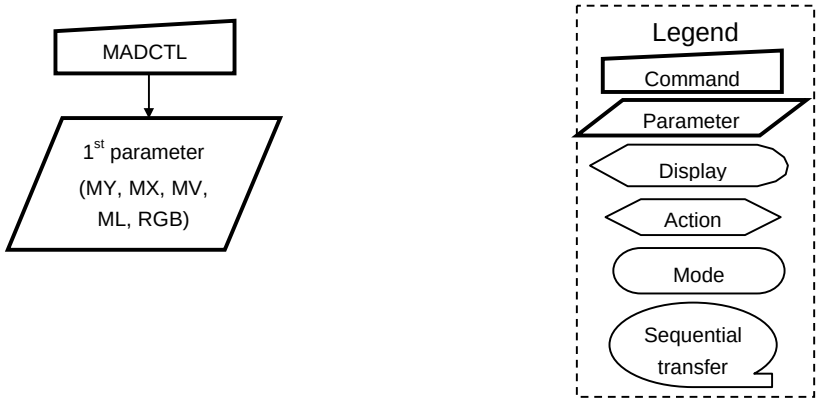
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0
S/W Reset	No Change
H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0

Flow Chart



6.1.25 VSCSAD: Vertical Scroll Start Address of RAM (37h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VSCSAD	0	↑	1	0	0	1	1	0	1	1	1	(37h)
1st parameter	1	↑	1	SSA15	SSA14	SSA13	SSA12	SSA11	SSA10	SSA9	SSA8	-
2nd parameter	1	↑	1	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	-

Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.

The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

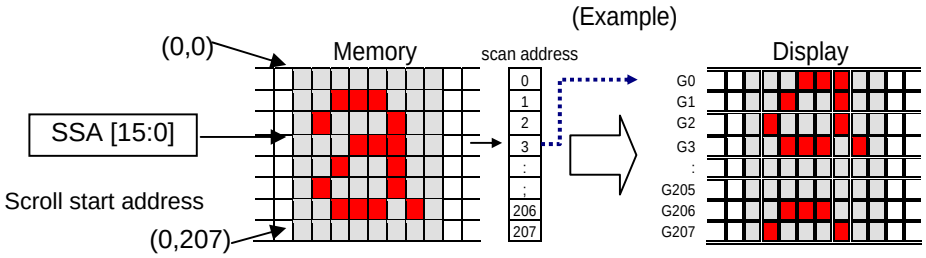
This command Start the scrolling.

Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).

When MADCTL ML=0

Example:

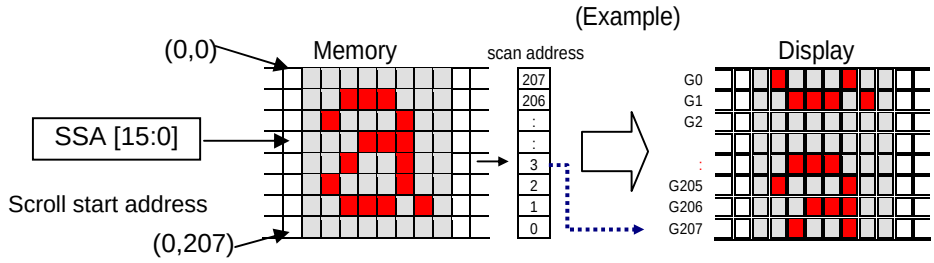
When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=208 and Vertical Scrolling Pointer SSA='3' (when GM="00").



When MADCTL ML =1

Example:

When Top Fixed Area= Bottom Fixed Area=00, Vertical Scrolling Area=208 and SSA='3' (when GM="00").



NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

SSA refers to the Frame Memory scan address.

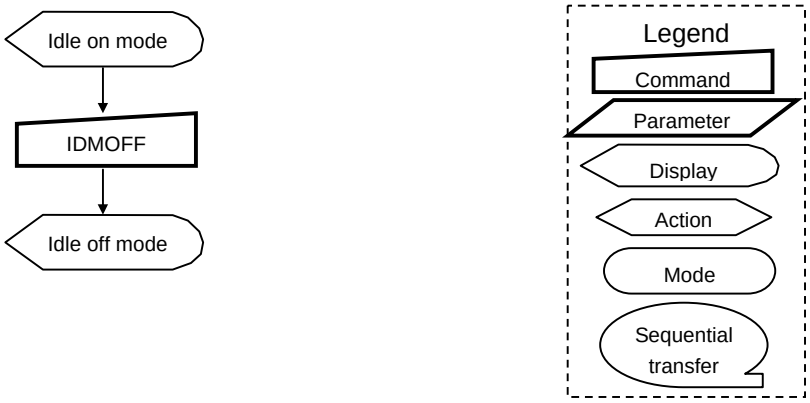
Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00</td></tr>
<tr><td>S/W Reset</td><td>00</td></tr>
<tr><td>H/W Reset</td><td>00</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

6.1.26 IDMOFF: Idle Mode Off (38h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMOFF	0	↑	1	0	0	1	1	1	0	0	0	(38h)
Parameter	No Parameter											

Description	This command is used to recover from Idle mode on. There will be no abnormal visible effect on the display mode change transition. In the idle off mode, 1. LCD can display maximum 65k-or 262k-colors. 2. Normal frame frequency is applied.
Restriction	This command has no effect when module is already in idle off mode.
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status: Default Value Power On Sequence: Idle off mode S/W Reset: Idle off mode H/W Reset: Idle off mode
Flow Chart	

6.1.27 IDMON: Idle Mode On (39h)

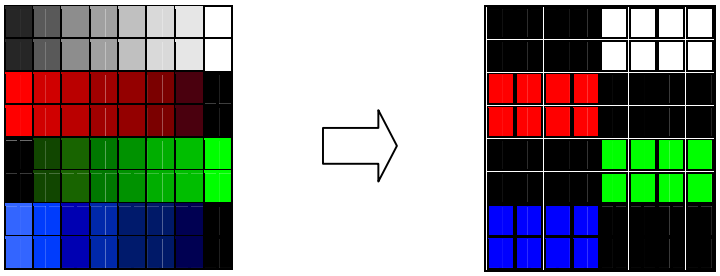
Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMON	0	↑	1	0	0	1	1	1	0	0	1	(39h)
Parameter	No Parameter											

Description

This command is used to enter into Idle mode on.
There will be no abnormal visible effect on the display mode change transition.
In the idle on mode,
1. Color expression is reduced. The primary and the secondary colors using MSB of each RMG and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)

Memory Display



"X": don't care

Color	R_5 R_4 R_3 R_2 R_1 R_0	G_5 G_4 G_3 G_2 G_1 G_0	B_5 B_4 B_3 B_4 B_1 B_0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

Restriction

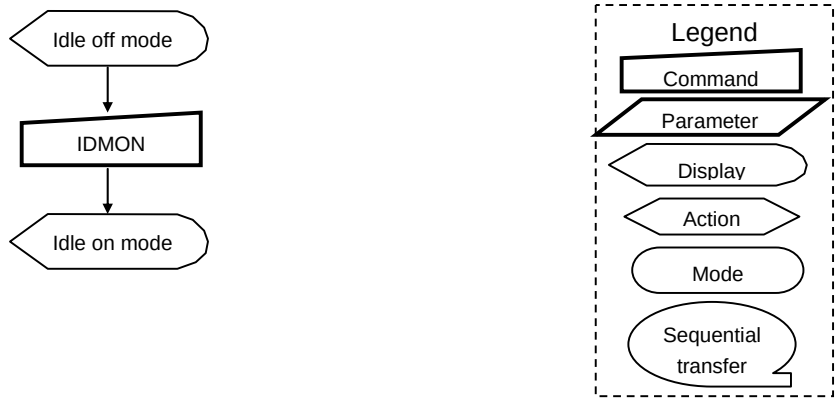
This command has no effect when module is already in idle on mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle off mode
S/W Reset	Idle off mode
H/W Reset	Idle off mode

Flow Chart	

Idle off mode
IDMON
Idle on mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.1.28 COLMOD: Interface Pixel Format (3Ah)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
COLMOD	0	↑	1	0	0	1	1	1	0	1	0	(3Ah)
Parameter	1	↑	1	-	-	-	-	-	P2	P1	P0	-

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MCU Interface. The formats are shown in the table:-

Interface Format	D2	D1	D0
Not Defined	0	0	0
Not Defined	0	0	1
8Bit/Pixel	0	1	0
12Bit/Pixel	0	1	1
Not Defined	1	0	0
16Bit/Pixel	1	0	1
18Bit/Pixel	1	1	0
Not Defined	1	1	1

NOTE: In 8 Bit/Pixel or 12 Bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory.

Restriction

There is no visible effect until the Frame Memory is written to.

Register Availability

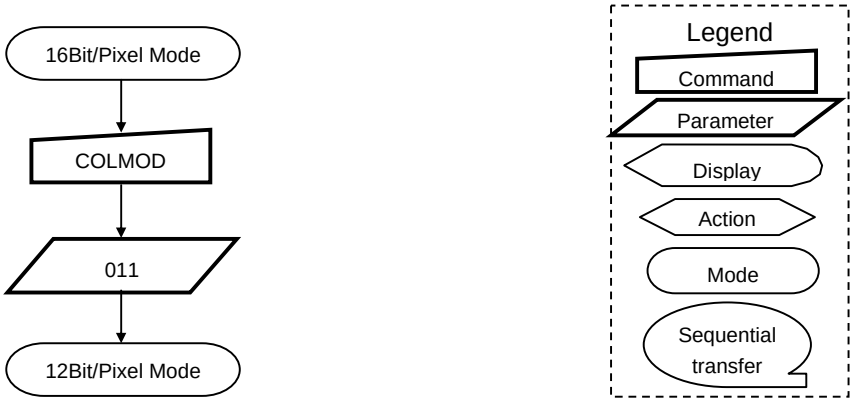
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	When CM=High	When CM=Low
Power On Sequence	18Bit/Pixel	16Bit/Pixel
S/W Reset	No Change	
H/W Reset	18Bit/Pixel	16Bit/Pixel

Flow Chart

Example:



6.1.29 RDID1: Read ID1 Value (DAh)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID1	0	↑	1	1	1	0	1	1	0	1	0	(DAh)
Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-

Description

This read byte returns 8-bit LCD module's manufacturer ID

The 1st parameter is dummy data

The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

NOTE: See command RDDID (04h), 2nd parameter.

Restriction

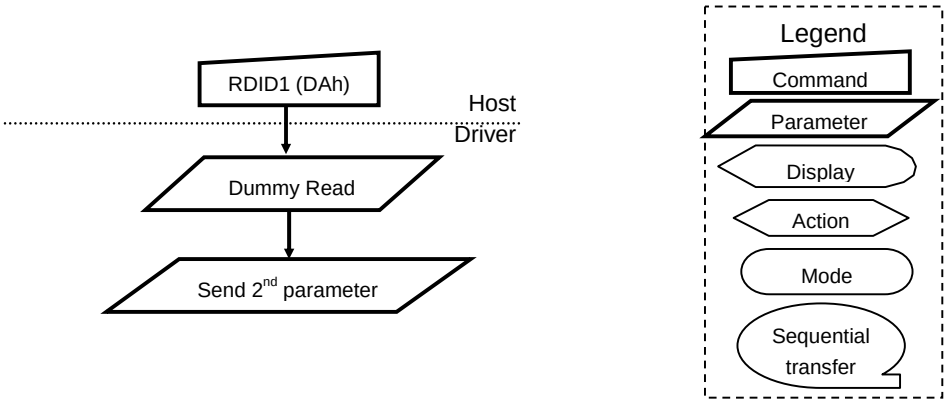
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	45h
S/W Reset	45h
H/W Reset	45h

Flow Chart



6.1.30 RDID2: Read ID2 Value (DBh)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	0	↑	1	1	1	0	1	1	0	1	1	(DBh)
Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-

Description

This read byte returns 8-bit LCD module/driver version ID
The 1st parameter is dummy data
The 2nd parameter (ID26 to ID20): LCD module/driver version ID
Parameter Range: ID=80h to FFh
NOTE: See command RDDID (04h), 3rd parameter.

Restriction

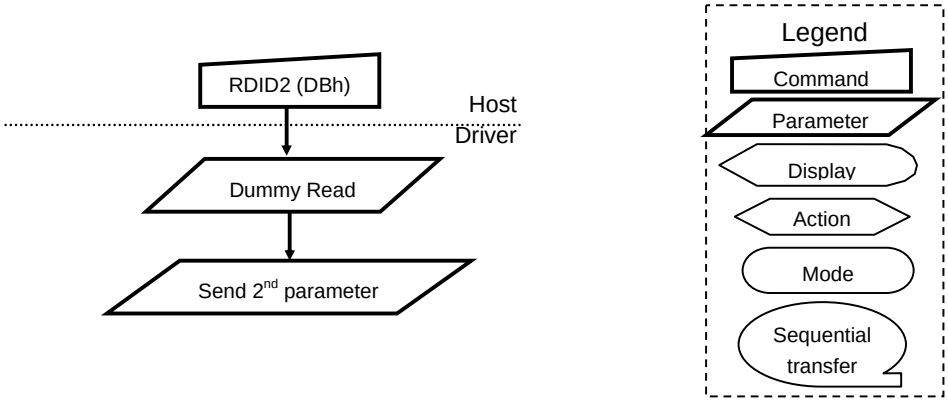
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

Flow Chart



6.1.31 RDID3: Read ID3 Value (DCh)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID3	0	↑	1	1	1	0	1	1	1	0	0	(DCh)
Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

Description

This read byte returns 8-bit LCD module/driver ID.
The 1st parameter is dummy data
The 2nd parameter (ID37 to ID30): LCD module/driver ID.
NOTE: See command RDDID (04h), 4th parameter.

Restriction

-

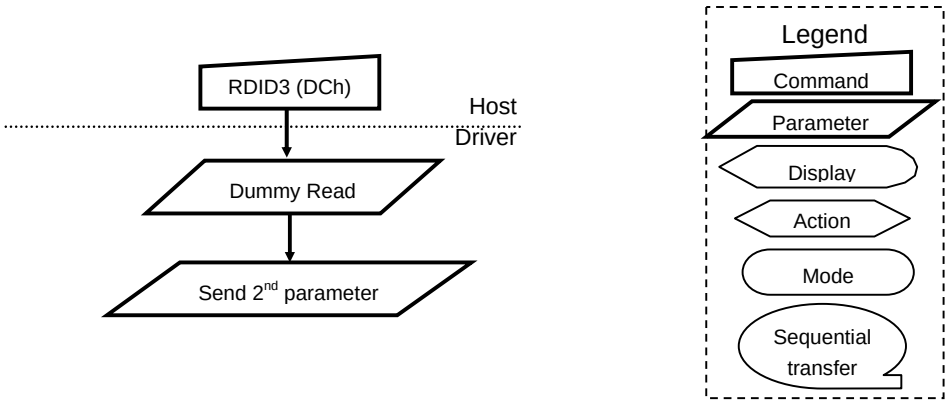
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	14h
S/W Reset	14h
H/W Reset	14h

Flow Chart



6.1.32 CLKINT: Internal Oscillator (B0h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CLKINT	0	↑	1	1	0	1	1	0	0	0	0	(B0h)
Parameter	No Parameter											

Description	Select and using internal oscillator.
Restriction	-

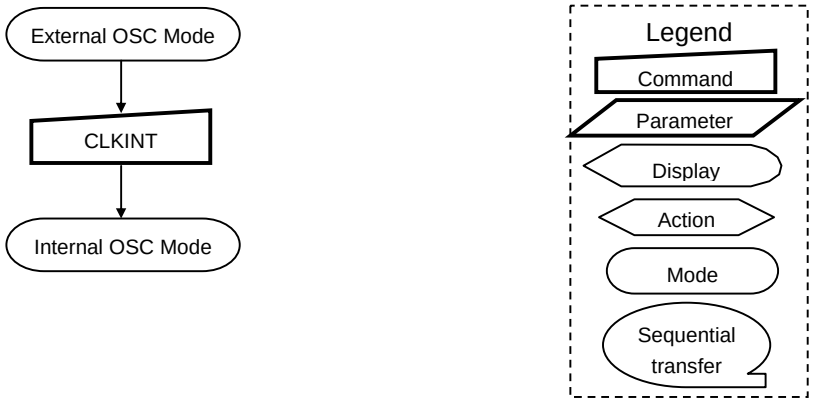
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Internal OSC mode
S/W Reset	Internal OSC mode
H/W Reset	Internal OSC mode

Flow Chart



6.1.33 CLKEXT: External Oscillator (B1h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CLKEXT	0	↑	1	1	0	1	1	0	0	0	1	(B1h)
Parameter	No Parameter											

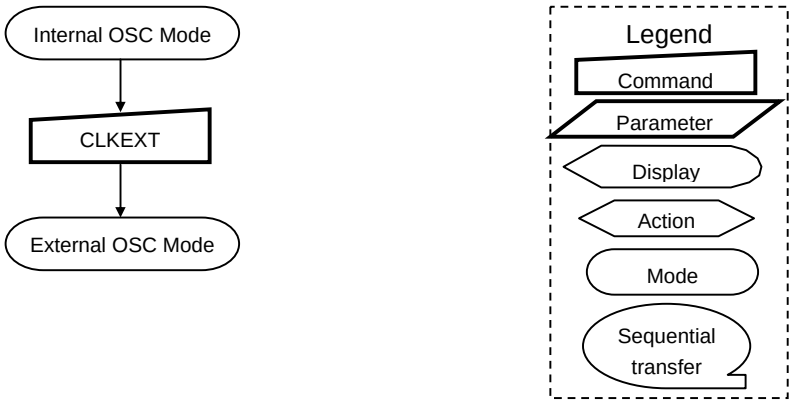
Description	Select and using external oscillator. When an external oscillator is used the external oscillator is connected to the OSC pad.
Restriction	
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Internal OSC mode
S/W Reset	Internal OSC mode
H/W Reset	Internal OSC mode

Flow Chart



6.1.34 INVCTR: Inversion Control (B2h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
INVCTR	0	↑	1	1	0	1	1	0	0	1	1	(B3h)
1st parameter	1	↑	1	DANA	TWIA	INVA	FR2A	-	NLA2	NLA1	NLA0	-
2nd parameter	1	↑	1	DANB	TWIB	INVB	FR2B	-	NLB2	NLB1	NLB0	-

Description

Display inversion mode set

1st parameter: for full colour display mode

NLA2 to NLA0: line inversion value set

DANA: “1”= Dancing scan mode on, “0”=Dancing scan mode off

TWIA: “1”= Twist mode on when dancing scan, “0”= Twist mode off

INVA: “1”= Inversion mode on when dancing scan, “0”= Inversion mode off

FR2A: “1”= 2-frame mode on when dancing scan, “0”= 2-frame mode off

2nd parameter: for 8 colour display mode

NLB2 to NLB0: line inversion value set

DANB: “1”= Dancing scan mode on, “0”=Dancing scan mode off

TWIB: “1”= Twist mode on when dancing scan, “0”= Twist mode off

INVB: “1”= Inversion mode on when dancing scan, “0”= Inversion mode off

FR2B: “1”= 2-frame mode on when dancing scan, “0”= 2-frame mode off

NLA2 (NLB2)	NLA1 (NLB1)	NLA0 (NLB0)	DANA (DANB) =1	DANA (DANB) =0
0	0	0	Frame inversion	Frame inversion
0	0	1	2-Dance mode	1-Line inversion
0	1	0	3-Dance mode	2-Line inversion
0	1	1	4-Dance mode	3-Line inversion
1	0	0	5-Dance mode	4-Line inversion
1	0	1	6-Dance mode	5-Line inversion
1	1	0	7-Dance mode	6-Line inversion
1	1	1	8-Dance mode	7-Line inversion

Restriction

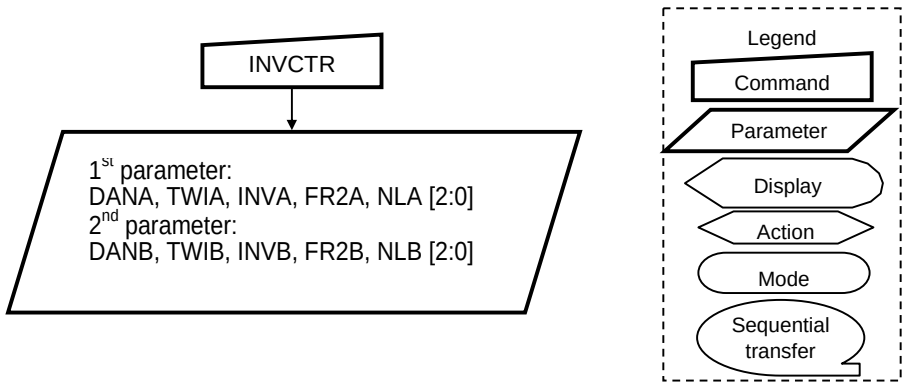
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	1st parameter	2nd parameter
Power On Sequence	01h	00h
S/W Reset	01h	00h
H/W Reset	01h	00h

Flow Chart	

INVCTR
1st parameter:
DANA, TWIA, INVA, FR2A, NLA [2:0]
2nd parameter:
DANB, TWIB, INVB, FR2B, NLB [2:0]
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.1.35 PATCTR: Partial Control (B3h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PATCTR	0	↑	1	1	0	1	1	0	0	1	1	(B3h)
1st Parameter	1	1	↑	-	-	-	-	-	PF2	PF1	PF0	-

Description

Partial display off area frame frequency control.

The 1st parameter (PF2 to PF0): frame frequency ratio between display on area and display off area.

PF2	PF1	PF0	Description
0	0	0	Partial display off frequency = display on frequency / 1
0	0	1	Partial display off frequency = display on frequency / 3
0	1	0	Partial display off frequency = display on frequency / 5
0	1	1	Partial display off frequency = display on frequency / 7
1	0	0	Partial display off frequency = display on frequency / 9
1	0	1	Partial display off frequency = display on frequency / 11
1	1	0	Partial display off frequency = display on frequency / 13
1	1	1	Partial display off frequency = display on frequency / 15

Restriction

-

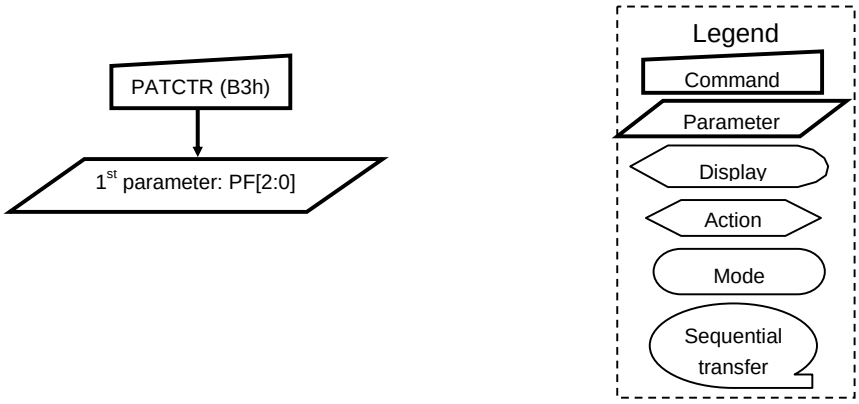
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	3
S/W Reset	3
H/W Reset	3

Flow Chart



6.1.36 GAMCTR: Set Gamma Correction Characteristics (B4h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMCTR	0	↑	1	1	0	1	1	0	1	0	0	(B4h)
1st parameter	1	↑	1	-	-	-	-	DCP3	DCP2	DCP1	DCP0	-
2nd parameter	1	↑	1	-	SP12	SP11	SP10	-	SP02	SP01	SP10	-
3rd parameter	1	↑	1	-	-	-	-	DCN4	DCN2	DCN1	DCN0	-
4th parameter	1	↑	1	-	SN12	SN11	SN10	-	SN02	SN01	SN10	-
5th parameter	1	↑	1	-	SP32	SP31	SP30	-	SP22	SP21	SP20	-
6th parameter	1	↑	1	-	SP52	SP51	SP50	-	SP42	SP41	SP40	-
7th parameter	1	↑	1	-	SP72	SP71	SP70	-	SP62	SP61	SP60	-
8th parameter	1	↑	1	-	SN32	SN31	SN30	-	SN22	SN21	SN20	-
9th parameter	1	↑	1		SN52	SN51	SN50	-	SN42	SN41	SN40	-
10th parameter	1	↑	1		SN72	SN71	SN70	-	SN62	SN61	SN60	-

Description

Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.
1st parameter: Dancing compensation on positive polarity side.
2nd parameter: Dancing compensation on negative polarity side.
3rd to 6th parameter: Gamma adjustment register on positive polarity side.
7th to 10th parameter: Gamma adjustment register on negative polarity side.

Adjustable gamma voltage is (VS/100)/step.
That is, Default+3(VS/100)V when SPx[2:0]=000 and Default-4(VS/100)V when SPx[2:0]=111 at the positive polarity.
Default-3(VS/100)V when SNx[2:0]=000 and Default+4(VS/100)V when SNx[2:0]=111 at the negative polarity.
The default value is described at the section 5.9.4.2

Note: See section 5.9.4 for details of the setting method.

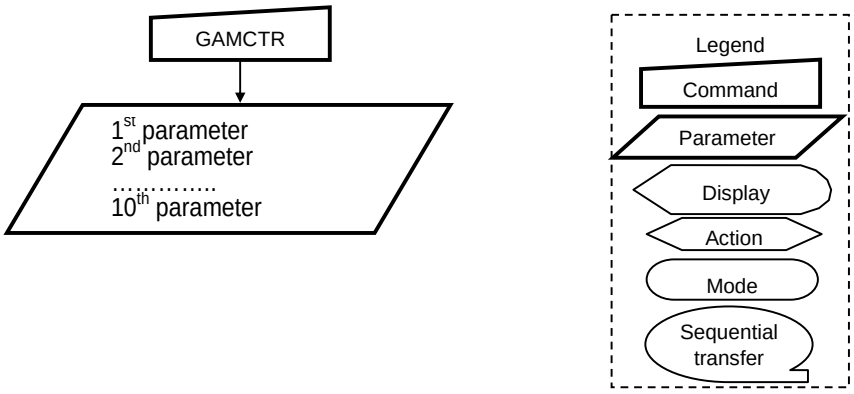
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	DCP [3:0] /DCN [3:0]	SP0 [2:0] ~ SP7 [2:0]	SN0 [2:0] ~SN7 [2:0]
Power On Sequence	00h/00h	3/3/3/3/3/3/3/3	3/3/3/3/3/3/3/3
S/W Reset	00h/00h	3/3/3/3/3/3/3/3	3/3/3/3/3/3/3/3
H/W Reset	00h/00h	3/3/3/3/3/3/3/3	3/3/3/3/3/3/3/3

Flow Chart	

GAMCTR
1st parameter
2nd parameter
……
10th parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.1.37 IFMODE: Set Display Interface Mode (B5h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IFMODE	0	↑	1	1	0	1	1	0	1	0	1	(B5h)
1st parameter	1	↑	1	-	-	-	-	-	-	IF1	IF0	-
2nd parameter	1	↑	1	-	-	DW1	DW0	DP	EP	HSP	VSP	-

Description

Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.

1st parameter: Interface mode set

IF1	IF0	Data Transfer Mode
0	0	MPU data transfer
0	1	RGB data transfer1
1	0	RGB data transfer2
1	1	RGB data transfer3

2nd parameter: RGB Interface bus width set

DW1	DW0	RGB Interface Data Width
0	0	18-bit (1-transfer for one pixel)
0	1	16-bit (1-transfer for one pixel)
1	0	6-bit (3-transfer for one pixel)
1	1	Not permitted

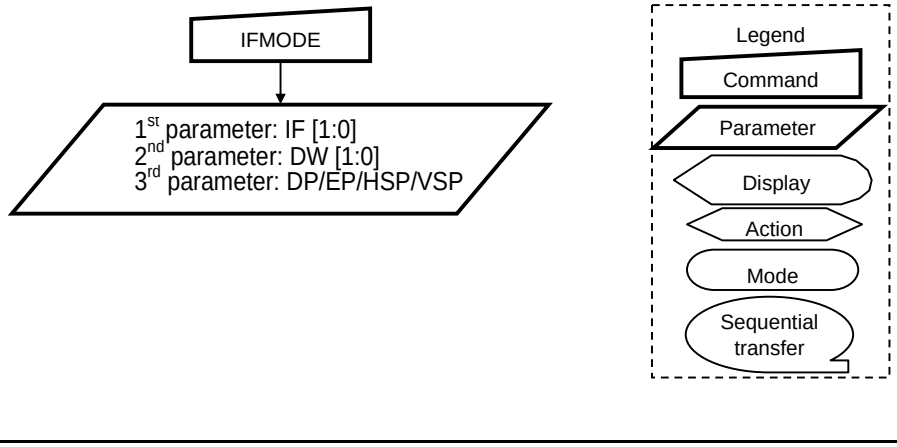
3rd parameter: Clock polarity set for RGB interface
DP: DCK polarity set ("0"=data fetched at the rising time, "1"=data fetched at the falling time)
EP: ENABLE polarity ("0"= High enable for RGB interface, "1"=Low enable for RGB interface)
HSP: HSYNC polarity ("0"=Low level sync clock, "1"=High level sync clock)
VSP: VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	IF [1:0]	DW [1:0]	DP/EP/HSP/VSP
Power On Sequence	0	0	0/0/0/0
S/W Reset	0	0	0/0/0/0
H/W Reset	0	0	0/0/0/0

Flow Chart	

IFMODE
1st parameter: IF [1:0]
2nd parameter: DW [1:0]
3rd parameter: DP/EP/HSP/VSP
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.1.38 EPWROUT: EEPROM Write Out (B6h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
EPWROUT	0	↑	1	1	0	1	1	0	1	1	0	(B6h)
Parameter	No Parameter											

Description	EEPROM write mode disable.
Restriction	It will be necessary to wait more than 100msec after EEPROM write mode start (EPWRIN).

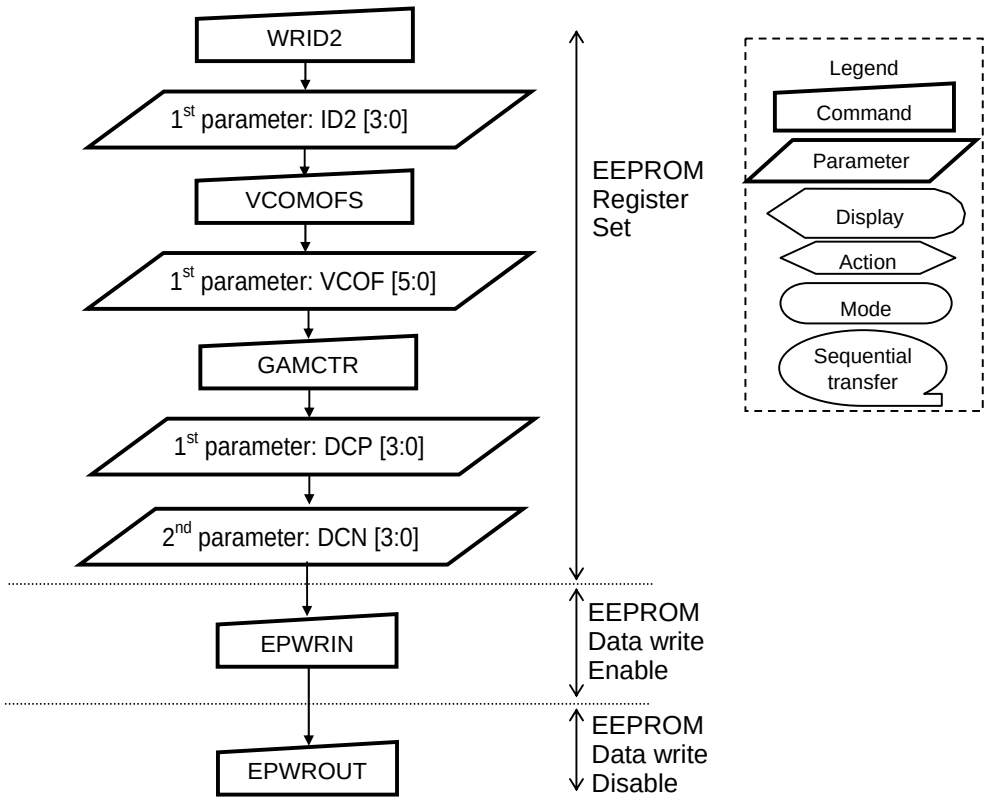
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	No
Normal Mode On, Idle Mode On, Sleep Out	No
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	EEPROM write out
S/W Reset	EEPROM write out
H/W Reset	EEPROM write out

Flow Chart



6.1.39 EPWRIN: EEPROM Write In (B7h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
EPWRIN	0	↑	1	1	0	1	1	0	1	1	1	(B7h)
Parameter	No Parameter											

Description	EEPROM write mode start.
Restriction	Before EPWRIN command, command with EEPROM parameter need to be pre-set. And it will be necessary to wait more than 1.5sec before exiting EEPROM write mode (EPWROUT).
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: No Normal Mode On, Idle Mode On, Sleep Out: No Partial Mode On, Idle Mode Off, Sleep Out: No Partial Mode On, Idle Mode On, Sleep Out: No Sleep In: **Yes**
Default	Status / Default Value Power On Sequence: Disable S/W Reset: Disable H/W Reset: Disable
Flow Chart	See the “Flow Chart” of EPWROUT command

6.1.40 DISCLK: Display Clock Set (B8h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TMPHYS	0	↑	1	1	0	1	1	1	0	0	0	(B8h)
1st parameter	1	↑	1	-	-	-	-	-	-	-	HA8	-
2nd parameter	1	↑	1	HA7	HA6	HA5	HA4	HA3	HA2	HA1	HA0	-
3rd parameter	1	↑	1	-	-	BPA5	BPA4	BPA3	BPA2	BPA11	BPA0	-
4th parameter	1	↑	1	-	-	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0	-
5th parameter	1	↑	1	-	-	-	-	-	-	-	HB8	-
6th parameter	1	↑	1	HB7	HB6	HB5	HB4	HB3	HB2	HB1	HB0	-
7th parameter	1	↑	1	-	-	BPB5	BPB4	BPB3	BPB2	BPB1	BPB0	-
8th parameter	1	↑	1	-	-	FPB5	FPB4	FPB3	FPB2	FPB1	FPB0	-

Description	Display clock condition set. 1st to 4th parameter: Display clock set for full colour display mode. HA [8:0]: Number of clocks during 1H = HA + 1 BPA [5:0]: Number of lines for vertical back porch FPA [5:0]: Number of lines for vertical front porch 5th to 8th parameter: Display clock set for 8-colour display mode. HB [8:0]: Number of clocks during 1H = HA + 1 BPB [5:0]: Number of lines for vertical back porch FPB [5:0]: Number of lines for vertical front porch By using DISCLK command, frame frequency can be set like below When Dancing mode off fFRA (Hz) = 1 / ((Number of gate + 1 dummy gate + BPA + FPA + 2) * ((HA+1) * 2usec)) for full colour display mode fFRB (Hz) = 1 / ((Number of gate + 1 dummy gate + BPB + FPB + 2) * ((HB+1) * 2usec)) for 8-colour display mode When Dancing mode on fFRA (Hz) = 1 / ((Number of gate + 1 dummy gate + BPA + FPA + 2 + 16) * ((HA+1) * 2usec)) for full colour display mode fFRB (Hz) = 1 / ((Number of gate + 1 dummy gate + BPB + FPB + 2 + 16) * ((HB+1) * 2usec)) for 8-colour display mode BPA (BPB) and FPA (FPB) are related to the vertical mode TE signal pulse width. TE (vertical mode, high pulse width) = (BFA + FPA + 2) * ((HA+1) * 2usec) for full colour display mode TE (vertical mode, high pulse width) = (BFB + FPB + 2) * ((HB+1) * 2usec) for 8-colour display mode
Restriction	-

Register Availability

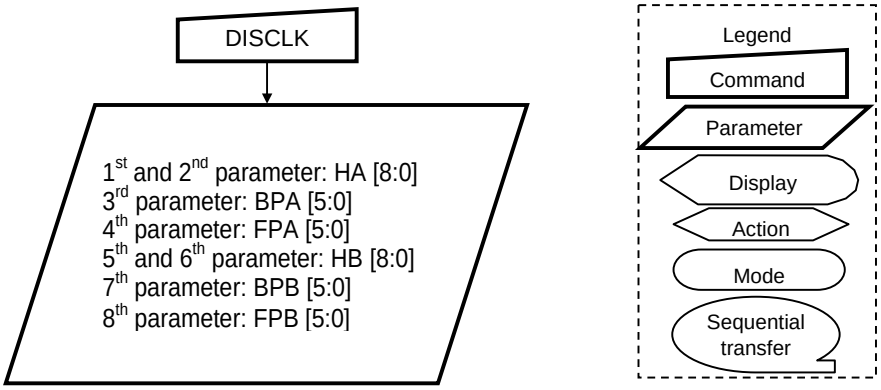
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	HA [8:0]	BPA [5:0]	FPA [5:0]	HB [8:0]	BPB [5:0]	FPB [5:0]
Power On Sequence	38	8	4	44	8	4
S/W Reset	38	8	4	44	8	4
H/W Reset	38	8	4	44	8	4

The default frame frequency (normal mode, 208 gate + 1 dummy gate)
= 1/((209+8+4+2)*(38+1)*2usec) = 57.5Hz
The default frame frequency (idle mode, 208 gate + 1 dummy gate)
= 1/((209+8+4+2)*(44+1)*2usec) = 49.8Hz
Vertical TE signal high pulse width
= (8+4+2)*(38+1)*2usec = 1092 usec

Flow Chart



6.1.41 WRID2: Write ID2 Value (D9h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	0	↑	1	1	1	0	1	1	0	0	1	(D9h)
Dummy read	1	1	↑	-	-	-	-	-	-	-	-	-
2nd Parameter	1	1	↑	-	-	-	-	ID23	ID22	ID21	ID20	-

Description

Write 4-bit LCD module/driver version ID to save it to EEPROM.
The 1st parameter (ID23 to ID20): LCD module/driver version ID

Restriction

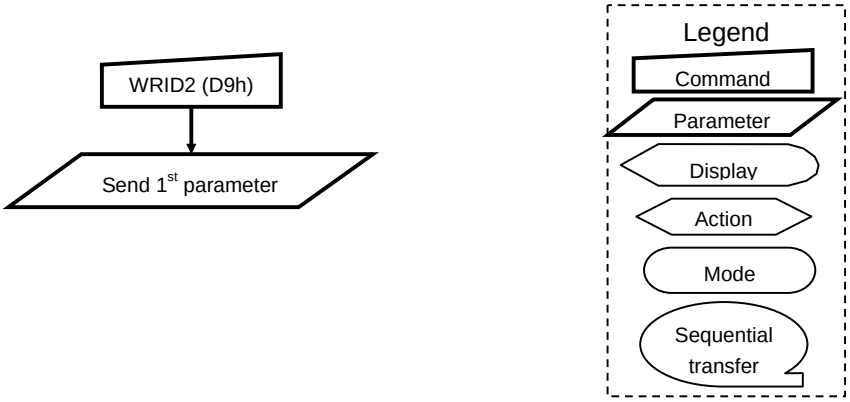
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Not Fixed
S/W Reset	Not Fixed
H/W Reset	Not Fixed

Flow Chart



6.1.42 VCOMOFS: VCOM Offset Control (B9h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VCOMOFS	0	↑	1	1	0	1	1	1	0	0	1	(B9h)
1st parameter	1	↑	1	-	-	VCOF5	VCOF4	VCOF3	VCOF2	VCOF1	VCOF0	-

Description

VCOM Offset Control

The 1st parameter: VCOM offset control

VCOF [5:0]	VCLC (Internal)	VCHC (Internal)
0	VCLC	VCHC
1	VCLC-31	VCHC-31
:	:	:
31	VCLC-1	VCHC-1
32 (default)	VCLC	VCHC
33	VCLC+1	VCHC+1
:	:	:
63	VCLC+31	VCHC+31

NOTE: If VCLC (Internal) or VCHC (Internal) is less than 0, it becomes 0.

If VCLC (Internal) or VCHC (Internal) is larger than 63, it becomes 63.

VCOF[5:0] are stored in EEPROM to fit contrast.

If RAPP bit of REGAPP command is "0", the VCOF value stored in EEPROM will be applied to calculate internal VCLC and VCHC data. Just when RAPP bit of REGAPP command is "1", the VCOFS value in the VCOF[5:0] register are applied directly to calculate internal VCLC and VCHC data.

Restriction

To control VCOM voltage with VCOMOFS command, RAPP parameter in REGAPP command should be set to "1".

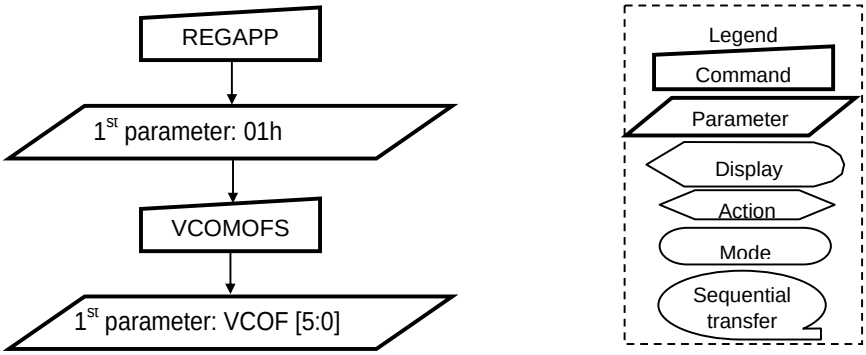
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (VCOF [5:0])
Power On Sequence	0
S/W Reset	0
H/W Reset	0

Flow Chart



6.1.43 VCOMCTR: VCOML / VCOMH Voltage Control (BAh)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VCOMCTR	0	↑	1	1	0	1	1	1	0	1	0	(BAh)
1st parameter	1	↑	1	-	-	VCLC5	VCLC4	VCLC3	VCLC2	VCLC1	VCLC0	-
2nd parameter	1	↑	1	-	-	VCHC5	VCHC4	VCHC3	VCHC2	VCHC1	VCHC0	-

Description

VCOML / VCOMH Voltage Control

The 1st parameter: VCOML voltage control (See below table)

The 2nd parameter: VCOMH voltage control (See below table)

VCLC [5:0]	VCOML output voltage	VCHC [5:0]	VCOMH output voltage
0	VCOML = -2.00 V	0	VCOMH = +2.50 V
1	VCOML = -1.95 V	1	VCOMH = +2.55 V
2	VCOML = -1.90 V	2	VCOMH = +2.60 V
:	:	:	:
60	VCOML = +1.00V	60	VCOMH = +5.50V
61 ~ 63	Not permitted	61 ~ 63	Not permitted

Restriction

VCOMH will be fixed to the trimmed value during wafer test. So, to control VCOMH with VCOMCTR command you should use some special test command (REGAPP1: F2h) with parameter 21h.

Register Availability

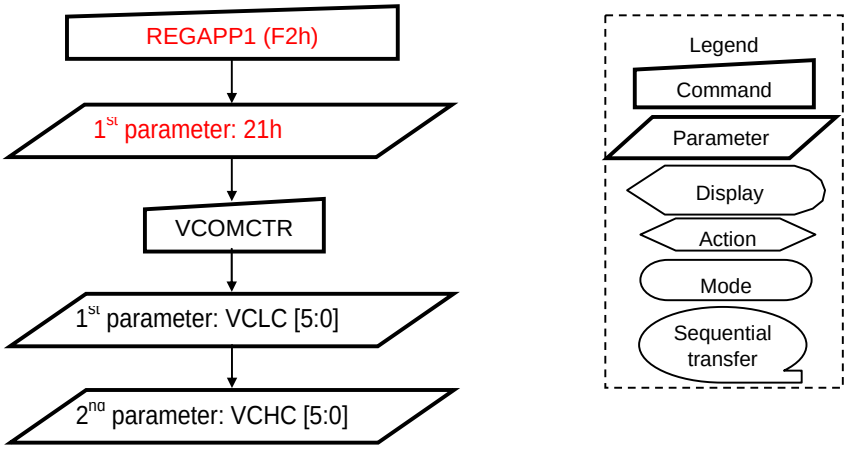
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VCLC [5:0]	VCHC [5:0]
Power On Sequence	32	*
S/W Reset	32	*
H/W Reset	32	*

NOTE: After Wafer level test, the default value of VCHC will be trimmed to fit the target VCOM amplitude.

Flow Chart



6.1.44 PWRCTR: Booster On/Off Control (BBh) (Just for TEST)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWRCTR	0	↑	1	1	0	1	1	1	0	1	1	(BBh)
1st parameter	1	↑	1	VCREG	VCL	VGHL	VG	VS	VR	AVD	OSC	-

Description

Booster on/off control
The 1st parameter: Booster / regulator on/off
OSC: Oscillator on/off control (“1”=ON, “0”=OFF)
AVD: AVDD booster on/off control (“1”=ON, “0”=OFF)
VR: VR regulator on/off control (“1”=ON, “0”=OFF)
VS: VS regulator on/off control (“1”=ON, “0”=OFF)
VG: VG regulator on/off control (“1”=ON, “0”=OFF)
VGHL: VGH/VGL1/VGL2 booster on/off control (“1”=ON, “0”=OFF)
VCL: VCL booster on/off control (“1”=ON, “0”=OFF)
VCREG: VCOMH/VCOML regulator on/off control (“1”=ON, “0”=OFF)

Restriction

This command should be used for TEST purpose only.
When using this command there can be an unexpected high current consumption.

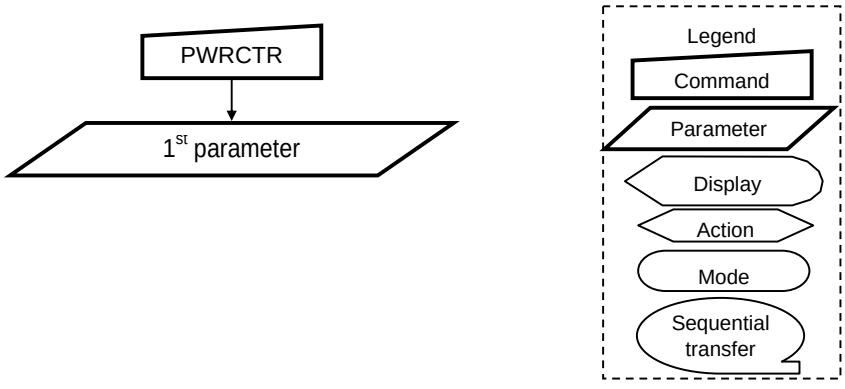
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All off
S/W Reset	All off
H/W Reset	All off

Flow Chart



6.1.45 OUTCTR: Output On/Off Control (BCh) (Just for TEST)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OUTCTR	0	↑	1	1	0	1	1	1	1	0	0	(BCh)
1st parameter	1	↑	1	-	-	-	-	-	VCOM	GATE	SRC	-

Description

Output on/off control

The 1st parameter: Output on/off

VCOM: VCOM output on/off control (“1”=ON, “0”=OFF)

GATE: Gate output on/off control (“1”=ON, “0”=OFF)

SRC: Source output on/off control (“1”=ON, “0”=OFF)

Restriction

This command should be used for TEST purpose only.

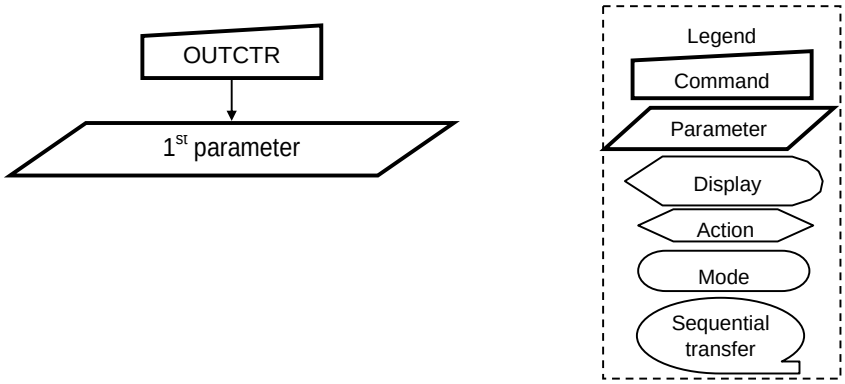
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All off
S/W Reset	All off
H/W Reset	All off

Flow Chart



6.1.46 REGCTR: Regulator Control (BDh)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VTGCTR	0	↑	1	1	0	1	1	1	1	0	1	(BDh)
1st parameter	1	↑	1	-	VRS2	VRS1	VRS0	-	VSG2	VSG1	VSG0	-

Description

Regulator voltage control

The 1st parameter:

VRS [2:0]: VR regulator output control

VSG [2:0]: VS and VG regulator output control

VRS [2:0]	VR output	VSG [2:0]	VS/VG output
0	VR = 3.00V	0	VS = VG = 3.00V
1	VR = 3.50V	1	VS = VG = 3.50V
2	VR = 3.75V	2	VS = VG = 3.75V
3	VR = 4.00V	3	VS = VG = 4.00V
4	VR = 4.25V	4	VS = VG = 4.25V
5	VR = 4.50V	5	VS = VG = 4.50V
6	VR = 4.75V	6	VS = VG = 4.75V
7	VR = 5.00V	7	VS = VG = 5.00V

Restriction

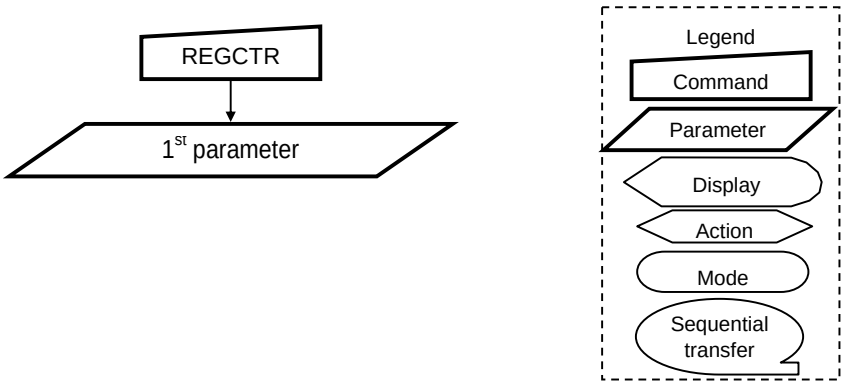
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VRS [2:0]	VSG [2:0]
Power On Sequence	2	4
S/W Reset	2	4
H/W Reset	2	4

Flow Chart



6.1.47 AMPCTR: OP-Amp Current Control (BEh)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
AMPCTR	0	↑	1	1	0	1	1	1	1	1	0	(BEh)
1st parameter	1	↑	1	-	-	-	-	-	-	-	-	-
2nd parameter	1	↑	1	-	-	-	-	SACS3	SACS2	SACS1	SACS0	-
3rd parameter	1	↑	1	-	-	-	-	GACS3	GACS2	GACS1	GACS0	-

Description

OP-amp current control

The 1st parameter:

Dummy parameter.

The 2nd to 3rd parameter:

SACS [3:0]: Source amp current control ("15": Minimum < "8" < "4" < "2" < "1":Maximum)

GACS [3:0]: Gamma amp current control ("1": Minimum < "2" < "4" < "8":Maximum)

Restriction

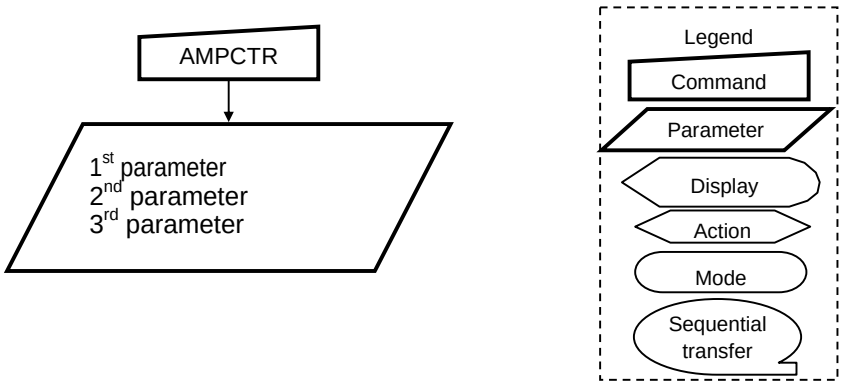
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	SACS [3:0]	GACS [3:0]
Power On Sequence	0Fh	01h
S/W Reset	0Fh	01h
H/W Reset	0Fh	01h

Flow Chart



6.1.48 BSTCLK: Booster Clock Control (BFh)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
BSTCLK	0	↑	1	1	0	1	1	1	1	1	1	(BFh)
1st parameter	1	↑	1	-	-	-	-	FGA3	FGA2	FGA1	FGA0	-
2nd parameter	1	↑	1	-	-	-	-	FCA3	FCA2	FCA1	FCA0	-
3rd parameter	1	↑	1	-	-	-	-	FAA3-	FAA3	FAA3	FAA3	-
4th parameter	1	↑	1	-	-	-	-	FGB3	FGB2	FGB1	FGB0	
5th parameter	1	↑	1	-	-	-	-	FCB3	FCB2	FCB1	FCB0	
6th parameter	1	↑	1	-	-	-	-	FAB3-	FAB3	FAB3	FAB3	
7th parameter	1	↑	1	-	-	-	-	-	-	VMS	VCD	

Description

Booster frequency and boosting ratio control

The 1st to 3rd parameter: Booster clock for full colour mode

FGA [3:0]: VGH/VGL1/VGL2 booster clock frequency select

FCA [3:0]: VCL booster clock frequency select

FAA [3:0]: AVDD booster clock frequency select

The 4th to 6th parameter: Booster clock for 8-colour mode

FGB [3:0]: VGH/VGL1/VGL2 booster clock frequency select

FCB [3:0]: VCL booster clock frequency select

FAB [3:0]: AVDD booster clock frequency select

FGA [3:0], FCA [3:0], FAA [3:0], FGB [3:0], FCB [3:0], FAB [3:0],	Booster clock frequency	FGA [3:0], FCA [3:0], FAA [3:0], FGB [3:0], FCB [3:0], FAB [3:0],	Booster clock frequency
0	1 kHz	8	16 kHz
1	2 kHz	9	18 kHz
2	4 kHz	10	21 kHz
3	6 kHz	11	25 kHz
4	8 kHz	12	31 kHz
5	10 kHz	13	36 kHz
6	12 kHz	14	42 kHz
7	14 kHz	15	50 kHz

The 7th parameter:

VMS: Boosting method select for booster1 (AVDD) (“0”: single mode, “1”: dual mode)

VCD: Boosting ratio select for booster1 (AVDD) (“0”: AVDD=2*VR, “1”: AVDD=3*VR)

Restriction

During power initialization, AVDD will start boosting by using single mode and then return to the register setting mode (VMS)

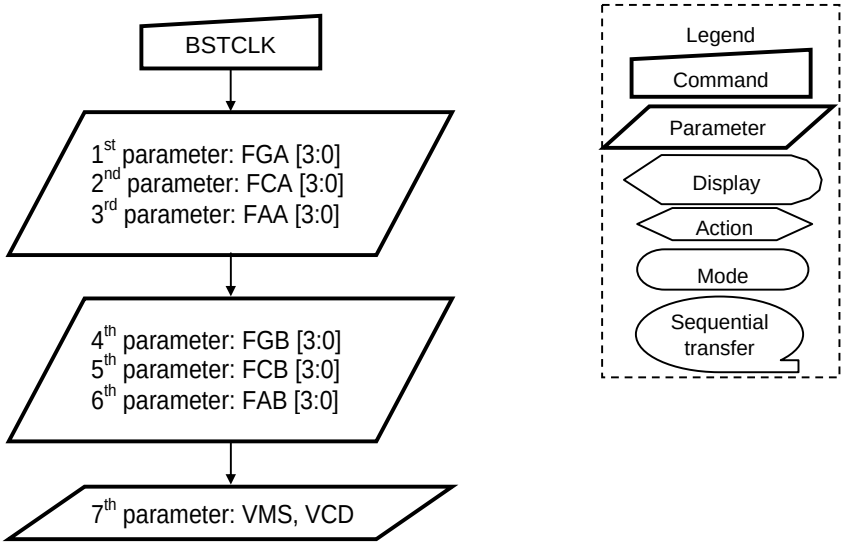
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value							
	FGA [3:0]	FCA [3:0]	FAA [3:0]	FGB [3:0]	FCB [3:0]	FAB [3:0]	VMS	VCD
Power On Sequence	2	2	4	2	2	4	1	0
S/W Reset	2	2	4	2	2	4	1	0
H/W Reset	2	2	4	2	2	4	1	0

Flow Chart



6.1.49 VGLCTR: Gate Low Voltage Control (C0h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GOPSEL	0	↑	1	1	1	0	0	0	0	0	0	(C0h)
1st parameter	1	↑	1	-	-	-	-	-	-	VGLC1	VGLC0	-

Description

Gate Low voltage level select
The 1st parameter: VGLC [1:0]
"00": Option1, Gate low level = VGL2
"01": Option2, Enable the VGLDC output and VGLI input
"10": Option3, Enable the VGLAC output and VGLI input
"11": Option4, Gate low level = VGL1

Restriction

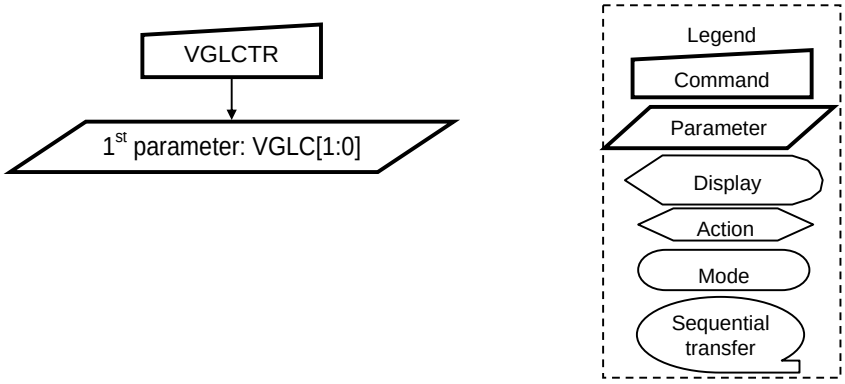
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	VGLC [1:0]
Power On Sequence	0
S/W Reset	0
H/W Reset	0

Flow Chart



6.1.50 SGTCTR: Source/Gate On/Off Time Control (C1h)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SGTCTR	0	↑	1	1	1	0	0	0	0	0	1	(C1h)
1st parameter	1	↑	1	0	0	0	0	0	0	0	0	-
2nd parameter	1	↑	1	0	0	0	0	0	0	0	0	-
3rd parameter	1	↑	1	GON7	GON6	GON5	GON4	GON3	GON2	GON1	GON0	-
4th parameter	1	↑	1	GOF7	GOF6	GOF5	GOF4	GOF3	GOF2	GOF1	GOF0	-

Description

Display timing control
The 1st parameter: SZS [7:0]= 0 (do not use any other value)
The 2nd parameter: SZE [7:0]= 0 (do not use any other value)
The 3rd parameter: GON [7:0]= Gate signal select timing
The 4th parameter: GOF [7:0]= Gate signal non-select timing

Restriction

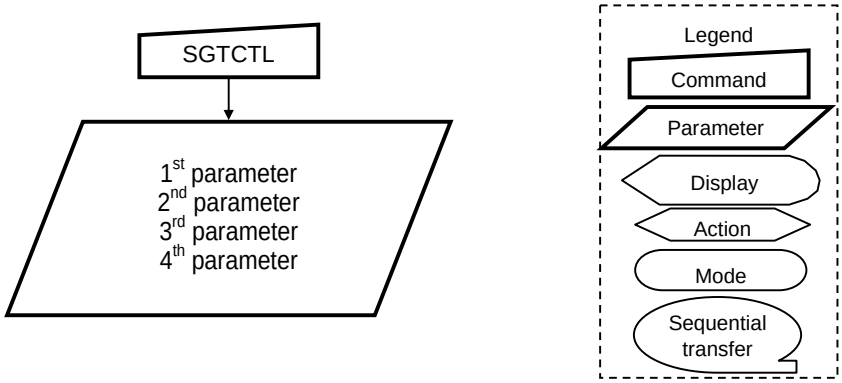
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	SZS [7:0]	SZE [7:0]	GON [7:0]	GOF [7:0]
Power On Sequence	0	0	05h	FCh
S/W Reset	0	0	05h	FCh
H/W Reset	0	0	05h	FCh

Flow Chart



6.1.51 IFMPU: Set MPU Interface Mode (C2h) (Just for TEST)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IFMPU	0	↑	1	1	1	0	0	0	0	1	0	(C2h)
1st parameter	1	↑	1	-	-	-	-	-	PP68	PBS1	PBS0	-

Description

Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.

1st parameter: MPU Interface mode set

PP68	PBS1	PBS0	MPU Interface Mode
0	0	0	3-Pin serial interface
0	0	1	8080-series 8-bit parallel interface
0	1	0	8080-series 16-bit parallel interface
0	1	1	8080-series 18-bit parallel interface
1	0	0	4-Pin serial interface
1	0	1	6800-series 8-bit parallel interface
1	1	0	6800-series 16-bit parallel interface
1	1	1	6800-series 18-bit parallel interface

Restriction

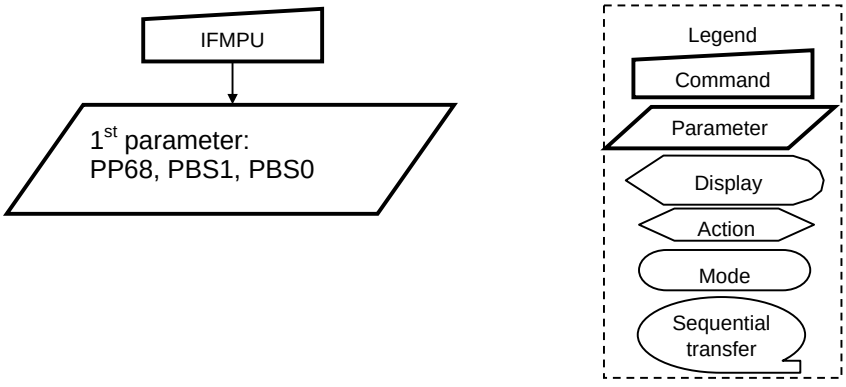
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

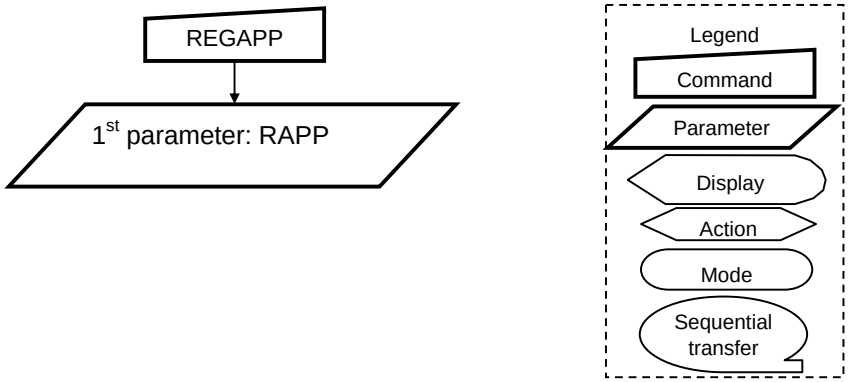
Status	Default Value
	PP68, PBS1, PBS0
Power On Sequence	Same as P68, BS1 and BS0 pin connection
S/W Reset	No change
H/W Reset	Same as P68, BS1 and BS0 pin connection

Flow Chart



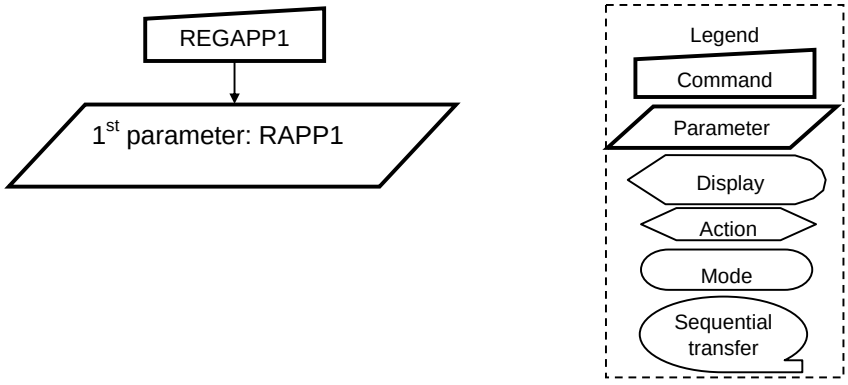
6.1.52 REGAPP: Set Register Value Direct Apply (F8h) (Just for TEST)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
REGAPP	0	↑	1	1	1	1	1	1	0	0	0	(F8h)
1st parameter	1	↑	1	-	-	-	-	-	-	-	RAPP	-

Description	Set VCOF[5:0], VAP1[3:0], VAN1[3:0] value direct apply to internal circuit. RAPP="0": The programmed value in EEPROM are used as VCOF[5:0], DCP[3:0] and DCN[3:0]. RAPP="1": The parameter value by using VCOMOFS and GAMCTR command are directly used as internal VCOF[5:0], DCP[3:0] and DCN[3:0].
Restriction	Use this command just to fit the display characteristic before EEPROM programming.
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value Power On Sequence: 0 S/W Reset: 0 H/W Reset: 0
Flow Chart	

6.1.53 REGAPP1: Set Register Value Direct Apply for VCOMH (F2h) (Just for TEST)

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
REGAPP	0	↑	1	1	1	1	1	0	0	1	0	(F2h)
1st parameter	1	↑	1	0	0	1	0	0	0	0	RAPP1	-

Description	Set VCHC [5:0] value direct apply to internal circuit. RAPP1="0": The trimmed values are used as VCHC [5:0]. RAPP1="1": The parameter value by using VCOMCTR command are directly used as internal VCHC [5:0].
Restriction	Use this command just for TEST.
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value Power On Sequence: 0 S/W Reset: 0 H/W Reset: 0
Flow Chart	

6.1.54 TEST1: Test Command1 (E-h)

This instruction is a testing instruction code for Leadis. Please do not use it.

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST1	0	↑	1	1	1	1	0	-	-	-	-	(E-h)

6.1.55 TEST2: Test Command2 (F-h)

This instruction is a testing instruction code for Leadis. Please do not use it.

Inst / Para	D/!C	!WR	!RD	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST2	0	↑	1	1	1	1	1	-	-	-	-	(F-h)

6.2 RESET TABLE (DEFAULT VALUE)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display On/Off	Off	Off	Off
Column: Start Address (XS)	00h	00h	00h
Column: End Address (XE)	AFh	AFh	AFh
Row: Start Address (YS)	00h	00h	00h
*1) Row: End Address (YE)	CFh / DBh / EFh	CFh / DBh / EFh	CFh / DBh / EFh
RGB for 4k and 256 Color Mode (R/G/B)	Random	See Section 5.2.8	No Change
Gamma setting	GC0	GC0	GC0
Partial: Start Address (PSL)	00h	00h	00h
*2) Partial: End Address (PEL)	CFh / DBh / EFh	CFh / DBh / EFh	CFh / DBh / EFh
Scroll: Top Fixed Area (TFA)	00h	00h	00h
*3) Scroll: Scroll Area (VSA)	00h	00h	00h
Scroll: Bottom Fixed Area (BFA)	00h	00h	00h
Scroll Start Address (SSA)	00h	00h	00h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Idle Mode On/Off	Off	Off	Off
Interface Pixel Color Format (When CM=High)	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
Interface Pixel Color Format (When CM=Low)	5 (16-Bit/Pixel)	5 (16-Bit/Pixel)	No Change
ID1	45h	45h	45h
ID2	Not Fixed	Not Fixed	Not Fixed
ID3	14h	14h	14h

*Note: *1), *2), *3) The default value is different according to the GM1 and GM0 pad connection.*
(GM[1:0]="00"/"01"/"10")

6.3 INSTRUCTION SETUP FLOW

6.3.1 Initializing with the Built-in Power Supply Circuits

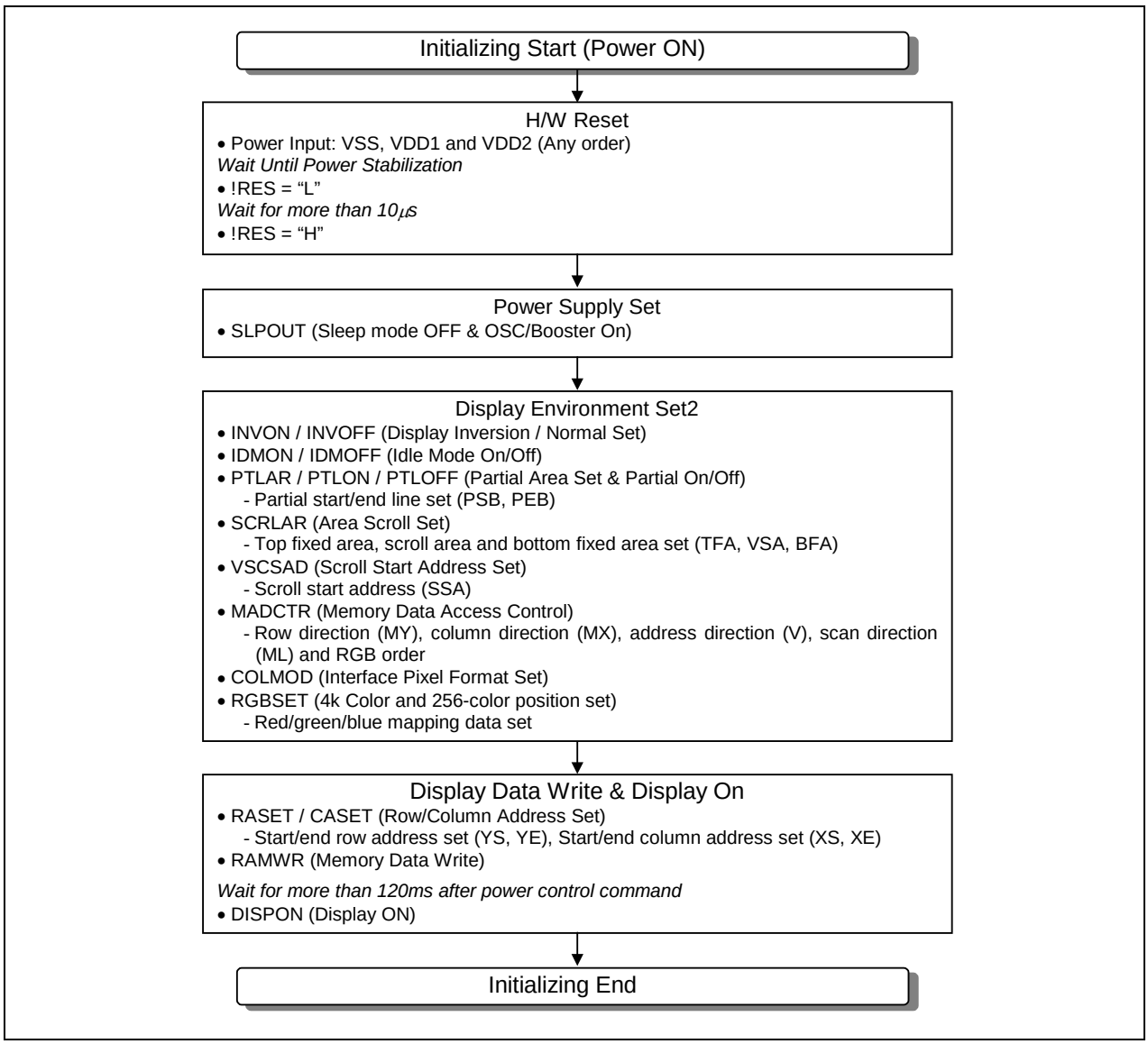


Fig. 6.3.1 Initializing with the built-in power supply circuits

The initializing sequence does not have any effect on the display. The display is in its normal background color during the initialization.

6.3.2 Power OFF Sequence

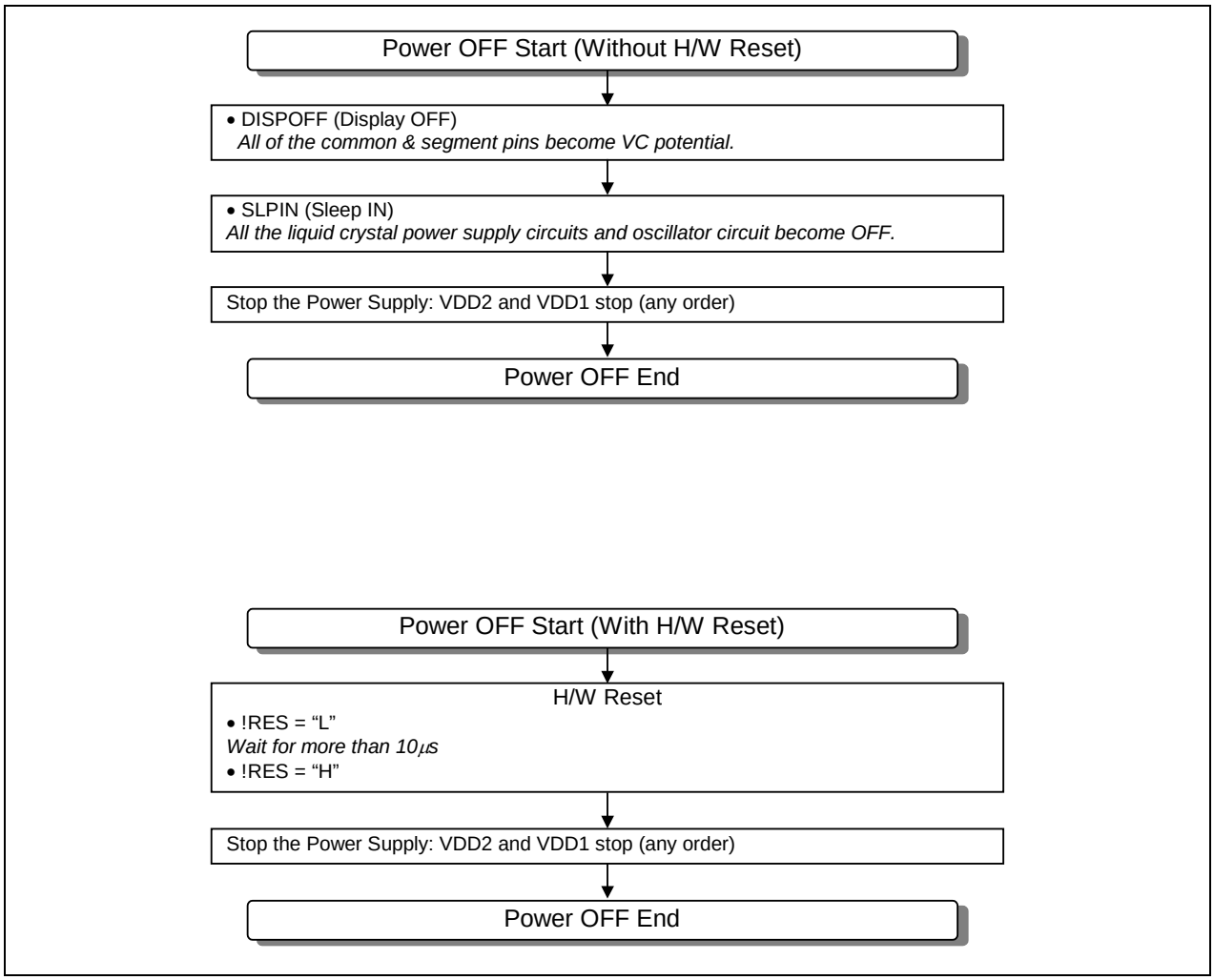
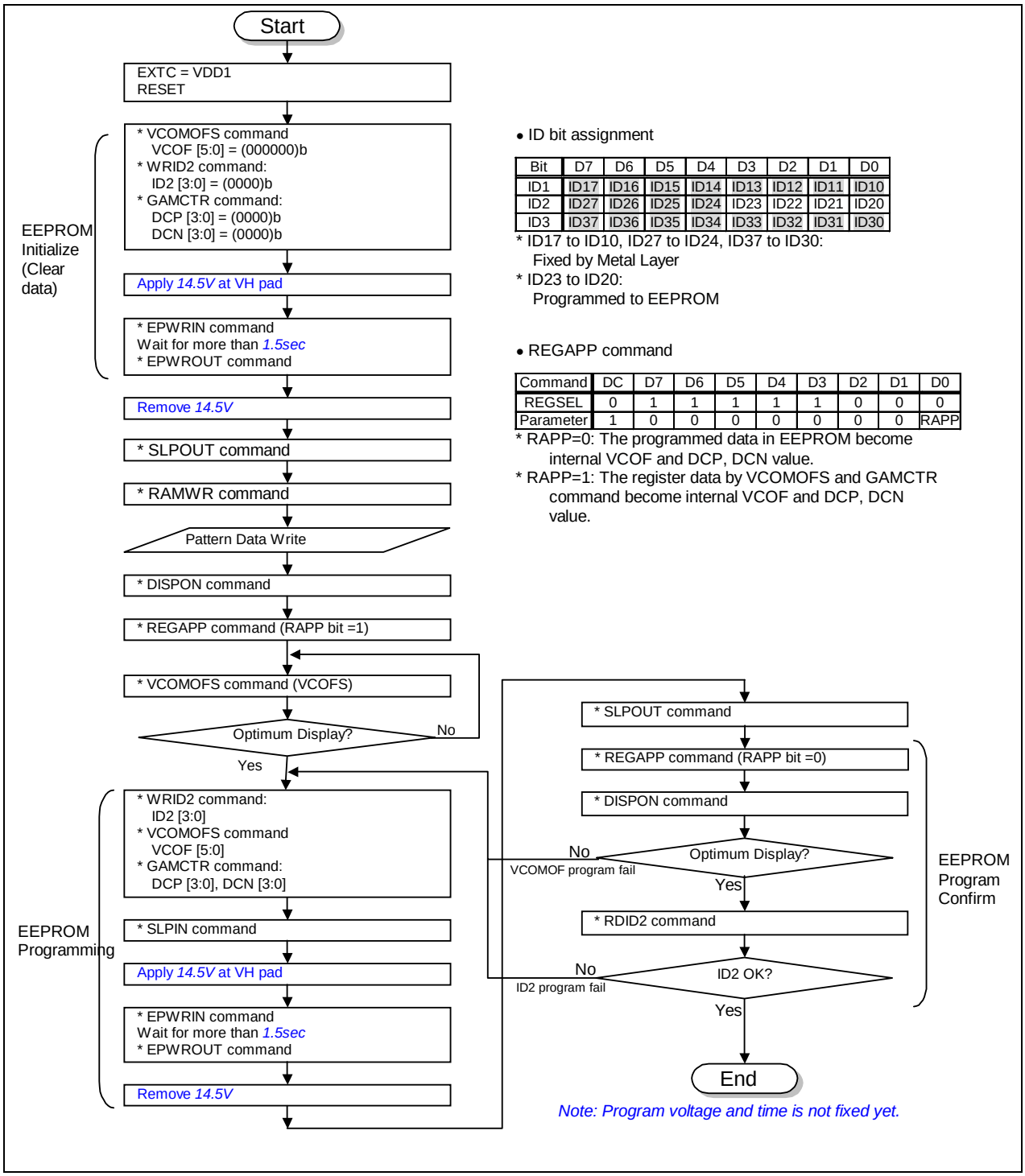


Fig. 6.3.2 Power OFF sequence

6.3.3 EEPROM Access Sequence



• ID bit assignment

Bit	D7	D6	D5	D4	D3	D2	D1	D0
ID1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
ID2	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
ID3	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

* ID17 to ID10, ID27 to ID24, ID37 to ID30:
Fixed by Metal Layer
* ID23 to ID20:
Programmed to EEPROM

• REGAPP command

Command	DC	D7	D6	D5	D4	D3	D2	D1	D0
REGSEL	0	1	1	1	1	1	0	0	0
Parameter	1	0	0	0	0	0	0	0	RAPP

* RAPP=0: The programmed data in EEPROM become internal VCOF and DCP, DCN value.
* RAPP=1: The register data by VCOMOFS and GAMCTR command become internal VCOF and DCP, DCN value.

Fig. 6.3.3 EEPROM write/read sequence

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Item	Symbol	Value	Unit
Supply voltage (1)	V_{DD1}	- 0.3 ~ + 2.8	V
Supply voltage (2)	V_{DD2}	- 0.3 ~ + 3.7	V
Drive Supply Voltage	VGH – VGL2	- 0.3 ~ + 33.0	V
Input voltage range	V_{IN}	- 0.3 ~ V_{DD1} + 0.3	V
Output voltage range	V_O	- 0.3 ~ V_{DD1} + 0.3	V
Operating temperature range	T_{OPR}	- 40 ~ + 85	°C
Storage temperature range	T_{STG}	- 55 ~ + 125	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings

7.2 ESD PROTECTION LEVEL

Table 7.2.1 ESD models.

Model	Test Condition	Protection Level	Unit
Human Body Model	C = 100 pF, R = 1.5 kΩ	> 2000	V
Machine Model	C = 200 pF, R = 0.0 Ω	> 200	V

7.3 LATCH-UP PROTECTION LEVEL

The device will not latch up at trigger current levels less than ±100 mA.

7.4 LIGHT SENSITIVITY

The operation of the IC will not be materially altered by incident light.

7.5 MAXIMUM SERIES RESISTANCE

The driver will operate in 'Chip on Glass' applications with series resistances (due to ITO track resistance). Voltages are specified at module I/O assuming maximum values as in ***Table 7.5.1.***

Table 7.5.1 Maximum series resistance on module.

Name	Type	Maximum Series Resistance	Unit
VDD1	Power supply	50	Ω
VDD2	Power supply	20	Ω
VSS	Power supply	20	Ω
VSS1	Power supply	200	Ω
OSC	Input	500	Ω
SRGB, SMX, SMY, GM1, GM0, CM, FRM, EXTC	Input	500	Ω
P68, BS1, BS0	Input	500	Ω
!RES	Input	200	Ω
!CS (!SCE)	Input	200	Ω
D/!C (SCL)	Input	200	Ω
!WR	Input	200	Ω
!RD	Input	200	Ω
TE, VSYNCO	Output	200	Ω
D17 to D0	Input / Output	200	Ω
VD17 to VD0, DCK, ENABLE, VSYNC, HSYNC	Input	200	Ω
VGH	Capacitor connection	50	Ω
VGL1, VGL2	Capacitor connection	50	Ω
C1P, C1M	Capacitor connection	20	Ω
C2P, C2M	Capacitor connection	20	Ω
C3P, C3M	Capacitor connection	50	Ω
C4P, C4M	Capacitor connection	50	Ω
C5P, C5M	Capacitor connection	50	Ω
C6P, C6M	Capacitor connection	20	Ω
TEST4, TEST5	Input	200	Ω

7.6 DC CHARACTERISTICS

7.6.1 Basic Characteristics

(V_{SS}=0V, V_{DD1}=1.65V to 2.50V, V_{DD2}=2.3V to 2.9V,Ta = -30 to 70°C)

Parameter	Symbol	Conditions	Related Pins	MIN	TYP	MAX	Unit
Power & Operating Voltages							
Logic Operating voltage	V_{DD1}	-	VDD1	1.65	1.8 / 2.1	2.5	V
Analog Operating voltage	V_{DD2}	-	VDD2	2.3	2.5 / 2.75	2.9	
Source Drive Voltage	VS	-	VS	3.0	4.25	5.0	
Gate Drive High Voltage	VGH	-	VGH	9.0	15.0	18.0	
Gate Drive Low Voltage	VGL2	-	VGL2	-13.50	-11.25	-6.0	
Drive Supply Voltage	VGH-VGL2	-	VGH, VGL2	15.0	30.0	31.5	
Input / Output							
High level input voltage	V_{IH}		*1)	0.7V_{DD1}	-	V_{DD1}	V
Low level input voltage	V_{IL}	-	*1)	V_{SS}	-	0.3V_{DD1}	
High level output voltage	V_{OH}	I_{OH} = -1.0mA	D17 to D0, TE, TEST1	0.8V_{DD1}	-	V_{DD1}	
Low level output voltage	V_{OL}	I_{OL} = +1.0mA		V_{SS}	-	0.2V_{DD1}	
Input leakage current	I_{IL}	V_{IN} = V_{DD1} or V_{SS}	*1)	-1.0	-	+1.0	µA
Oscillator frequency	f_{OSC}	-	-	450	500	550	kHz
Booster							
AVDD boost voltage1	AVDD1	IAVDD=1mA, dual-type, X2	AVDD	1.9*VDC	-	2.0*VDC	V
AVDD boost voltage2	AVDD2	IAVDD=1mA, single-type, X2	AVDD	1.8*VDC	-	2.0*VDC	
AVDD boost voltage3	AVDD3	IAVDD=1mA, X3	AVDD	2.5*VDC	-	3.0*VDC	
VGH boost voltage	VGH	I_{GH}=300uA, 3*VR	VGH	2.7*VGDI	-	3.0*VGDI	
VGL1 boost voltage	VGL1	I_{GL1}=-300uA, -2*VR	VGL1	-2*VGDI	-	-1.8*VGDI	
VGL2 boost voltage	VGL2	I_{GL2}=-300uA, -3*VR	VGL2	-3*VGDI	-	-2.7*VGDI	
VCL boost voltage	VCL	I_{CL}=-300uA, -1*VDD2	VCL	-1*VDC	-	-0.9*VDC	
VS output voltage	VS	No load	VS	4.10	4.25	4.40	
VR output voltage	VR	No load	VR	3.60	3.75	3.90	

NOTE:

CM, SRGB, SMX, SMY, GM1, GM0, DCK, ENABLE, VSYNC, HSYNC, OSC, P68, BS1, BS0, !CS, !RES, D/!C, !WR, !RD, PD17 to PD0 and D17 to D0 pins

Parameter	Symbol	Conditions	Related Pins	MIN	TYP	MAX	Unit
VCOM Generator							
VCOM amplitude	VCOMA	No load	VCOMH VCOML	4.55	4.70	4.85	V
VCOM output high resistance	R_{VCOMH}	VCOM output = High I_{VCOM} = 1mA	VCOM	-	100	TBD	Ω
VCOM output low resistance	R_{VCOML}	VCOM output = Low I_{VCOM} = 1mA	VCOM	-	100	TBD	
Source Driver							
Gray scale resistance	Rgray	Rap~Rjp, Ran~Rjn, R0~R62 of gray voltage generator	S1 to S528	0.7*Rx	Rx	1.3*Rx	Ω
*1) *2) Drive output current	I_{VOSH}	VS=5V, VSO=V0 at positive, VOUT=V0-2V	S1 to S528	-	-200	-100	μA
	I_{VOSL}	VS=5V, VSO=V0 at negative, VOUT=V0-2V	S1 to S528	100	200	-	μA
Output voltage deviation	D_{VOS}	VSS1+1.0 ~ VS-1.0	S1 to S528	-	±10	±20	mV
		VSS1+0.1V ~ VSS1+1.0 VS-1.0 ~ VS-0.1V	S1 to S528	-	±30	±50	mV
Output voltage range	V_{OS}	-	S1 to S528	0.1	-	VS-0.1	V
Gate Driver							
*3) Output ON resistance	R_{ONG}	Ta = 25°C	G0 to G241	-	2	3	kΩ

NOTE:

1) V_{SO} is the output voltage of source output pins S1 to S528.

2) V_{OUT} is the applied voltage to source output pins S1 to S528.

3) Resistance value when -0.1[mA] is applied during the ON status of the gate output pin G0 to G240.

R_{ON} [kΩ] = ΔV [V] / 0.1[mA] (ΔV: Voltage change when –0.1[mA] is applied in the on status.)

7.6.2 Current Consumption

Host I/F	Mode of operation	Frame Frequency	Inversion Mode	Image	Memory Data Access Control (MY:MX:MV)	Current consumption			
						Typical		Worst case	
						VDD2 (mA)	VDD1 (mA)	VDD2 (mA)	VDD1 (mA)
Host interface NOT active	- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	60Hz		Note 1	X;X;X				
				Note 2	X;X;X				
				Note 3	X;X;X				
				Note 4	X;X;X				
				Note 5	X;X;X				
	- Normal Mode On - Partial Mode Off - Idle Mode On - Sleep Out Mode	60Hz		Note 5	X;X;X				
	- Normal Mode Off - Partial Mode On (32 lines) - Idle Mode Off - Sleep Out Mode	60Hz		Grey Levels	X;X;X				
	- Normal Mode Off - Partial Mode On (32 lines) - Idle Mode On - Sleep Out Mode	60Hz		Note 6	X;X;X				
				Note 7	X;X;X				
	- Sleep In Mode	N/A	N/A	N/A	X;X;X	0.002		0.010	
Host interface active	- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode		Full screen	65k Colors Checker board one by one CPU Access @ 10fps	0;0;0				
					0;0;1				
					0;1;0				
					0;1;1				
					1;0;0				
					1;0;1				
					1;1;0				
					1;1;1				

NOTE:

X Do not care

1. *All pixels black*
2. *Checker board one by one*
3. *Checker board 4 by 4*
4. *Grey-scale from top to bottom*
5. *20% Black, 80%White*
6. *Black & White Checker board 8 by 8.*
7. *Absolute Worst Case Patterns:*
   - *Black & White Horizontal Stripe 1 by 1*
   - *Black & White Checker board 1pixel by 1pixel*
   - *Black & White Checker board 1dot by 1dot*

Typical Case:
T_A = 25ºC
VDD2 = 2.75V
VDD1 = 1.8V

Worst Case:
T_A = -30 to70ºC
VDD2 = 2.3V to 2.9V
VDD1 = 1.65V to 2.5V
Includes Process Variance.

7.7 AC CHARACTERISTICS

7.7.1 Parallel Interface Characteristics (8080-series MPU)

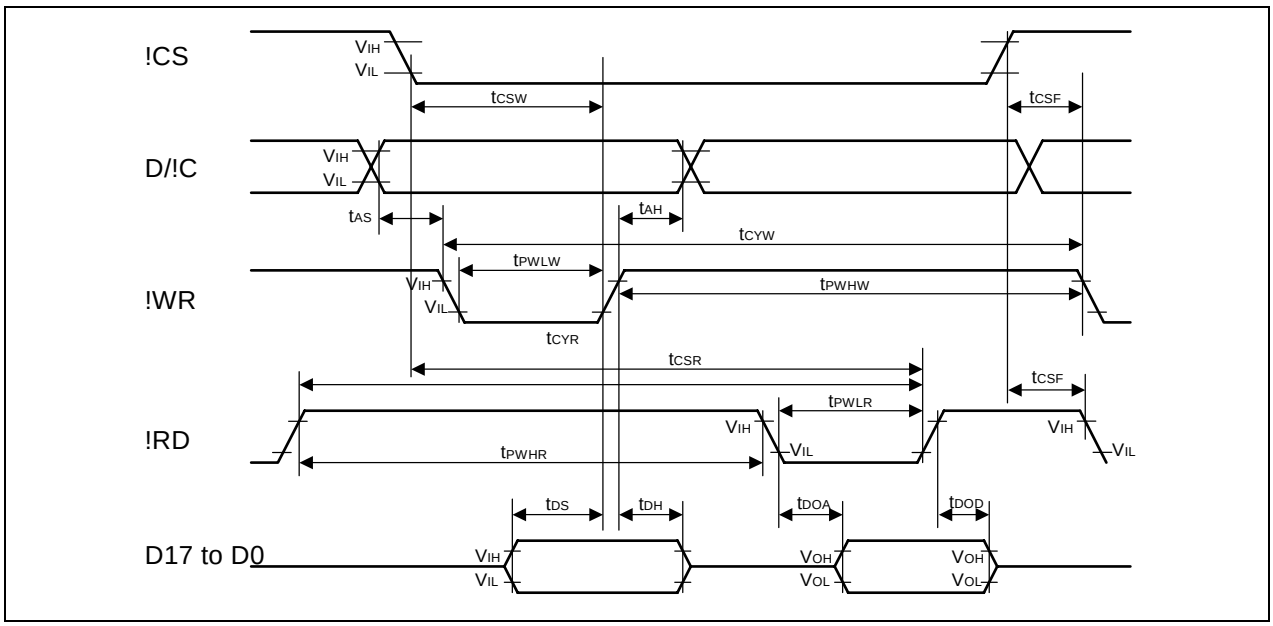


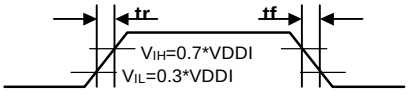
Fig. 7.7.1 Parallel Interface characteristics (8080-series MPU)

(V_{SS}=0V, V_{DD1}=1.65V to 2.50V, V_{DD2}=2.3V to 2.9V,Ta = -30 to 70°C)

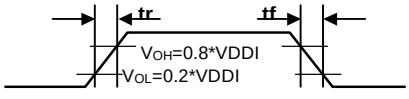
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CSW}, t_{CSR} t_{CSF}	Chip select setup time Chip select hold time	-	!CS	40 10	- -	- -	ns
t_{AS} t_{AH}	Address setup time Address hold time	-	D/!C	10 10	- -	- -	ns
t_{CYW} t_{PWHW} t_{PWLW}	Write cycle time Write High Time Write Low Time	-	!WR	150 90 40	-	-	ns
t_{CYR} t_{PWHR} t_{PWLR}	Read cycle time (Parameter read) Read High (Parameter read) Read Low (Parameter read)	-	!RD	150 90 40	-	-	ns
t_{CYR} t_{PWHR} t_{PWLR}	Read cycle time (Data read) Read High (Data read) Read Low (Data read)	-	!RD	450 355 90	-	-	ns
t_{DS} t_{DH}	Data setup time Data hold time	-	D17 to D0	10 10	- -	- -	ns
t_{DOA} t_{DOD}	Data output access time Data output disable time	CL = 30pF		- 40	- -	40 80	ns

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Input Signal Slope



Output Signal Slope



7.7.2 Parallel Interface Characteristics (6800-series MPU)

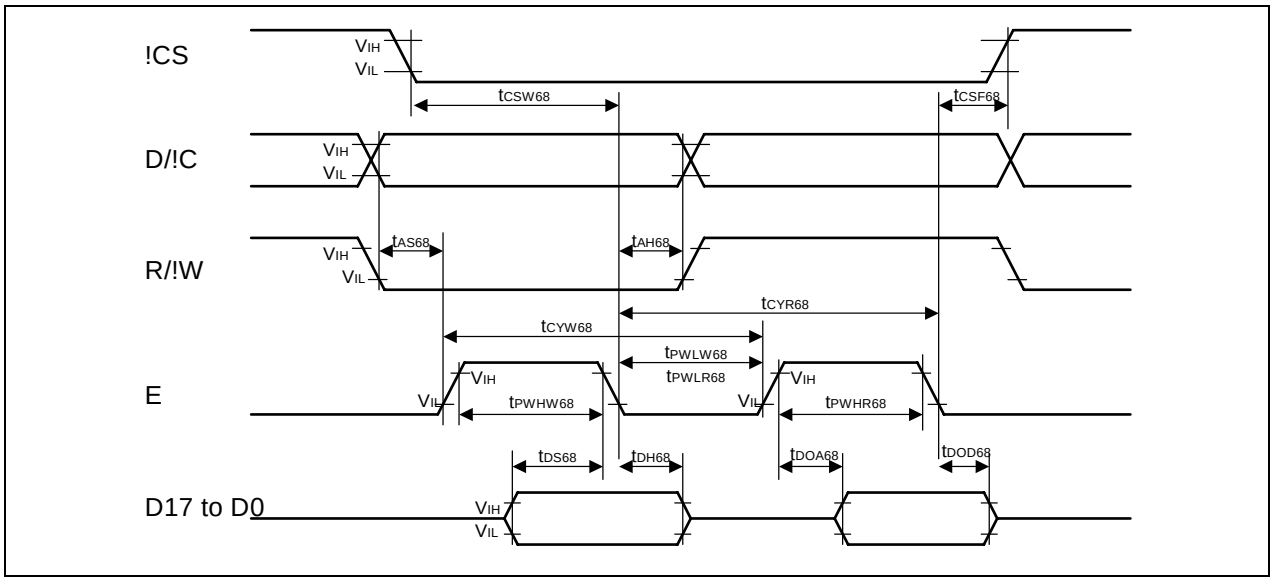


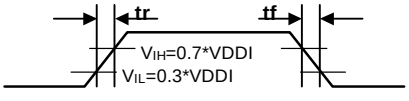
Fig. 7.7.2 Parallel Interface characteristics (8080-series MPU)

(V_{SS}=0V, V_{DD1}=1.65V to 2.50V, V_{DD2}=2.3V to 2.9V,Ta = -30 to 70°C)

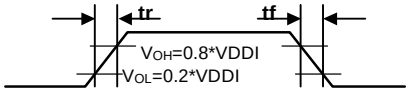
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CSW68} t_{CSF68}	Chip select setup time Chip select hold time	-	!CS	40 10	- -	- -	ns
t_{AS68} t_{AH68}	Address setup time Address hold time	-	D/!C R/!W	10 10	- -	- -	ns
t_{CYW68} t_{PWHW68} t_{PWLW68}	Write cycle time Write High Time Write Low Time	-	E	150 40 90	-	-	ns
t_{CYR68} t_{PWHR68} t_{PWLR68}	Read cycle time (Parameter read) Read High (Parameter read) Read Low (Parameter read)	-	E	150 40 90	-	-	ns
t_{CYR68} t_{PWHR68} t_{PWLR68}	Read cycle time (Data read) Read High (Data read) Read Low (Data read)	-	E	450 90 355	-	-	ns
t_{DS68} t_{DH68}	Data setup time Data hold time	-	D17 to D0	10 10	- -	- -	ns
t_{DOA68} t_{DOD68}	Data output access time Data output disable time	CL = 30pF		- 40	- -	40 80	ns

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Input Signal Slope



Output Signal Slope



7.7.3 Serial Interface Characteristics

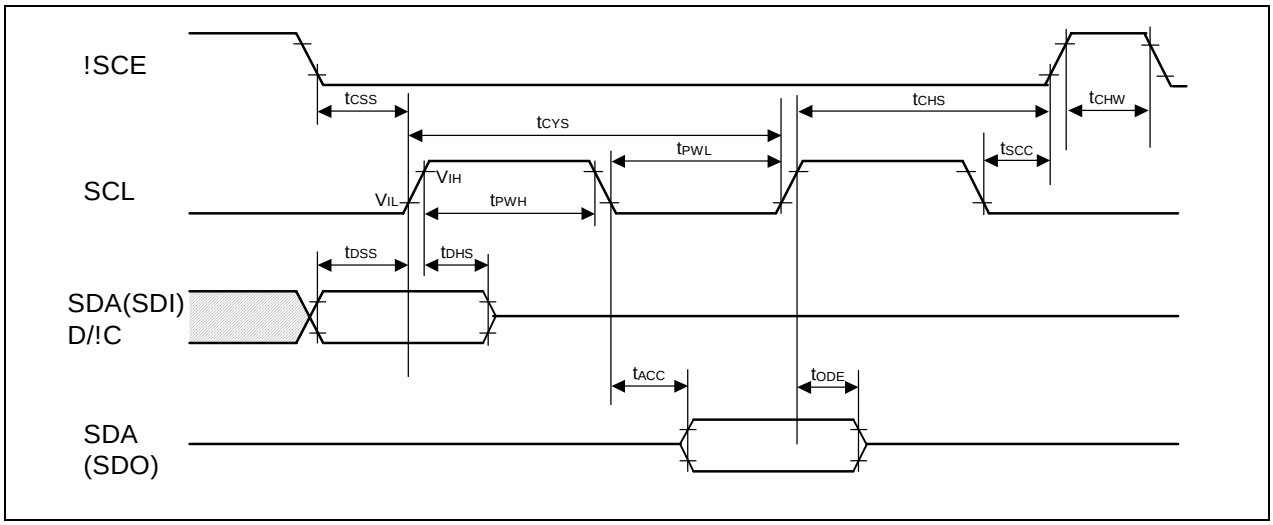


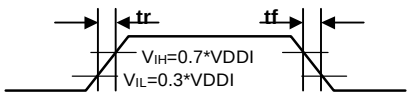
Fig. 7.7.3 Serial interface characteristics

(V_{SS}=0V, V_{DD1}=1.65V to 2.50V, V_{DD2}=2.3V to 2.9V,Ta = -30 to 70°C)

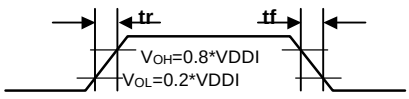
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CYS} t_{WHS} t_{WLS}	Serial clock cycle High pulse width High pulse width	-	SCL	150 60 60	- -	- -	ns
t_{DSS} t_{DHS}	Data (D/!C) setup time Data (D/!C) hold time		SDA (SDI) D/!C	60 60	- -	- -	ns
t_{CSS} t_{CHS} t_{CHW}	Chip select setup time Chip select hold time Chip select high pulse width	-	!SCE	60 65 45	- - -	- - -	ns
t_{SCC}	SCL to Chip select	-	SCL, !SCE	20	-	-	ns
t_{ACC} t_{ODE}	SDO access time SDO disable time	*1)	SDA (SDO)	10 25	- -	50 80	ns

*NOTE:*1) t_{ACC} condition: Load = 30pF, t_{ODE} condition: Load = 5pF and R = 3kOhm*
The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Input Signal Slope



Output Signal Slope



7.7.4 RGB Interface Characteristics

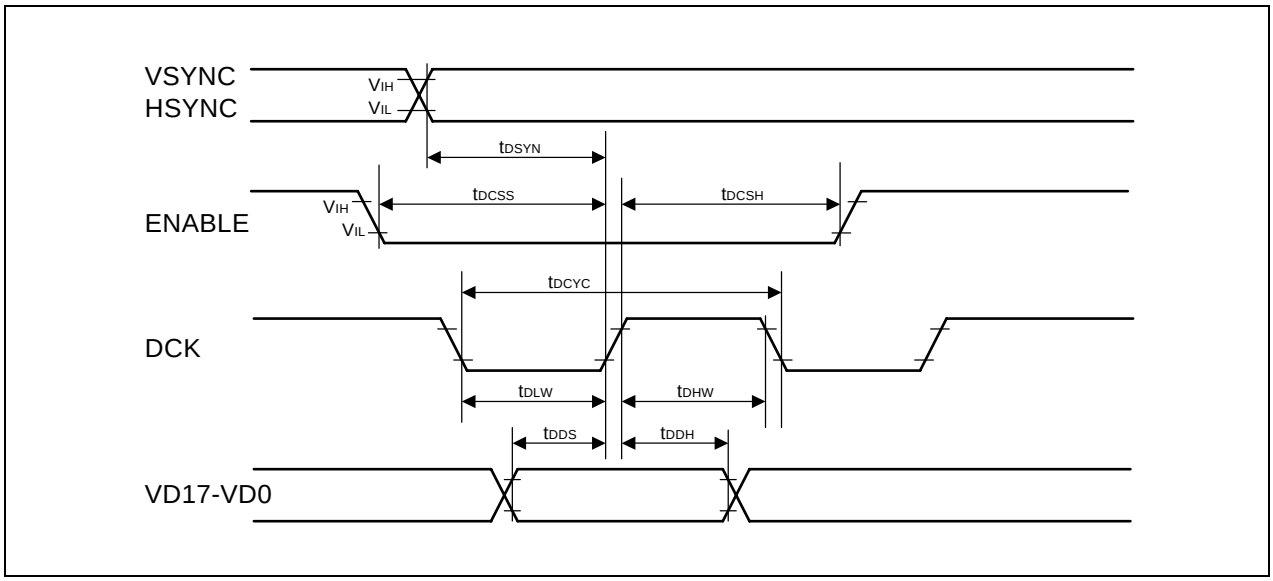


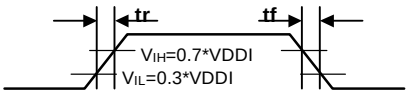
Fig. 7.7.4 RGB Interface characteristics

(V_{SS}=0V, V_{DD1}=1.65V to 2.50V, V_{DD2}=2.3V to 2.9V,Ta = -30 to 70°C)

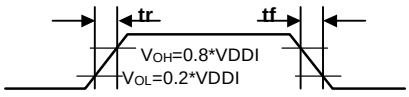
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{DCYC} t_{DLW} t_{CHW}	DCK cycle time DCK Low time DCK High time	-	DCK	TBD TBD TBD	- -	- -	ns
t_{DDS} t_{DDH}	RGB Data setup time RGB Data hold time	-	DCK, VD17-VD0	20 20	- -	- -	ns
t_{DCSS} t_{DCSH}	ENABLE setup time ENABLE hold Time	-	ENABLE	150 150	-	-	ns
t_{DSYN}	SYNC setup time	-	DCK, HSYNC, VSYNC	20	-	-	ns

NOTE: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Input Signal Slope



Output Signal Slope



7.7.5 Reset Input Timing

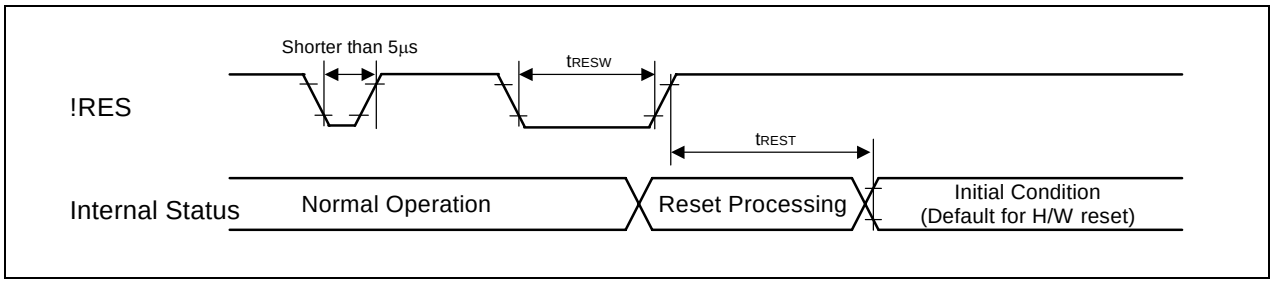


Fig. 7.7.5 Reset input timing

(V_{SS}=0V, V_{DD1}=1.65V to 2.50V, V_{DD2}=2.3V to 2.9V,Ta = -30 to 70°C)

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	!RES	10	-	-	-	µs
t_{REST}	*2) Reset complete time	-	-	-	5	-	ms

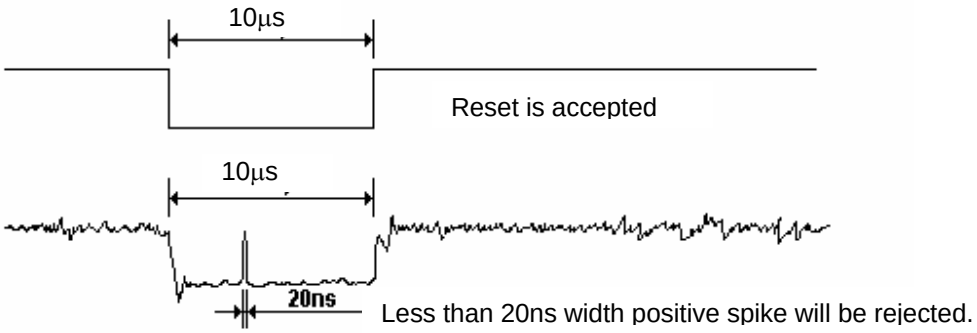
NOTE:

1) Spike due to an electrostatic discharge on !RES line does not cause irregular system reset according to the table below.

!RES Pulse	*Action*
Shorter than 5µs	*Reset Rejected*
Longer than 10µs	*Reset*
Between 5µs and 10µs	*Not Determined*

2) During the resetting period, the display will be blanked and then return to Default condition for H/W reset.

3) Spike Rejection also applies during a valid reset pulse as shown below:

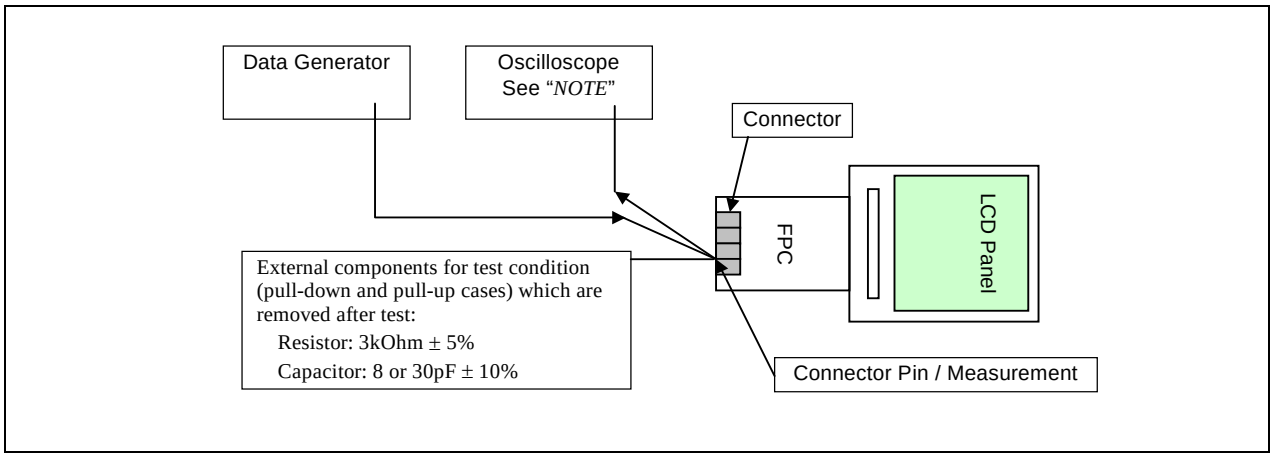


4) It is necessary to wait 10µsec after releasing !RES before sending commands. After reset complete, Sleep Out command can be sent to start internal power circuit.

7.7.6 Measurement Conditions

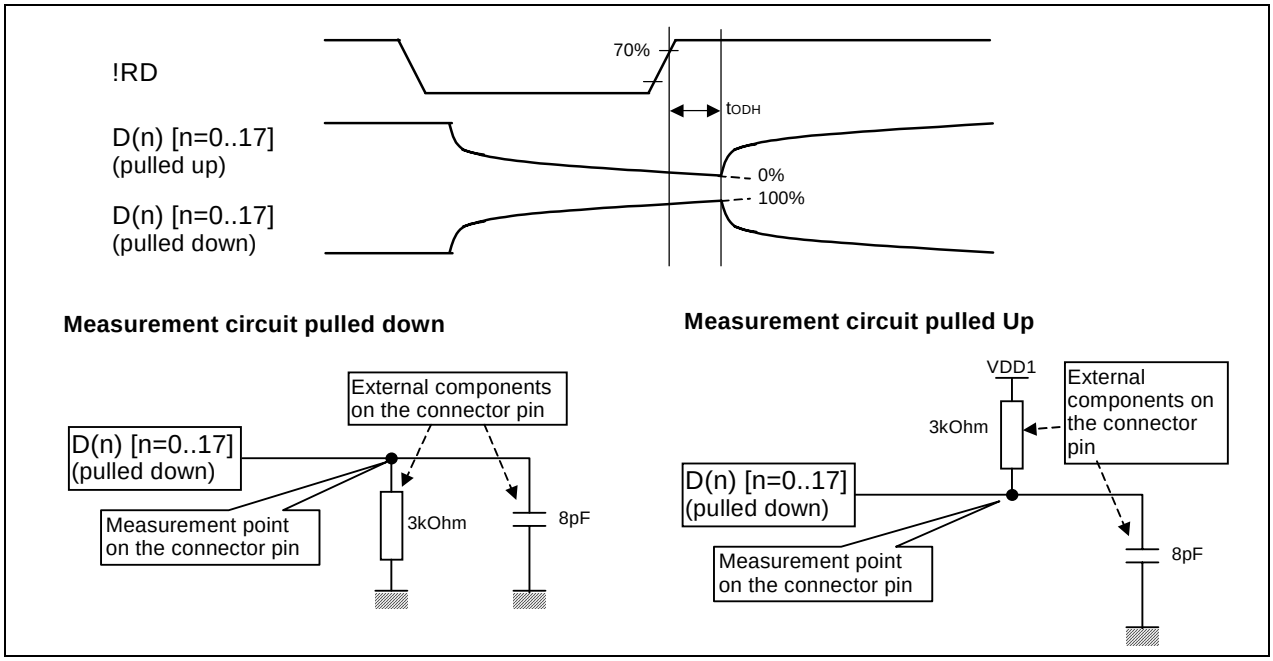
7.7.6.1 t_{DOA}, t_{DOD} Measurement Condition

Measurement Condition Set-up

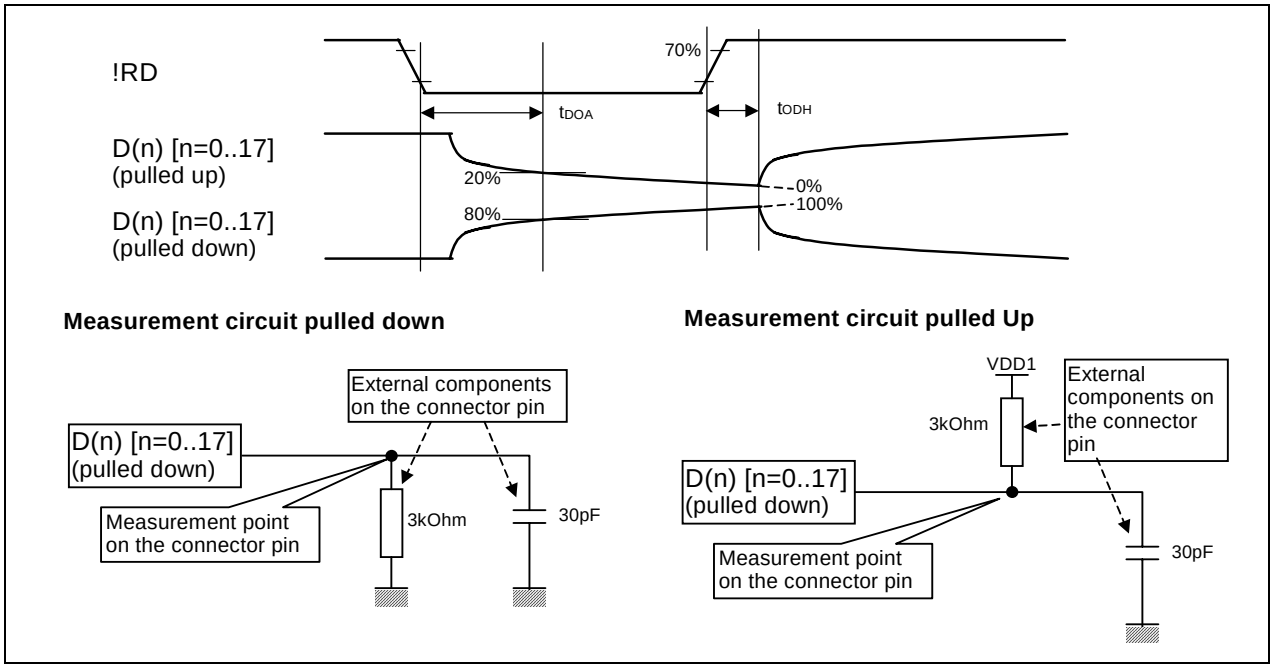


NOTE: Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements

Minimum Value Measurement



Maximum Value Measurement



8 REFERENCE APPLICATIONS

8.1 MICROPROCESSOR INTERFACE

8.1.1 Interfacing with 3-Pin Serial Mode (P68 = "L", BS1 = "L", BS0 = "L")

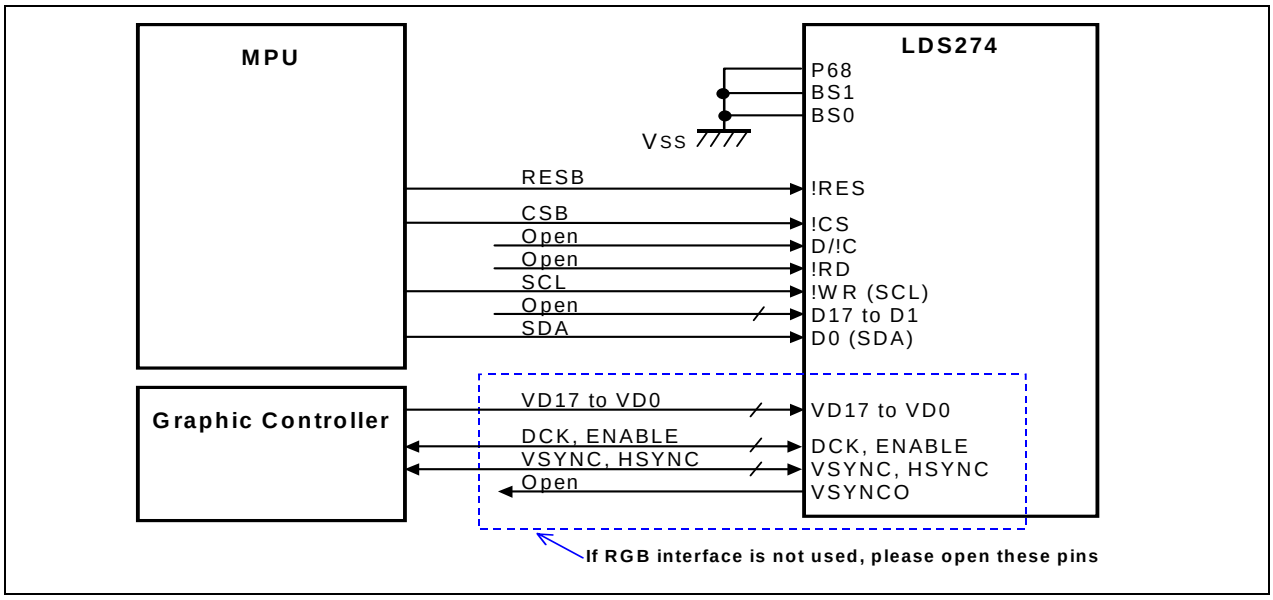


Fig. 8.1.1 Interfacing with 3-Pin Serial Mode

8.1.2 Interfacing with 4-Pin Serial Mode (P68 = "L", BS1 = "L", BS0 = "H")

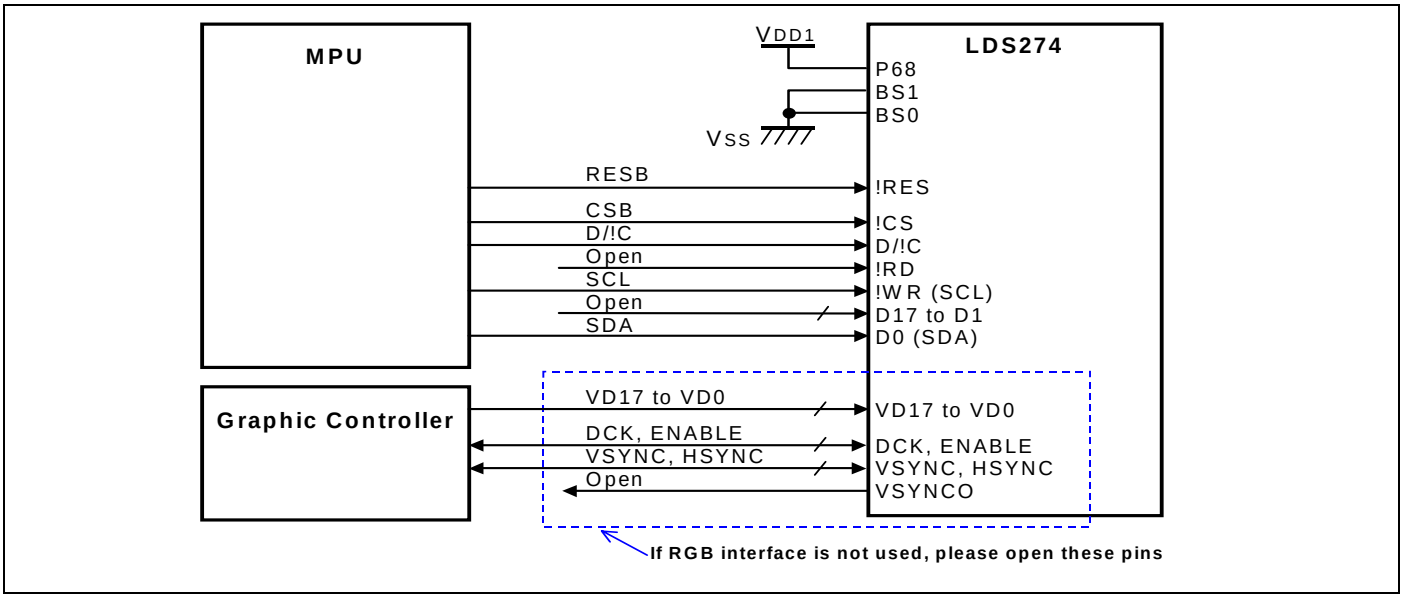


Fig. 8.1.2 Interfacing with 4-Pin Serial Mode

8.1.3 Interfacing with 8080-series MPU 8-Bit Bus (P68 = "L", BS1 = "L", BS0 = "H")

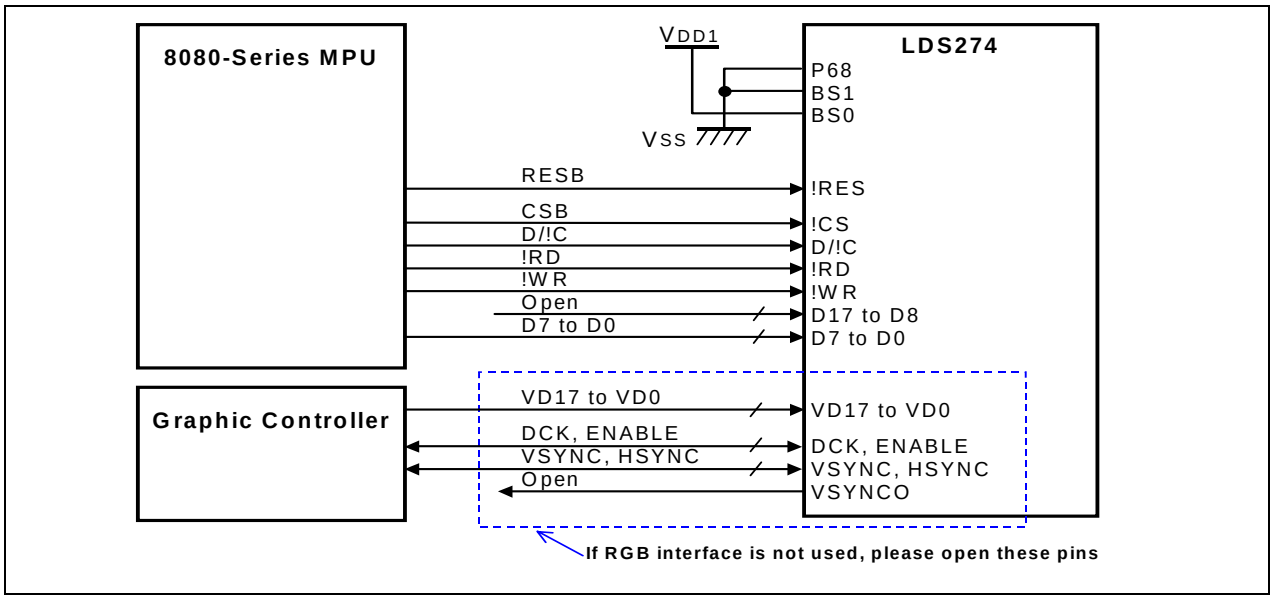


Fig. 8.1.3 Interfacing with 8-bit 8080-series

8.1.4 Interfacing with 6800-series MPU 8-Bit Bus (P68 = "H", BS1 = "L", BS0 = "H")

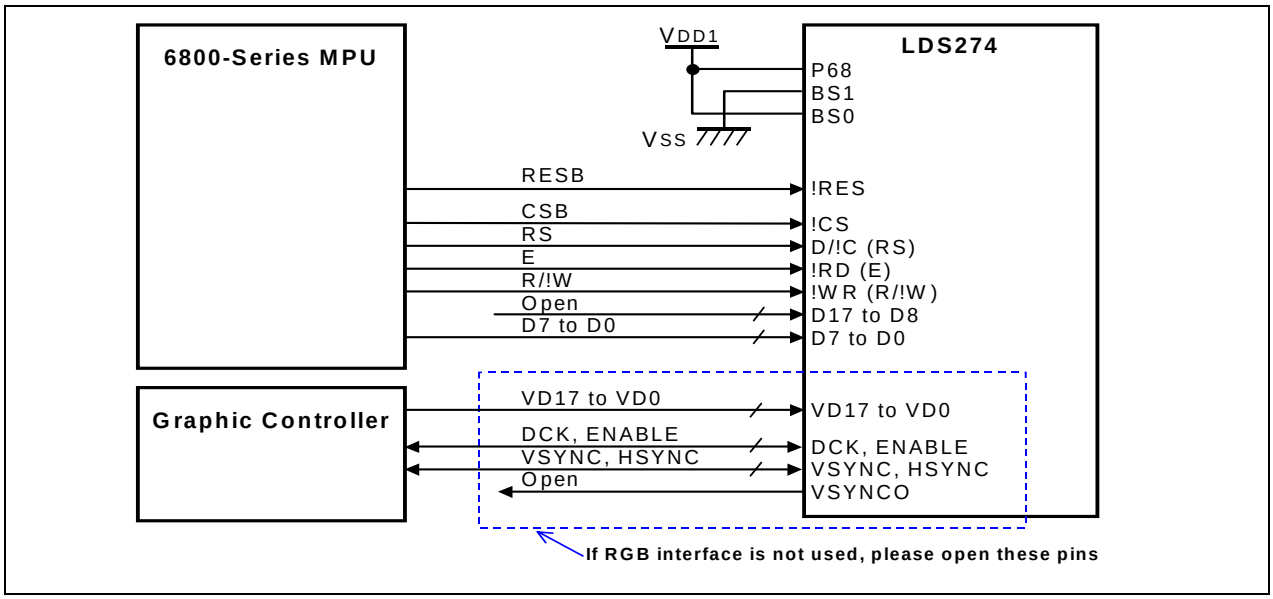


Fig. 8.1.4 Interfacing with 8-bit 6800-series

8.1.5 Interfacing with 8080-series MPU 16-Bit Bus (P68 = "L", BS1 = "H", BS0 = "L")

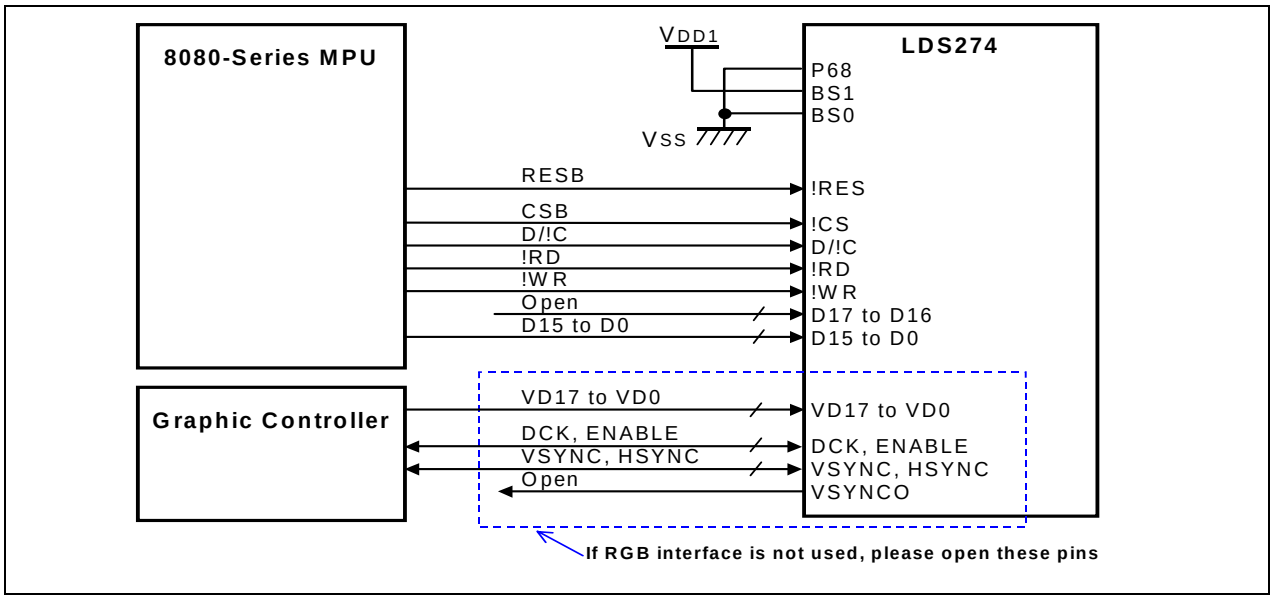


Fig. 8.1.5 Interfacing with 16-bit 8080-series

8.1.6 Interfacing with 6800-series MPU 16-Bit Bus (P68 = "H", BS1 = "H", BS0 = "L")

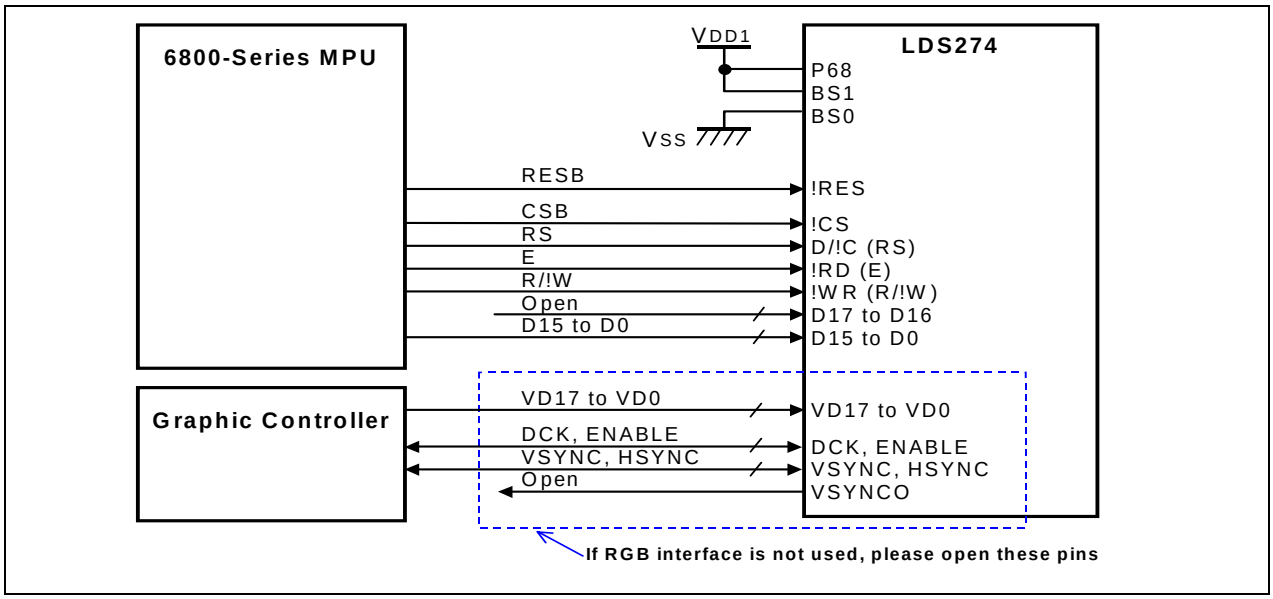


Fig. 8.1.6 Interfacing with 16-bit 6800-series

8.1.7 Interfacing with 8080-series MPU 18-Bit Bus (P68 = "L", BS1 = "H", BS0 = "H")

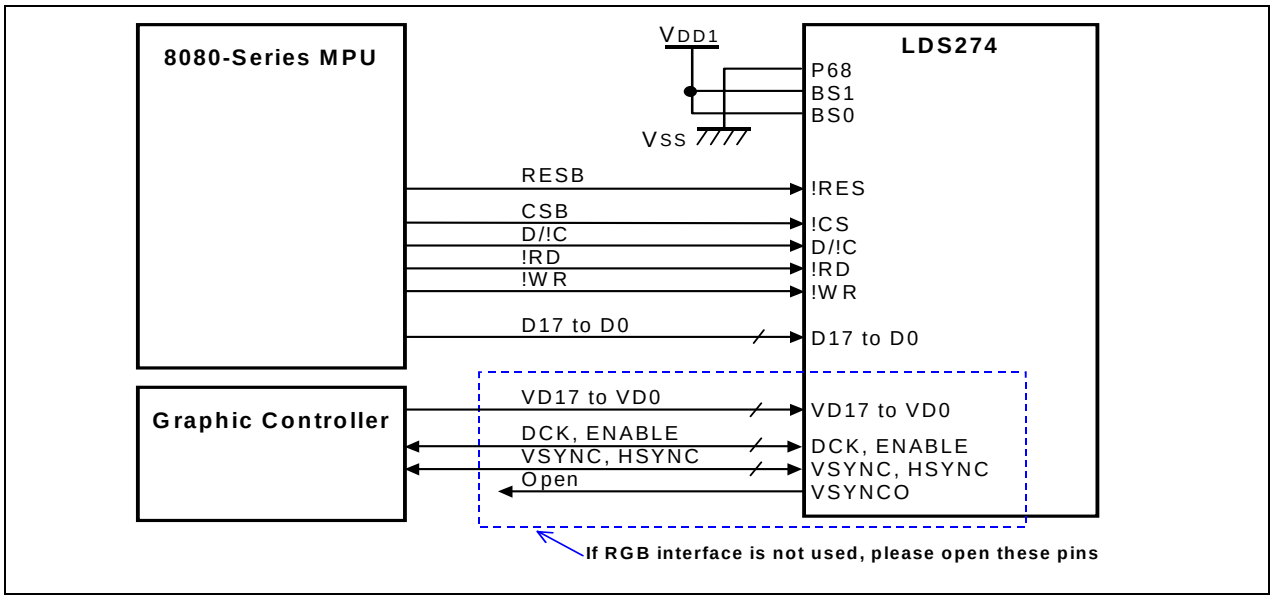


Fig. 8.1.7 Interfacing with 18-bit 8080-series

8.1.8 Interfacing with 6800-series MPU 18-Bit Bus (P68 = "H", BS1 = "H", BS0 = "H")

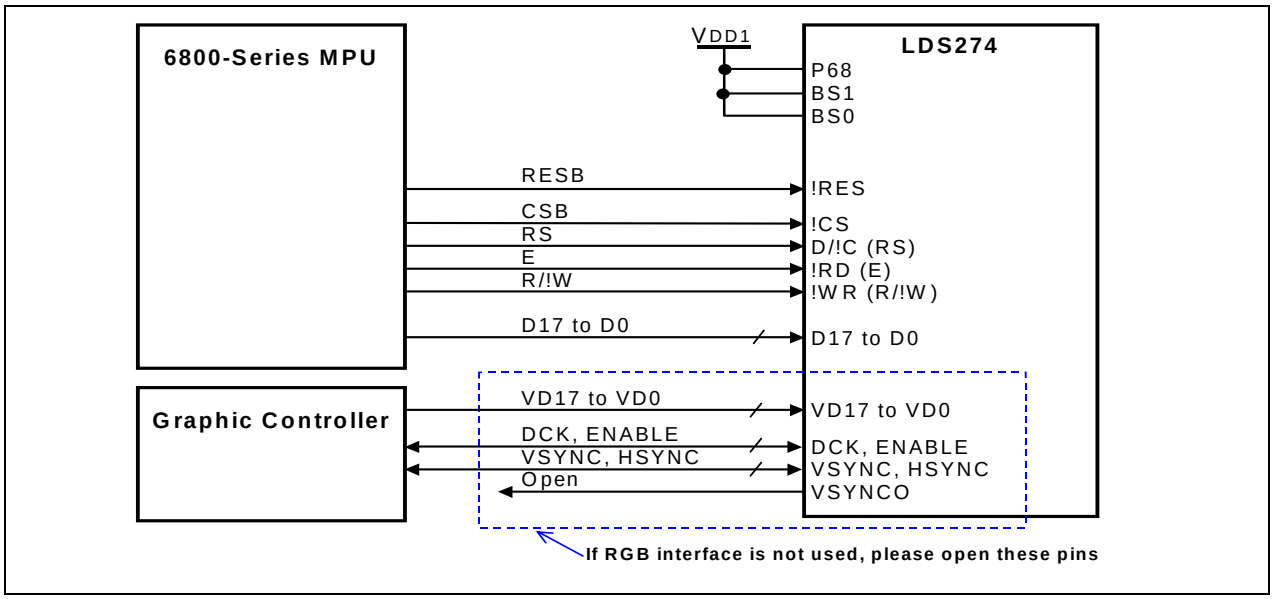
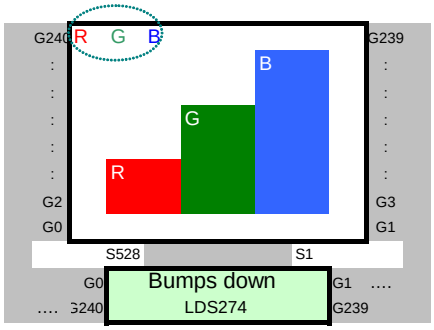
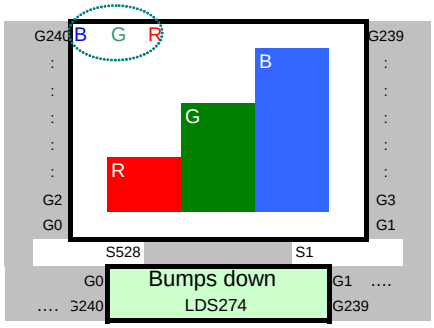
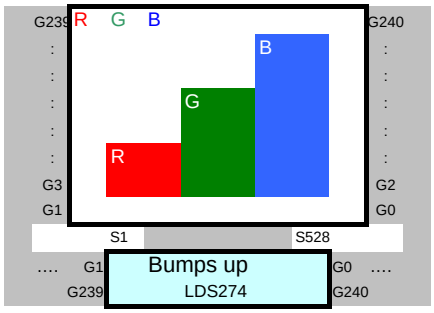
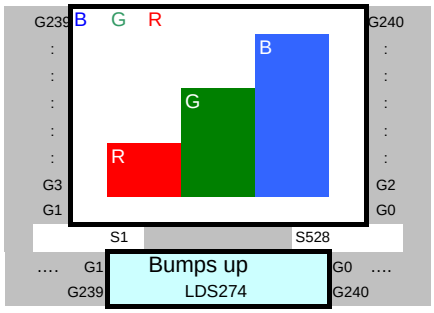
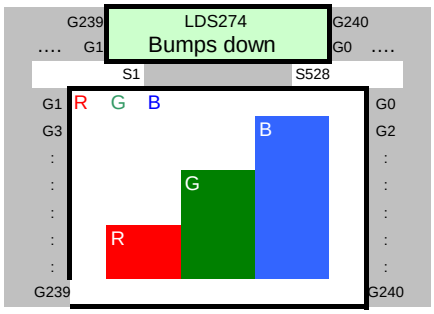
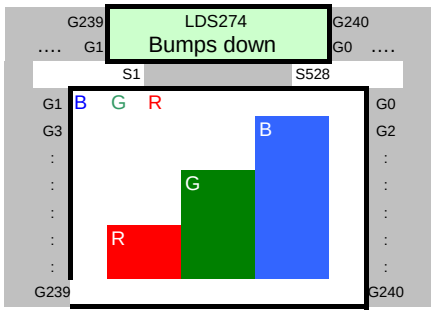
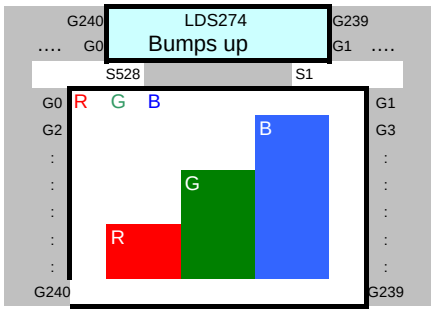
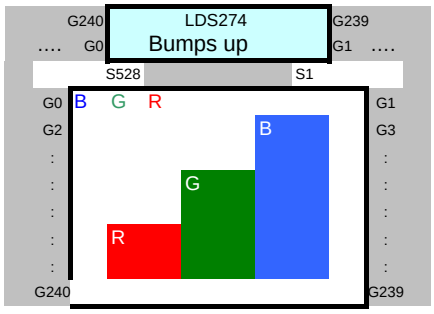
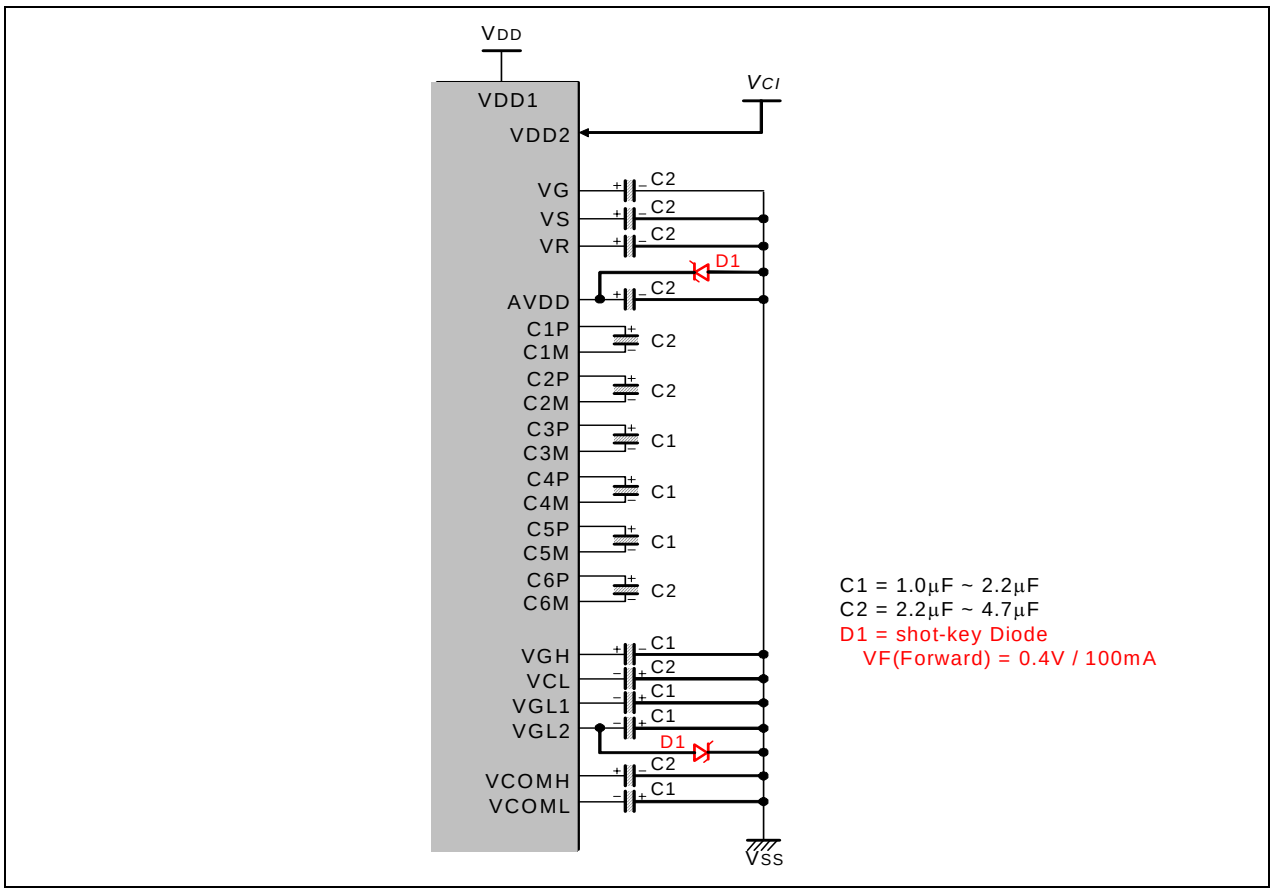


Fig. 8.1.8 Interfacing with 18-bit 6800-series

8.2 CONNECTIONS WITH LCD PANEL

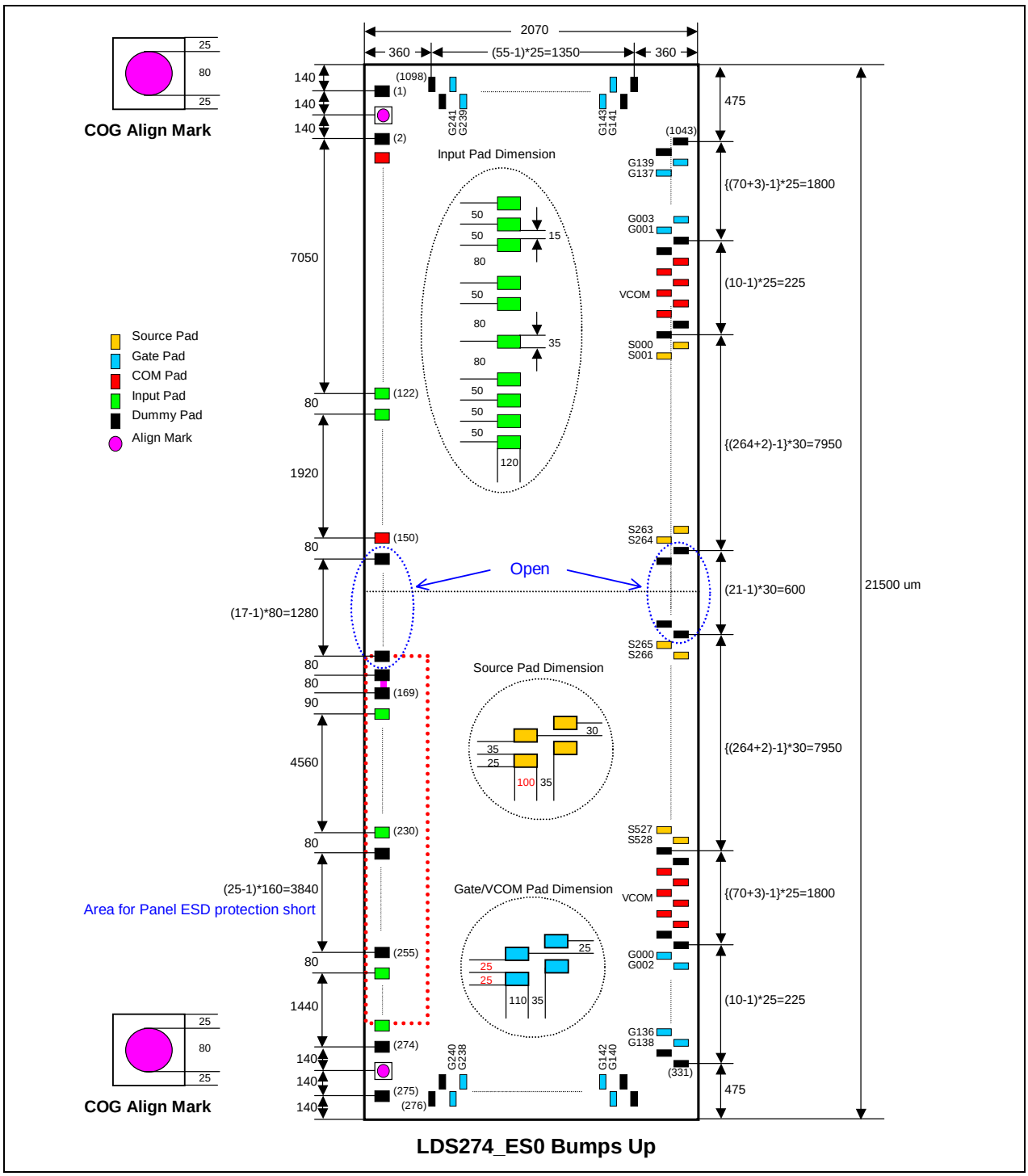
RGB filter order = RGB (from left top of the panel)	RGB filter order = BGR (from left top of the panel)
 SMX = 1 SMY = 1 SRGB = 1 S1 = Filter B S2 = Filter G S3 = Filter R …	 SMX = 1 SMY = 1 SRGB = 0 S1 = Filter R S2 = Filter G S3 = Filter B …
 SMX = 0 SMY = 1 SRGB = 0 S1 = Filter R S2 = Filter G S3 = Filter B …	 SMX = 0 SMY = 1 SRGB = 1 S1 = Filter B S2 = Filter G S3 = Filter R …
 SMX = 0 SMY = 0 SRGB = 0 S1 = Filter R S2 = Filter G S3 = Filter B …	 SMX = 0 SMY = 0 SRGB = 1 S1 = Filter B S2 = Filter G S3 = Filter R …
 SMX = 1 SMY = 0 SRGB = 1 S1 = Filter B S2 = Filter G S3 = Filter R …	 SMX = 1 SMY = 0 SRGB = 0 S1 = Filter R S2 = Filter G S3 = Filter B …

8.3 CONNECTION EXAMPLE WITH EXTERNAL COMPONENTS



9 CHIP INFORMATION

9.1 CHIP OVERVIEW



LDS274_ES0 Bumps Up

NOTE:

** Chip Size = 21,500 x 2,070 (Excluding Scribe Lane)*

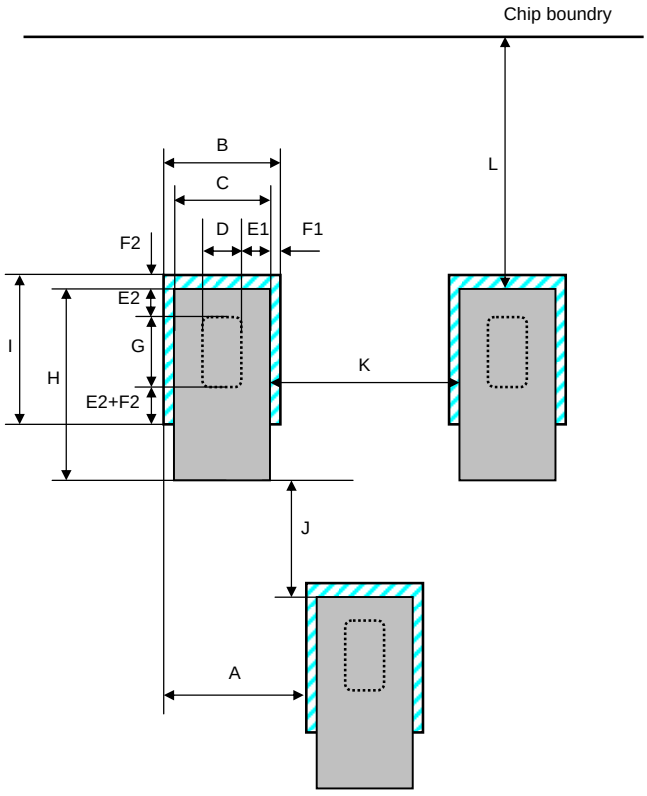
** Chip Thickness = 410 ± 12 μm*

** Bump height = 17 ± 3 μm (chip to chip), less than 2 μm (pad to pad in one chip)*

9.2 BUMP INFORMATION

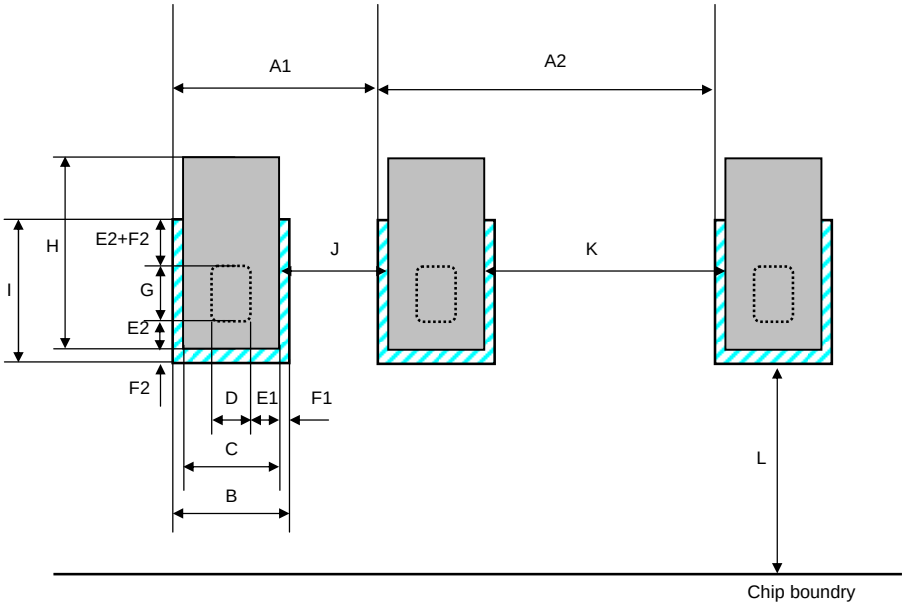
9.2.1 Source/Gate/VCOM Output Pad Format

Item	Symbol	Size	
		Source	Gate / VCOM
Pad pitch	A	30 um	25 um
AL width	B	32 um	32 um
Bump width	C	25 um	25 um
Pad open width	D	12 um	12 um
AL height	I	52 um	72 um
Bump height	H	100 um	110 um
Pad open height	G	32 um	52 um
Pad open to Bump gap	E1	6.5 um	6.5 um
	E2	6.5 um	6.5 um
Bump to AL gap	F1	3.5 um	3.5 um
	F2	3.5 um	3.5 um
Bump to Bump gap1 (Vertical)	J	35 um	35 um
Bump to Bump gap2 (Horizontal)	K	35 um	25 um
Bump area	C*H	2500 um^2	2750 um^2
Chip boundary to Bump edge	L	70 um	80 um



9.2.2 Input/Output Pad Format

Item	Symbol	Size
Pad pitch1 (within Multi pad group)	A1	50 um
Pad pitch2 (between Multi pad group)	A2	80 um
AL width	B	45 um
Bump width	C	35 um
Pad open width	D	22 um
AL height	I	85 um
Bump height	H	120 um
Pad open height	G	42 um
Pad open to Bump gap	E1	6.5 um
	E2	6.5 um
Bump to AL gap	F1	5 um
	F2	15 um
Bump to Bump gap (within Multi pad group)	J	15 um
Bump to Bump gap (between Multi pad group)	K	45 um
Bump area	C*H	4200 um^2
Chip boundary to Bump edge	L	80 um



9.3 PAD COORDINATES

Table 9.3.1 Pad Center Coordinates

No	Name	X	Y	No	Name	X	Y
1	DUMMY	-10610	-895	51	C5+	-7370	-895
2	DUMMY	-10330	-895	52	C5-	-7290	-895
3	VCOM	-10250	-895	53	C5-	-7240	-895
4	DUMMY	-10170	-895	54	C4+	-7160	-895
5	VCOMH	-10090	-895	55	C4+	-7110	-895
6	VCOMH	-10040	-895	56	C4-	-7030	-895
7	VCOMH	-9990	-895	57	C4-	-6980	-895
8	VCOML	-9910	-895	58	C3+	-6900	-895
9	VCOML	-9860	-895	59	C3+	-6850	-895
10	VCOML	-9810	-895	60	C3-	-6770	-895
11	VCOMS	-9730	-895	61	C3-	-6720	-895
12	VCOMS	-9680	-895	62	C2+	-6640	-895
13	VGLDC	-9600	-895	63	C2+	-6590	-895
14	VGLDC	-9550	-895	64	C2+	-6540	-895
15	VGLAC	-9470	-895	65	C2+	-6490	-895
16	VGLAC	-9420	-895	66	C2+	-6440	-895
17	VGLI	-9340	-895	67	C2-	-6360	-895
18	VGLI	-9290	-895	68	C2-	-6310	-895
19	VGL2	-9210	-895	69	C2-	-6260	-895
20	VGL2	-9160	-895	70	C2-	-6210	-895
21	VGL2	-9110	-895	71	C2-	-6160	-895
22	VGL1	-9030	-895	72	C1+	-6080	-895
23	VGL1	-8980	-895	73	C1+	-6030	-895
24	VGL1	-8930	-895	74	C1+	-5980	-895
25	VCL	-8850	-895	75	C1+	-5930	-895
26	VCL	-8800	-895	76	C1+	-5880	-895
27	VCL	-8750	-895	77	C1-	-5800	-895
28	VCL	-8700	-895	78	C1-	-5750	-895
29	VDD2	-8620	-895	79	C1-	-5700	-895
30	VDD2	-8570	-895	80	C1-	-5650	-895
31	VDD2	-8520	-895	81	C1-	-5600	-895
32	VDD2	-8470	-895	82	VDD2	-5520	-895
33	VDD2	-8420	-895	83	VDD2	-5470	-895
34	VSS	-8340	-895	84	VDD2	-5420	-895
35	VSS	-8290	-895	85	VDD2	-5370	-895
36	VSS	-8240	-895	86	VDD2	-5320	-895
37	VSS	-8190	-895	87	VSS	-5240	-895
38	VSS	-8140	-895	88	VSS	-5190	-895
39	VGH	-8060	-895	89	VSS	-5140	-895
40	VGH	-8010	-895	90	VSS	-5090	-895
41	VGH	-7960	-895	91	VSS	-5040	-895
42	C6+	-7880	-895	92	AVDD	-4960	-895
43	C6+	-7830	-895	93	AVDD	-4910	-895
44	C6+	-7780	-895	94	AVDD	-4860	-895
45	C6+	-7730	-895	95	AVDD	-4810	-895
46	C6-	-7650	-895	96	AVDD	-4760	-895
47	C6-	-7600	-895	97	VR	-4680	-895
48	C6-	-7550	-895	98	VR	-4630	-895
49	C6-	-7500	-895	99	VR	-4580	-895
50	C5+	-7420	-895	100	VR	-4530	-895

Table 9.3.2 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
101	VR	-4480	-895	151	DUMMY	-1200	-895
102	VS	-4400	-895	152	DUMMY	-1120	-895
103	VS	-4350	-895	153	DUMMY	-1040	-895
104	VS	-4300	-895	154	DUMMY	-960	-895
105	VS	-4250	-895	155	DUMMY	-880	-895
106	VS	-4200	-895	156	DUMMY	-800	-895
107	VG	-4120	-895	157	DUMMY	-720	-895
108	VG	-4070	-895	158	DUMMY	-640	-895
109	VG	-4020	-895	159	DUMMY	-560	-895
110	VG	-3970	-895	160	DUMMY	-480	-895
111	VG	-3920	-895	161	DUMMY	-400	-895
112	VSS	-3840	-895	162	DUMMY	-320	-895
113	VSS	-3790	-895	163	DUMMY	-240	-895
114	VSS	-3740	-895	164	DUMMY	-160	-895
115	VSS	-3690	-895	165	DUMMY	-80	-895
116	VSS	-3640	-895	166	DUMMY	0	-895
117	VDD1	-3560	-895	167	DUMMY	80	-895
118	VDD1	-3510	-895	168	DUMMY	160	-895
119	VDD1	-3460	-895	169	DUMMY	240	-895
120	VDD1	-3410	-895	170	V7N	330	-895
121	VDD1	-3360	-895	171	V6N	410	-895
122	RVG	-3280	-895	172	V5N	490	-895
123	FRM	-3200	-895	173	V4N	570	-895
124	EXTC	-3120	-895	174	V3N	650	-895
125	VDD1	-3040	-895	175	V2N	730	-895
126	VDD1	-2990	-895	176	V1N	810	-895
127	VDD1	-2940	-895	177	V0N	890	-895
128	VDD1	-2890	-895	178	V7P	970	-895
129	VDD1	-2840	-895	179	V6P	1050	-895
130	WRB	-2760	-895	180	V5P	1130	-895
131	RESB	-2680	-895	181	V4P	1210	-895
132	RDB	-2600	-895	182	V3P	1290	-895
133	TE	-2520	-895	183	V2P	1370	-895
134	VSS	-2440	-895	184	V1P	1450	-895
135	VSS	-2390	-895	185	V0P	1530	-895
136	VSS	-2340	-895	186	DUMMY	1610	-895
137	VSS	-2290	-895	187	D8	1690	-895
138	VSS	-2240	-895	188	D9	1770	-895
139	D0	-2160	-895	189	D10	1850	-895
140	D1	-2080	-895	190	D11	1930	-895
141	D2	-2000	-895	191	D12	2010	-895
142	D3	-1920	-895	192	D13	2090	-895
143	D4	-1840	-895	193	D14	2170	-895
144	D5	-1760	-895	194	D15	2250	-895
145	D6	-1680	-895	195	D16	2330	-895
146	D7	-1600	-895	196	D17	2410	-895
147	DC	-1520	-895	197	DUMMY	2490	-895
148	CSB	-1440	-895	198	VD0	2570	-895
149	DUMMY	-1360	-895	199	VD1	2650	-895
150	VCOM	-1280	-895	200	VD2	2730	-895

Table 9.3.3 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
201	VD3	2810	-895	251	DUMMY	8170	-895
202	VD4	2890	-895	252	DUMMY	8330	-895
203	VD5	2970	-895	253	DUMMY	8490	-895
204	VD6	3050	-895	254	DUMMY	8650	-895
205	VD7	3130	-895	255	DUMMY	8810	-895
206	VD8	3210	-895	256	CM	8890	-895
207	VD9	3290	-895	257	GM1	8970	-895
208	VD10	3370	-895	258	GM0	9050	-895
209	VD11	3450	-895	259	PVDD1	9130	-895
210	VD12	3530	-895	260	TEST5	9210	-895
211	VD13	3610	-895	261	TEST4	9290	-895
212	VD14	3690	-895	262	PVSS1	9370	-895
213	VD15	3770	-895	263	SRGB	9450	-895
214	VD16	3850	-895	264	SMX	9530	-895
215	VD17	3930	-895	265	SMY	9610	-895
216	VSS	4010	-895	266	PVDD1	9690	-895
217	VSS	4060	-895	267	P68	9770	-895
218	VSS	4110	-895	268	BS1	9850	-895
219	VSS	4160	-895	269	BS0	9930	-895
220	VSS	4210	-895	270	PVSS1	10010	-895
221	VSYNCO	4290	-895	271	TEST2	10090	-895
222	VSYNC	4370	-895	272	OSC	10170	-895
223	HSYNC	4450	-895	273	TEST1	10250	-895
224	ENABLE	4530	-895	274	DUMMY	10330	-895
225	DCK	4610	-895	275	DUMMY	10610	-895
226	VDD1	4690	-895	276	DUMMY	10615	-675
227	VDD1	4740	-895	277	DUMMY	10470	-650
228	VDD1	4790	-895	278	G<240>	10615	-625
229	VDD1	4840	-895	279	G<238>	10470	-600
230	VDD1	4890	-895	280	G<236>	10615	-575
231	DUMMY	4970	-895	281	G<234>	10470	-550
232	DUMMY	5130	-895	282	G<232>	10615	-525
233	DUMMY	5290	-895	283	G<230>	10470	-500
234	DUMMY	5450	-895	284	G<228>	10615	-475
235	DUMMY	5610	-895	285	G<226>	10470	-450
236	DUMMY	5770	-895	286	G<224>	10615	-425
237	DUMMY	5930	-895	287	G<222>	10470	-400
238	DUMMY	6090	-895	288	G<220>	10615	-375
239	DUMMY	6250	-895	289	G<218>	10470	-350
240	DUMMY	6410	-895	290	G<216>	10615	-325
241	DUMMY	6570	-895	291	G<214>	10470	-300
242	DUMMY	6730	-895	292	G<212>	10615	-275
243	DUMMY	6890	-895	293	G<210>	10470	-250
244	DUMMY	7050	-895	294	G<208>	10615	-225
245	DUMMY	7210	-895	295	G<206>	10470	-200
246	DUMMY	7370	-895	296	G<204>	10615	-175
247	DUMMY	7530	-895	297	G<202>	10470	-150
248	DUMMY	7690	-895	298	G<200>	10615	-125
249	DUMMY	7850	-895	299	G<198>	10470	-100
250	DUMMY	8010	-895	300	G<196>	10615	-75

Table 9.3.4 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
301	G<194>	10470	-50	351	G<102>	9775	900
302	G<192>	10615	-25	352	G<100>	9750	755
303	G<190>	10470	0	353	G<98>	9725	900
304	G<188>	10615	25	354	G<96>	9700	755
305	G<186>	10470	50	355	G<94>	9675	900
306	G<184>	10615	75	356	G<92>	9650	755
307	G<182>	10470	100	357	G<90>	9625	900
308	G<180>	10615	125	358	G<88>	9600	755
309	G<178>	10470	150	359	G<86>	9575	900
310	G<176>	10615	175	360	G<84>	9550	755
311	G<174>	10470	200	361	G<82>	9525	900
312	G<172>	10615	225	362	G<80>	9500	755
313	G<170>	10470	250	363	G<78>	9475	900
314	G<168>	10615	275	364	G<76>	9450	755
315	G<166>	10470	300	365	G<74>	9425	900
316	G<164>	10615	325	366	G<72>	9400	755
317	G<162>	10470	350	367	G<70>	9375	900
318	G<160>	10615	375	368	G<68>	9350	755
319	G<158>	10470	400	369	G<66>	9325	900
320	G<156>	10615	425	370	G<64>	9300	755
321	G<154>	10470	450	371	G<62>	9275	900
322	G<152>	10615	475	372	G<60>	9250	755
323	G<150>	10470	500	373	G<58>	9225	900
324	G<148>	10615	525	374	G<56>	9200	755
325	G<146>	10470	550	375	G<54>	9175	900
326	G<144>	10615	575	376	G<52>	9150	755
327	G<142>	10470	600	377	G<50>	9125	900
328	G<140>	10615	625	378	G<48>	9100	755
329	DUMMY	10470	650	379	G<46>	9075	900
330	DUMMY	10615	675	380	G<44>	9050	755
331	DUMMY	10275	900	381	G<42>	9025	900
332	DUMMY	10250	755	382	G<40>	9000	755
333	G<138>	10225	900	383	G<38>	8975	900
334	G<136>	10200	755	384	G<36>	8950	755
335	G<134>	10175	900	385	G<34>	8925	900
336	G<132>	10150	755	386	G<32>	8900	755
337	G<130>	10125	900	387	G<30>	8875	900
338	G<128>	10100	755	388	G<28>	8850	755
339	G<126>	10075	900	389	G<26>	8825	900
340	G<124>	10050	755	390	G<24>	8800	755
341	G<122>	10025	900	391	G<22>	8775	900
342	G<120>	10000	755	392	G<20>	8750	755
343	G<118>	9975	900	393	G<18>	8725	900
344	G<116>	9950	755	394	G<16>	8700	755
345	G<114>	9925	900	395	G<14>	8675	900
346	G<112>	9900	755	396	G<12>	8650	755
347	G<110>	9875	900	397	G<10>	8625	900
348	G<108>	9850	755	398	G<8>	8600	755
349	G<106>	9825	900	399	G<6>	8575	900
350	G<104>	9800	755	400	G<4>	8550	755

Table 9.3.5 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
401	G<2>	8525	900	451	S<490>	7080	915
402	G<0>	8500	755	452	S<489>	7050	780
403	DUMMY	8475	900	453	S<488>	7020	915
404	DUMMY	8450	755	454	S<487>	6990	780
405	VCOM	8425	900	455	S<486>	6960	915
406	VCOM	8400	755	456	S<485>	6930	780
407	VCOM	8375	900	457	S<484>	6900	915
408	VCOM	8350	755	458	S<483>	6870	780
409	VCOM	8325	900	459	S<482>	6840	915
410	VCOM	8300	755	460	S<481>	6810	780
411	DUMMY	8275	900	461	S<480>	6780	915
412	DUMMY	8250	755	462	S<479>	6750	780
413	S<528>	8220	915	463	S<478>	6720	915
414	S<527>	8190	780	464	S<477>	6690	780
415	S<526>	8160	915	465	S<476>	6660	915
416	S<525>	8130	780	466	S<475>	6630	780
417	S<524>	8100	915	467	S<474>	6600	915
418	S<523>	8070	780	468	S<473>	6570	780
419	S<522>	8040	915	469	S<472>	6540	915
420	S<521>	8010	780	470	S<471>	6510	780
421	S<520>	7980	915	471	S<470>	6480	915
422	S<519>	7950	780	472	S<469>	6450	780
423	S<518>	7920	915	473	S<468>	6420	915
424	S<517>	7890	780	474	S<467>	6390	780
425	S<516>	7860	915	475	S<466>	6360	915
426	S<515>	7830	780	476	S<465>	6330	780
427	S<514>	7800	915	477	S<464>	6300	915
428	S<513>	7770	780	478	S<463>	6270	780
429	S<512>	7740	915	479	S<462>	6240	915
430	S<511>	7710	780	480	S<461>	6210	780
431	S<510>	7680	915	481	S<460>	6180	915
432	S<509>	7650	780	482	S<459>	6150	780
433	S<508>	7620	915	483	S<458>	6120	915
434	S<507>	7590	780	484	S<457>	6090	780
435	S<506>	7560	915	485	S<456>	6060	915
436	S<505>	7530	780	486	S<455>	6030	780
437	S<504>	7500	915	487	S<454>	6000	915
438	S<503>	7470	780	488	S<453>	5970	780
439	S<502>	7440	915	489	S<452>	5940	915
440	S<501>	7410	780	490	S<451>	5910	780
441	S<500>	7380	915	491	S<450>	5880	915
442	S<499>	7350	780	492	S<449>	5850	780
443	S<498>	7320	915	493	S<448>	5820	915
444	S<497>	7290	780	494	S<447>	5790	780
445	S<496>	7260	915	495	S<446>	5760	915
446	S<495>	7230	780	496	S<445>	5730	780
447	S<494>	7200	915	497	S<444>	5700	915
448	S<493>	7170	780	498	S<443>	5670	780
449	S<492>	7140	915	499	S<442>	5640	915
450	S<491>	7110	780	500	S<441>	5610	780

Table 9.3.6 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
501	S<440>	5580	915	551	S<390>	4080	915
502	S<439>	5550	780	552	S<389>	4050	780
503	S<438>	5520	915	553	S<388>	4020	915
504	S<437>	5490	780	554	S<387>	3990	780
505	S<436>	5460	915	555	S<386>	3960	915
506	S<435>	5430	780	556	S<385>	3930	780
507	S<434>	5400	915	557	S<384>	3900	915
508	S<433>	5370	780	558	S<383>	3870	780
509	S<432>	5340	915	559	S<382>	3840	915
510	S<431>	5310	780	560	S<381>	3810	780
511	S<430>	5280	915	561	S<380>	3780	915
512	S<429>	5250	780	562	S<379>	3750	780
513	S<428>	5220	915	563	S<378>	3720	915
514	S<427>	5190	780	564	S<377>	3690	780
515	S<426>	5160	915	565	S<376>	3660	915
516	S<425>	5130	780	566	S<375>	3630	780
517	S<424>	5100	915	567	S<374>	3600	915
518	S<423>	5070	780	568	S<373>	3570	780
519	S<422>	5040	915	569	S<372>	3540	915
520	S<421>	5010	780	570	S<371>	3510	780
521	S<420>	4980	915	571	S<370>	3480	915
522	S<419>	4950	780	572	S<369>	3450	780
523	S<418>	4920	915	573	S<368>	3420	915
524	S<417>	4890	780	574	S<367>	3390	780
525	S<416>	4860	915	575	S<366>	3360	915
526	S<415>	4830	780	576	S<365>	3330	780
527	S<414>	4800	915	577	S<364>	3300	915
528	S<413>	4770	780	578	S<363>	3270	780
529	S<412>	4740	915	579	S<362>	3240	915
530	S<411>	4710	780	580	S<361>	3210	780
531	S<410>	4680	915	581	S<360>	3180	915
532	S<409>	4650	780	582	S<359>	3150	780
533	S<408>	4620	915	583	S<358>	3120	915
534	S<407>	4590	780	584	S<357>	3090	780
535	S<406>	4560	915	585	S<356>	3060	915
536	S<405>	4530	780	586	S<355>	3030	780
537	S<404>	4500	915	587	S<354>	3000	915
538	S<403>	4470	780	588	S<353>	2970	780
539	S<402>	4440	915	589	S<352>	2940	915
540	S<401>	4410	780	590	S<351>	2910	780
541	S<400>	4380	915	591	S<350>	2880	915
542	S<399>	4350	780	592	S<349>	2850	780
543	S<398>	4320	915	593	S<348>	2820	915
544	S<397>	4290	780	594	S<347>	2790	780
545	S<396>	4260	915	595	S<346>	2760	915
546	S<395>	4230	780	596	S<345>	2730	780
547	S<394>	4200	915	597	S<344>	2700	915
548	S<393>	4170	780	598	S<343>	2670	780
549	S<392>	4140	915	599	S<342>	2640	915
550	S<391>	4110	780	600	S<341>	2610	780

Table 9.3.7 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
601	S<340>	2580	915	651	S<290>	1080	915
602	S<339>	2550	780	652	S<289>	1050	780
603	S<338>	2520	915	653	S<288>	1020	915
604	S<337>	2490	780	654	S<287>	990	780
605	S<336>	2460	915	655	S<286>	960	915
606	S<335>	2430	780	656	S<285>	930	780
607	S<334>	2400	915	657	S<284>	900	915
608	S<333>	2370	780	658	S<283>	870	780
609	S<332>	2340	915	659	S<282>	840	915
610	S<331>	2310	780	660	S<281>	810	780
611	S<330>	2280	915	661	S<280>	780	915
612	S<329>	2250	780	662	S<279>	750	780
613	S<328>	2220	915	663	S<278>	720	915
614	S<327>	2190	780	664	S<277>	690	780
615	S<326>	2160	915	665	S<276>	660	915
616	S<325>	2130	780	666	S<275>	630	780
617	S<324>	2100	915	667	S<274>	600	915
618	S<323>	2070	780	668	S<273>	570	780
619	S<322>	2040	915	669	S<272>	540	915
620	S<321>	2010	780	670	S<271>	510	780
621	S<320>	1980	915	671	S<270>	480	915
622	S<319>	1950	780	672	S<269>	450	780
623	S<318>	1920	915	673	S<268>	420	915
624	S<317>	1890	780	674	S<267>	390	780
625	S<316>	1860	915	675	S<266>	360	915
626	S<315>	1830	780	676	S<265>	330	780
627	S<314>	1800	915	677	DUMMY	300	915
628	S<313>	1770	780	678	DUMMY	270	780
629	S<312>	1740	915	679	DUMMY	240	915
630	S<311>	1710	780	680	DUMMY	210	780
631	S<310>	1680	915	681	DUMMY	180	915
632	S<309>	1650	780	682	DUMMY	150	780
633	S<308>	1620	915	683	DUMMY	120	915
634	S<307>	1590	780	684	DUMMY	90	780
635	S<306>	1560	915	685	DUMMY	60	915
636	S<305>	1530	780	686	DUMMY	30	780
637	S<304>	1500	915	687	DUMMY	0	915
638	S<303>	1470	780	688	DUMMY	-30	780
639	S<302>	1440	915	689	DUMMY	-60	915
640	S<301>	1410	780	690	DUMMY	-90	780
641	S<300>	1380	915	691	DUMMY	-120	915
642	S<299>	1350	780	692	DUMMY	-150	780
643	S<298>	1320	915	693	DUMMY	-180	915
644	S<297>	1290	780	694	DUMMY	-210	780
645	S<296>	1260	915	695	DUMMY	-240	915
646	S<295>	1230	780	696	DUMMY	-270	780
647	S<294>	1200	915	697	DUMMY	-300	915
648	S<293>	1170	780	698	S<264>	-330	780
649	S<292>	1140	915	699	S<263>	-360	915
650	S<291>	1110	780	700	S<262>	-390	780

Table 9.3.8 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
701	S<261>	-420	915	751	S<211>	-1920	915
702	S<260>	-450	780	752	S<210>	-1950	780
703	S<259>	-480	915	753	S<209>	-1980	915
704	S<258>	-510	780	754	S<208>	-2010	780
705	S<257>	-540	915	755	S<207>	-2040	915
706	S<256>	-570	780	756	S<206>	-2070	780
707	S<255>	-600	915	757	S<205>	-2100	915
708	S<254>	-630	780	758	S<204>	-2130	780
709	S<253>	-660	915	759	S<203>	-2160	915
710	S<252>	-690	780	760	S<202>	-2190	780
711	S<251>	-720	915	761	S<201>	-2220	915
712	S<250>	-750	780	762	S<200>	-2250	780
713	S<249>	-780	915	763	S<199>	-2280	915
714	S<248>	-810	780	764	S<198>	-2310	780
715	S<247>	-840	915	765	S<197>	-2340	915
716	S<246>	-870	780	766	S<196>	-2370	780
717	S<245>	-900	915	767	S<195>	-2400	915
718	S<244>	-930	780	768	S<194>	-2430	780
719	S<243>	-960	915	769	S<193>	-2460	915
720	S<242>	-990	780	770	S<192>	-2490	780
721	S<241>	-1020	915	771	S<191>	-2520	915
722	S<240>	-1050	780	772	S<190>	-2550	780
723	S<239>	-1080	915	773	S<189>	-2580	915
724	S<238>	-1110	780	774	S<188>	-2610	780
725	S<237>	-1140	915	775	S<187>	-2640	915
726	S<236>	-1170	780	776	S<186>	-2670	780
727	S<235>	-1200	915	777	S<185>	-2700	915
728	S<234>	-1230	780	778	S<184>	-2730	780
729	S<233>	-1260	915	779	S<183>	-2760	915
730	S<232>	-1290	780	780	S<182>	-2790	780
731	S<231>	-1320	915	781	S<181>	-2820	915
732	S<230>	-1350	780	782	S<180>	-2850	780
733	S<229>	-1380	915	783	S<179>	-2880	915
734	S<228>	-1410	780	784	S<178>	-2910	780
735	S<227>	-1440	915	785	S<177>	-2940	915
736	S<226>	-1470	780	786	S<176>	-2970	780
737	S<225>	-1500	915	787	S<175>	-3000	915
738	S<224>	-1530	780	788	S<174>	-3030	780
739	S<223>	-1560	915	789	S<173>	-3060	915
740	S<222>	-1590	780	790	S<172>	-3090	780
741	S<221>	-1620	915	791	S<171>	-3120	915
742	S<220>	-1650	780	792	S<170>	-3150	780
743	S<219>	-1680	915	793	S<169>	-3180	915
744	S<218>	-1710	780	794	S<168>	-3210	780
745	S<217>	-1740	915	795	S<167>	-3240	915
746	S<216>	-1770	780	796	S<166>	-3270	780
747	S<215>	-1800	915	797	S<165>	-3300	915
748	S<214>	-1830	780	798	S<164>	-3330	780
749	S<213>	-1860	915	799	S<163>	-3360	915
750	S<212>	-1890	780	800	S<162>	-3390	780

Table 9.3.9 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
801	S<161>	-3420	915	851	S<111>	-4920	915
802	S<160>	-3450	780	852	S<110>	-4950	780
803	S<159>	-3480	915	853	S<109>	-4980	915
804	S<158>	-3510	780	854	S<108>	-5010	780
805	S<157>	-3540	915	855	S<107>	-5040	915
806	S<156>	-3570	780	856	S<106>	-5070	780
807	S<155>	-3600	915	857	S<105>	-5100	915
808	S<154>	-3630	780	858	S<104>	-5130	780
809	S<153>	-3660	915	859	S<103>	-5160	915
810	S<152>	-3690	780	860	S<102>	-5190	780
811	S<151>	-3720	915	861	S<101>	-5220	915
812	S<150>	-3750	780	862	S<100>	-5250	780
813	S<149>	-3780	915	863	S<99>	-5280	915
814	S<148>	-3810	780	864	S<98>	-5310	780
815	S<147>	-3840	915	865	S<97>	-5340	915
816	S<146>	-3870	780	866	S<96>	-5370	780
817	S<145>	-3900	915	867	S<95>	-5400	915
818	S<144>	-3930	780	868	S<94>	-5430	780
819	S<143>	-3960	915	869	S<93>	-5460	915
820	S<142>	-3990	780	870	S<92>	-5490	780
821	S<141>	-4020	915	871	S<91>	-5520	915
822	S<140>	-4050	780	872	S<90>	-5550	780
823	S<139>	-4080	915	873	S<89>	-5580	915
824	S<138>	-4110	780	874	S<88>	-5610	780
825	S<137>	-4140	915	875	S<87>	-5640	915
826	S<136>	-4170	780	876	S<86>	-5670	780
827	S<135>	-4200	915	877	S<85>	-5700	915
828	S<134>	-4230	780	878	S<84>	-5730	780
829	S<133>	-4260	915	879	S<83>	-5760	915
830	S<132>	-4290	780	880	S<82>	-5790	780
831	S<131>	-4320	915	881	S<81>	-5820	915
832	S<130>	-4350	780	882	S<80>	-5850	780
833	S<129>	-4380	915	883	S<79>	-5880	915
834	S<128>	-4410	780	884	S<78>	-5910	780
835	S<127>	-4440	915	885	S<77>	-5940	915
836	S<126>	-4470	780	886	S<76>	-5970	780
837	S<125>	-4500	915	887	S<75>	-6000	915
838	S<124>	-4530	780	888	S<74>	-6030	780
839	S<123>	-4560	915	889	S<73>	-6060	915
840	S<122>	-4590	780	890	S<72>	-6090	780
841	S<121>	-4620	915	891	S<71>	-6120	915
842	S<120>	-4650	780	892	S<70>	-6150	780
843	S<119>	-4680	915	893	S<69>	-6180	915
844	S<118>	-4710	780	894	S<68>	-6210	780
845	S<117>	-4740	915	895	S<67>	-6240	915
846	S<116>	-4770	780	896	S<66>	-6270	780
847	S<115>	-4800	915	897	S<65>	-6300	915
848	S<114>	-4830	780	898	S<64>	-6330	780
849	S<113>	-4860	915	899	S<63>	-6360	915
850	S<112>	-4890	780	900	S<62>	-6390	780

Table 9.3.10 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
901	S<61>	-6420	915	951	S<11>	-7920	915
902	S<60>	-6450	780	952	S<10>	-7950	780
903	S<59>	-6480	915	953	S<9>	-7980	915
904	S<58>	-6510	780	954	S<8>	-8010	780
905	S<57>	-6540	915	955	S<7>	-8040	915
906	S<56>	-6570	780	956	S<6>	-8070	780
907	S<55>	-6600	915	957	S<5>	-8100	915
908	S<54>	-6630	780	958	S<4>	-8130	780
909	S<53>	-6660	915	959	S<3>	-8160	915
910	S<52>	-6690	780	960	S<2>	-8190	780
911	S<51>	-6720	915	961	S<1>	-8220	915
912	S<50>	-6750	780	962	DUMMY	-8250	755
913	S<49>	-6780	915	963	DUMMY	-8275	900
914	S<48>	-6810	780	964	VCOM	-8300	755
915	S<47>	-6840	915	965	VCOM	-8325	900
916	S<46>	-6870	780	966	VCOM	-8350	755
917	S<45>	-6900	915	967	VCOM	-8375	900
918	S<44>	-6930	780	968	VCOM	-8400	755
919	S<43>	-6960	915	969	VCOM	-8425	900
920	S<42>	-6990	780	970	DUMMY	-8450	755
921	S<41>	-7020	915	971	DUMMY	-8475	900
922	S<40>	-7050	780	972	G<1>	-8500	755
923	S<39>	-7080	915	973	G<3>	-8525	900
924	S<38>	-7110	780	974	G<5>	-8550	755
925	S<37>	-7140	915	975	G<7>	-8575	900
926	S<36>	-7170	780	976	G<9>	-8600	755
927	S<35>	-7200	915	977	G<11>	-8625	900
928	S<34>	-7230	780	978	G<13>	-8650	755
929	S<33>	-7260	915	979	G<15>	-8675	900
930	S<32>	-7290	780	980	G<17>	-8700	755
931	S<31>	-7320	915	981	G<19>	-8725	900
932	S<30>	-7350	780	982	G<21>	-8750	755
933	S<29>	-7380	915	983	G<23>	-8775	900
934	S<28>	-7410	780	984	G<25>	-8800	755
935	S<27>	-7440	915	985	G<27>	-8825	900
936	S<26>	-7470	780	986	G<29>	-8850	755
937	S<25>	-7500	915	987	G<31>	-8875	900
938	S<24>	-7530	780	988	G<33>	-8900	755
939	S<23>	-7560	915	989	G<35>	-8925	900
940	S<22>	-7590	780	990	G<37>	-8950	755
941	S<21>	-7620	915	991	G<39>	-8975	900
942	S<20>	-7650	780	992	G<41>	-9000	755
943	S<19>	-7680	915	993	G<43>	-9025	900
944	S<18>	-7710	780	994	G<45>	-9050	755
945	S<17>	-7740	915	995	G<47>	-9075	900
946	S<16>	-7770	780	996	G<49>	-9100	755
947	S<15>	-7800	915	997	G<51>	-9125	900
948	S<14>	-7830	780	998	G<53>	-9150	755
949	S<13>	-7860	915	999	G<55>	-9175	900
950	S<12>	-7890	780	1000	G<57>	-9200	755

Table 9.3.11 Pad Center Coordinates (Continued)

No	Name	X	Y	No	Name	X	Y
1001	G<59>	-9225	900	1051	G<151>	-10470	500
1002	G<61>	-9250	755	1052	G<153>	-10615	475
1003	G<63>	-9275	900	1053	G<155>	-10470	450
1004	G<65>	-9300	755	1054	G<157>	-10615	425
1005	G<67>	-9325	900	1055	G<159>	-10470	400
1006	G<69>	-9350	755	1056	G<161>	-10615	375
1007	G<71>	-9375	900	1057	G<163>	-10470	350
1008	G<73>	-9400	755	1058	G<165>	-10615	325
1009	G<75>	-9425	900	1059	G<167>	-10470	300
1010	G<77>	-9450	755	1060	G<169>	-10615	275
1011	G<79>	-9475	900	1061	G<171>	-10470	250
1012	G<81>	-9500	755	1062	G<173>	-10615	225
1013	G<83>	-9525	900	1063	G<175>	-10470	200
1014	G<85>	-9550	755	1064	G<177>	-10615	175
1015	G<87>	-9575	900	1065	G<179>	-10470	150
1016	G<89>	-9600	755	1066	G<181>	-10615	125
1017	G<91>	-9625	900	1067	G<183>	-10470	100
1018	G<93>	-9650	755	1068	G<185>	-10615	75
1019	G<95>	-9675	900	1069	G<187>	-10470	50
1020	G<97>	-9700	755	1070	G<189>	-10615	25
1021	G<99>	-9725	900	1071	G<191>	-10470	0
1022	G<101>	-9750	755	1072	G<193>	-10615	-25
1023	G<103>	-9775	900	1073	G<195>	-10470	-50
1024	G<105>	-9800	755	1074	G<197>	-10615	-75
1025	G<107>	-9825	900	1075	G<199>	-10470	-100
1026	G<109>	-9850	755	1076	G<201>	-10615	-125
1027	G<111>	-9875	900	1077	G<203>	-10470	-150
1028	G<113>	-9900	755	1078	G<205>	-10615	-175
1029	G<115>	-9925	900	1079	G<207>	-10470	-200
1030	G<117>	-9950	755	1080	G<209>	-10615	-225
1031	G<119>	-9975	900	1081	G<211>	-10470	-250
1032	G<121>	-10000	755	1082	G<213>	-10615	-275
1033	G<123>	-10025	900	1083	G<215>	-10470	-300
1034	G<125>	-10050	755	1084	G<217>	-10615	-325
1035	G<127>	-10075	900	1085	G<219>	-10470	-350
1036	G<129>	-10100	755	1086	G<221>	-10615	-375
1037	G<131>	-10125	900	1087	G<223>	-10470	-400
1038	G<133>	-10150	755	1088	G<225>	-10615	-425
1039	G<135>	-10175	900	1089	G<227>	-10470	-450
1040	G<137>	-10200	755	1090	G<229>	-10615	-475
1041	G<139>	-10225	900	1091	G<231>	-10470	-500
1042	DUMMY	-10250	755	1092	G<233>	-10615	-525
1043	DUMMY	-10275	900	1093	G<235>	-10470	-550
1044	DUMMY	-10615	675	1094	G<237>	-10615	-575
1045	DUMMY	-10470	650	1095	G<239>	-10470	-600
1046	G<141>	-10615	625	1096	DUMMY	-10615	-625
1047	G<143>	-10470	600	1097	DUMMY	-10470	-650
1048	G<145>	-10615	575	1098	DUMMY	-10615	-675
1049	G<147>	-10470	550	KEY_LEFT		-10470	-875
1050	G<149>	-10615	525	KEY_RIGHT		10470	-875